CD4538 Dual Precision Monostable

General Description

The CD4538BC is a dual, precision monostable multivibrator with independent trigger and reset controls. The device is retriggerable and resettable, and the control inputs are internally latched. Two trigger inputs are provided to allow either rising or falling edge triggering. The reset inputs are active LOW and prevent triggering while active. Precise control of output pulse-width has been achieved using linear CMOS techniques. The pulse duration and accuracy are determined by external components R_X and C_X. The device does not allow the timing capacitor to discharge through the timing pin on power-down condition. For this reason, no external protection resistor is required in series with the timing pin. Input protection from static discharge is provided on all pins.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- New formula: PW_{OUT} = RC (PW in seconds, R in Ohms, C in Farads)
- ±1.0% pulse-width variation from part to part (typ.)
- Wide pulse-width range: 1 µs to ∞
- Separate latched reset inputs
- Symmetrical output sink and source capability
- Low standby current: 5 nA (typ.) @ 5 V_{DC}
- Pin compatible to CD4528BC

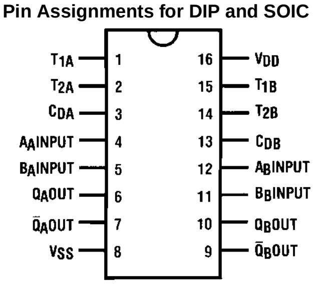
Ordering Code:

Order Number	Package Number	Package Description
CD4538BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD4538BCWM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
CD4538BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP and SOIC



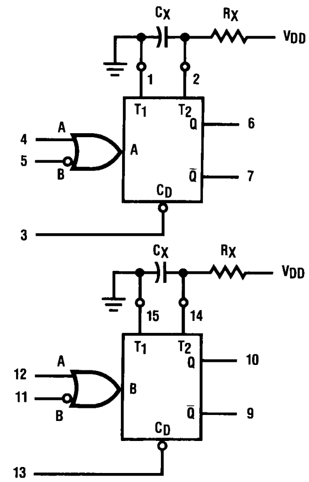
Top View

Truth Table

Inputs			Outputs	
Clear	**A**	**B**	**Q**	**$\overline{Q}$**
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⊓	⊔
H	↑	H	⊓	⊔

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⊓ = One HIGH Level Pulse
⊔ = One LOW Level Pulse
X = Irrelevant

Block Diagram



R_X and C_X are External Components

V_{DD} = Pin 16

V_{SS} = Pin 8

Logic Diagram

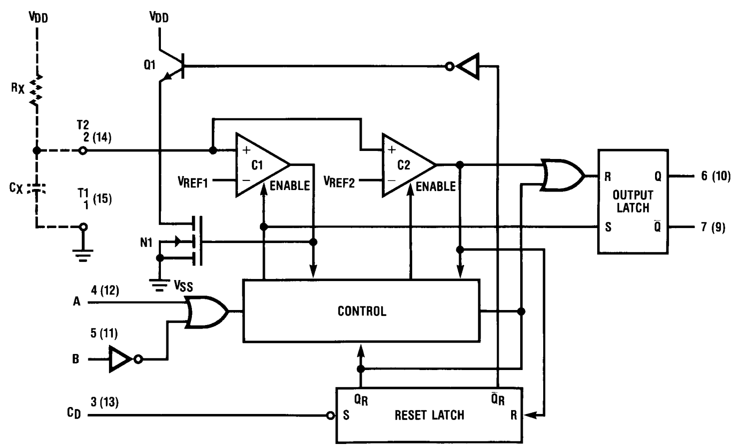


FIGURE 1.

Theory of Operation

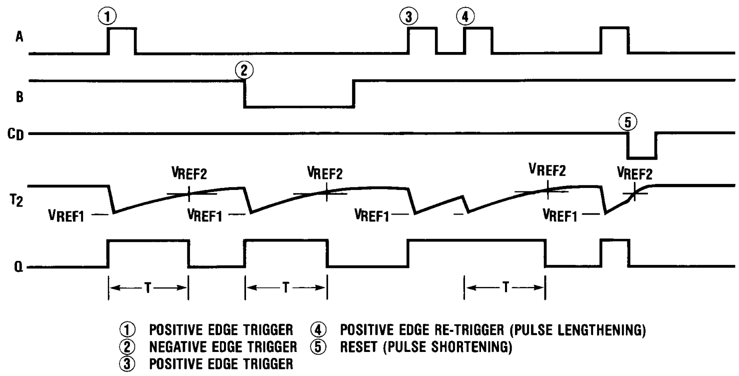


FIGURE 2.

Trigger Operation

The block diagram of the CD4538BC is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and Figure 2, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and C_D are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1(1). At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from V_{DD} to V_{SS} (while input A is at V_{SS} and input C_D is at V_{DD})(2).

It should be noted that in the quiescent state C_X is fully charged to V_{DD}, causing the current through resistor R_X to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the CD4538BC is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

Retrigger Operation

The CD4538BC is retriggered if a valid trigger occurs(3) followed by another valid trigger(4) before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated(4), the voltage at T2 will again drop to V_{REF1} before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

Reset Operation

The CD4538BC may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on C_D sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor Q1(5). When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the C_D input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

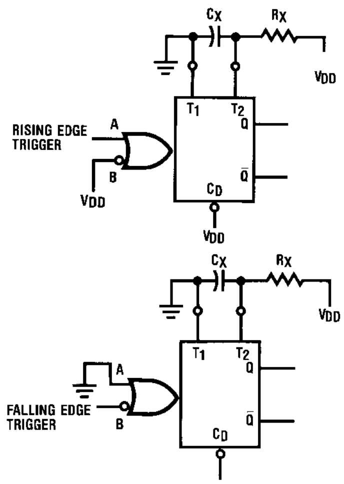


FIGURE 3. Retriggerable Monostables Circuitry

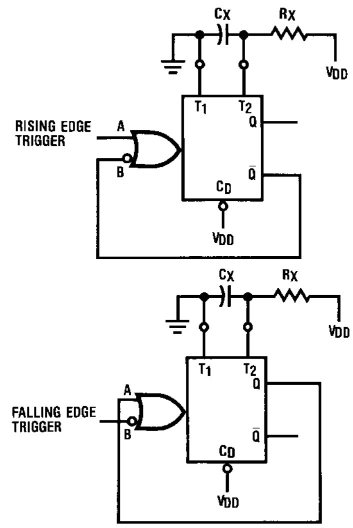


FIGURE 4. Non-Retriggerable Monostables Circuitry

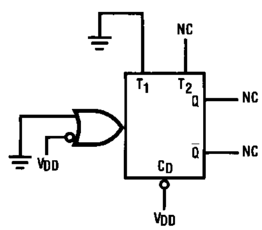


FIGURE 5. Connection of Unused Sections

Absolute Maximum Ratings(Note 1)

(Note 2)

DC Supply Voltage (V_{DD})	–0.5 to +18 V_{DC}
Input Voltage (V_{IN})	–0.5V to V_{DD} + 0.5 V_{DC}
Storage Temperature Range (T_S)	–65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	–40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions		–40°C		+25°C			+85°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent	V_{DD} = 5V	V_{IH} = V_{DD}		20		0.005	20		150	µA
	Device Current	V_{DD} = 10V	V_{IL} = V_{SS}		40		0.010	40		300	µA
		V_{DD} = 15V	All Outputs Open		80		0.015	80		600	µA
V_{OL}	LOW Level	V_{DD} = 5V	$\|I_O\|$ < 1 µA		0.05		0	0.05		0.05	V
	Output Voltage	V_{DD} = 10V	V_{IH} = V_{DD}, V_{IL} = V_{SS}		0.05		0	0.05		0.05	V
		V_{DD} = 15V			0.05		0	0.05		0.05	V
V_{OH}	HIGH Level	V_{DD} = 5V	$\|I_O\|$ < 1 µA	4.95		4.95	5		4.95		V
	Output Voltage	V_{DD} = 10V	V_{IH} = V_{DD}, V_{IL} = V_{SS}	9.95		9.95	10		9.95		V
		V_{DD} = 15V		14.95		14.95	15		14.95		V
V_{IL}	LOW Level	$\|I_O\|$ < 1 µA									
	Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V			1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V			3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V			4.0		6.75	4.0		4.0	V
V_{IH}	HIGH Level	$\|I_O\|$ < 1 µA									
	Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		11.0		11.0	8.25		11.0		V
I_{OL}	LOW Level	V_{DD} = 5V, V_O = 0.4V	V_{IH} = V_{DD}	0.52		0.44	0.88		0.36		mA
	Output Current	V_{DD} = 10V, V_O = 0.5V	V_{IL} = V_{SS}	1.3		1.1	2.25		0.9		mA
	(Note 3)	V_D = 15V, V_O = 1.5V		3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level	V_{DD} = 5V, V_O = 4.6V		–0.52		–0.44	–0.88		–0.36		mA
	Output Current	V_{DD} = 10V, V_O = 9.5V	V_{IL} = V_{SS}	–1.3		–1.1	–2.25		–0.9		mA
	(Note 3)	V_D = 15V, V_O = 13.5V		–3.6		–3.0	–8.8		–2.4		mA
I_{IN}	Input Current, Pin 2 or 14	V_{DD} = 15V, V_{IN} = 0V or 15V			±0.02		$\pm 10^{-5}$	±0.05		±0.5	µA
I_{IN}	Input Current Other Inputs	V_{DD} = 15V, V_{IN} = 0V or 15V			±0.3		$\pm 10^{-5}$	±0.3		±1.0	µA

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 4)

$T_A = 25°C$, $C_L = 50$ pF, and $t_r = t_f = 20$ ns unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{TLH}, t_{THL}	Output Transition Time	$V_{DD} = 5V$			100	200	ns
		$V_{DD} = 10V$			50	100	ns
		$V_{DD} = 15V$			40	80	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Trigger Operation—					
		A or B to Q or $\overline{Q}$					
		$V_{DD} = 5V$			300	600	ns
		$V_{DD} = 10V$			150	300	ns
		$V_{DD} = 15V$			100	220	ns
		Reset Operation—					
		C_D to Q or $\overline{Q}$					
		$V_{DD} = 5V$			250	500	ns
		$V_{DD} = 10V$			125	250	ns
		$V_{DD} = 15V$			95	190	ns
t_{WL}, t_{WH}	Minimum Input Pulse Width	$V_{DD} = 5V$			35	70	ns
	A, B, or C_D	$V_{DD} = 10V$			30	60	ns
		$V_{DD} = 15V$			25	50	ns
t_{RR}	Minimum Retrigger Time	$V_{DD} = 5V$				0	ns
		$V_{DD} = 10V$			0	0	ns
		$V_{DD} = 15V$				0	ns
C_{IN}	Input Capacitance	Pin 2 or 14			10		pF
		Other Inputs			5	7.5	pF
PW_{OUT}	Output Pulse Width (Q or $\overline{Q}$)	$R_X = 100$ kΩ	$V_{DD} = 5V$	208	226	244	µs
	(**Note:** For Typical Distribution,	$C_X = 0.002$ µF	$V_{DD} = 10V$	211	230	248	µs
	see Figure 6)		$V_{DD} = 15V$	216	235	254	µs
		$R_X = 100$ kΩ	$V_{DD} = 5V$	8.83	9.60	10.37	ms
		$C_X = 0.1$ µF	$V_{DD} = 10V$	9.02	9.80	10.59	ms
			$V_{DD} = 15V$	9.20	10.00	10.80	ms
		$R_X = 100$ kΩ	$V_{DD} = 5V$	0.87	0.95	1.03	s
		$C_X = 10.0$ µF	$V_{DD} = 10V$	0.89	0.97	1.05	s
			$V_{DD} = 15V$	0.91	0.99	1.07	s
Pulse Width Match between		$R_X = 100$ kΩ	$V_{DD} = 5V$		±1		%
Circuits in the Same Package		$C_X = 0.1$ µF	$V_{DD} = 10V$		±1		%
$C_X = 0.1$ µF, $R_X = 100$ kΩ			$V_{DD} = 15V$		±1		%
Operating Conditions							
R_X	External Timing Resistance			5.0		(Note 5)	kΩ
C_X	External Timing Capacitance			0		No Limit	pF

Note 4: AC parameters are guaranteed by DC correlated testing.

Note 5: The maximum usable resistance R_X is a function of the leakage of the Capacitor C_X, leakage of the CD4538BC, and leakage due to board layout, surface resistance, etc.

Typical Applications

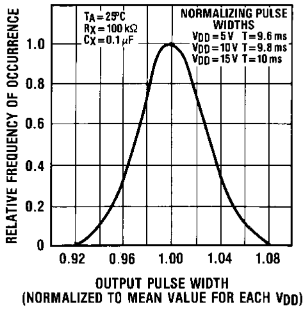


FIGURE 6. Typical Normalized Distribution of Units for Output Pulse Width

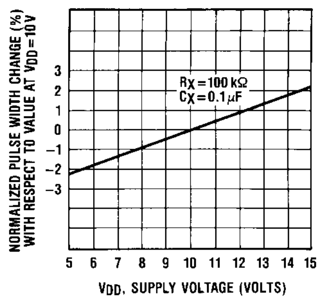


FIGURE 7. Typical Pulse Width Variation as a Function of Supply Voltage V_{DD}

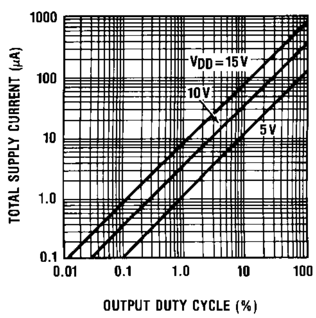


FIGURE 8. Typical Total Supply Current Versus Output Duty Cycle, $R_X = 100\ k\Omega$, $C_L = 50\ pF$, $C_X = 100\ pF$, One Monostable Switching Only

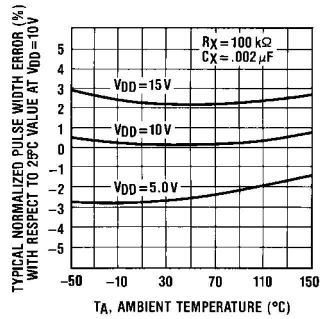


FIGURE 9. Typical Pulse Width Error Versus Temperature

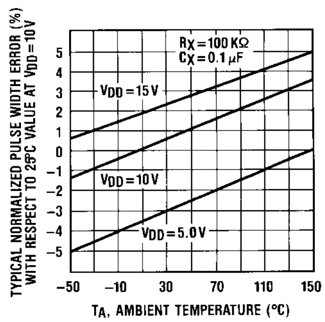


FIGURE 10. Typical Pulse Width Error Versus Temperature

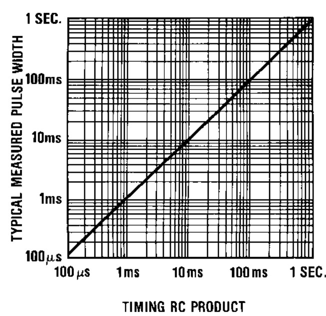


FIGURE 11. Typical Pulse Width Versus Timing RC Product

Test Circuits and Waveforms

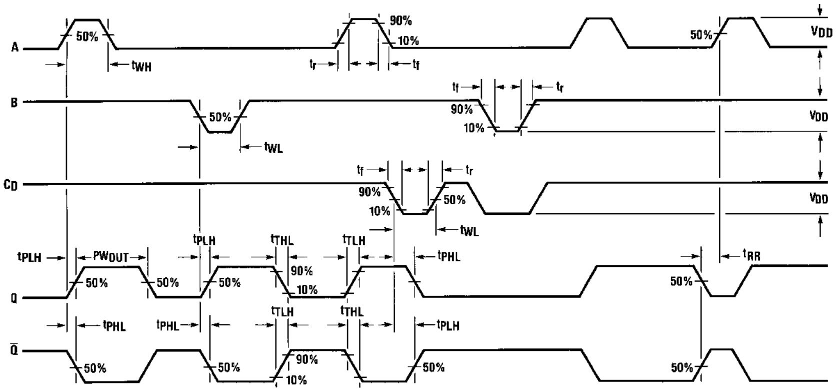
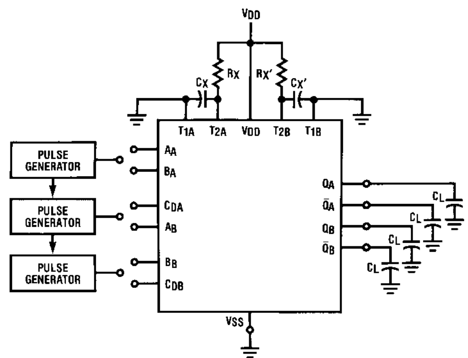


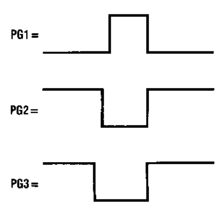
FIGURE 12. Switching Test Waveforms



*C_L = 50 pF

Input Connections

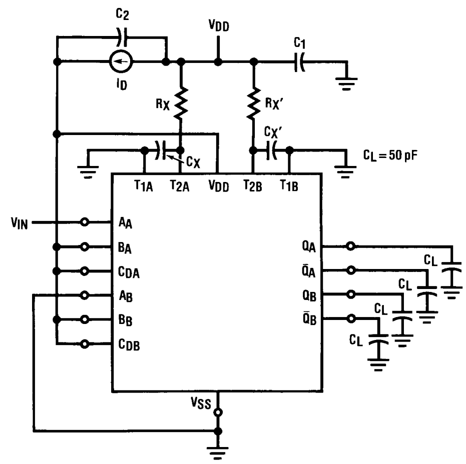
Characteristics	CD	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} PW_{OUT}, t_{WH}, t_{WL}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} PW_{OUT}, t_{WH}, t_{WL}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_{WH}, t_{WL}	PG3	PG1	PG2



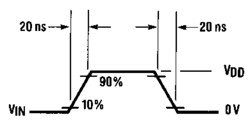
*Includes capacitance of probes, wiring, and fixture parasitic

Note: Switching test waveforms for PG1, PG2, PG3 are shown in Figure 12.

FIGURE 13. Switching Test Circuit



$R_X = R_X' = 100\ k\Omega$
$C_X = C_X' = 100\ pF$
$C_1 = C_2 = 0.1\ \mu F$



Duty Cycle = 50%

FIGURE 14. Power Dissipation Test Circuit and Waveforms