# DualPrecisionMonostable

## General Description

The CD4538B is a dual, precision monostable multivibrator with independent trigger and reset controls. The device is retriggerable and resettable, and the control inputs are inter- nally latched. Two trigger inputs are provided to allow either rising or falling edge triggering. The reset inputs are active low and prevent triggering while active. Precise control of output pulse-width has been achieved using linear CMOS techniques. The pulse duration and accuracy are deter-mined by external components RX and CX. The device does not allow the timing capacitor to discharge through the tim- ing pin on power-down condition. For this reason, no exter-nal protection resistor is required in series with the timing pin. Input protection from static discharge is provided on all pins.

## Features

- Wide supply voltage range:5.0V to 15V
- High noise immunity:0.45 $V_{CC}$ (typ.)
- Low power TTL compatibility:Fan out of 2 driving 74L or 1 driving 74LS
- New formula: $PW_{OUT}$ = RC (PW in seconds, R in Ohms, C in Farads)
- ±1.0% pulse-width variation from part to part (typ.)
- Wide pulse-width rang:1 µS to ∞
- Separate latched reset inputs
- Symmetrical output sink and source capability
- Low standby current:5 nA (typ.)@ 5 $V_{DC}$
- Pin compatible to CD4528B



DIP-16
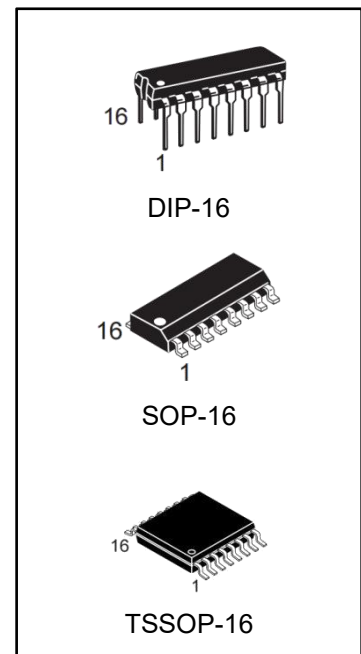
SOP-16

TSSOP-16

## Ordering Information

| DEVICE | Package Type | MARKING | Packing | Packing Qty |
|---|---|---|---|---|
| CD4538BE | DIP-16 | CD4538B | TUBE | 1000pcs/box |
| CD4538BM/TR | SOP-16 | CD4538B | REEL | 2500pcs/reel |
| CD4538BMT/TR | TSSOP-16 | CD4538B | REEL | 2500pcs/reel |

## Block and Connection Diagrams
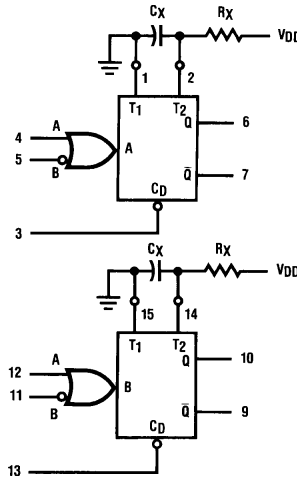


RX and CX are External Components

$V_{DD}$ － Pin 16

$V_{SS}$ － Pin 8

## Dual-In-Line Package

CD4538B



| | | |
|---|---|---|
| $T_{1A}$ | 1 | 16 $V_{DD}$ |
| $T_{2A}$ | 2 | 15 $T_{1B}$ |
| $C_{DA}$ | 3 | 14 $T_{2B}$ |
| $A_A$INPUT | 4 | 13 $C_{DB}$ |
| $B_A$INPUT | 5 | 12 $A_B$INPUT |
| $Q_A$OUT | 6 | 11 $B_B$INPUT |
| $\overline{Q}_A$OUT | 7 | 10 $Q_B$OUT |
| $V_{SS}$ | 8 | 9 $\overline{Q}_B$OUT |

Top View
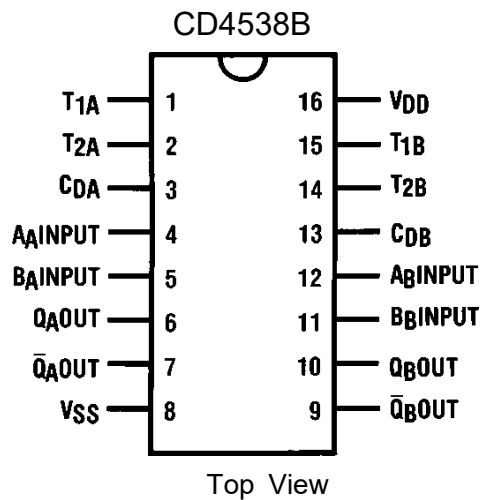
## Truth Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Clear | A | B | Q | Q |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↓ | M | W |
| H | ↑ | H | M | W |

H= High Level L

L= Low Level

↑= Transition from Low to High

↓= Transition from High to Low

M= One High Level Pulse

W= One Low Level Pulse

X= Irrelevant

## Maximum Ratings

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| VDD | DC Supply Voltage | | -0.5 | +18 | $V_{DC}$ |
| $V_{IN}$ | Input Voltage | | -0.5 | 0.5 | $V_{DC}$ |
| $T_S$ | Storage Temperature Range | | -65 | +150 | °C |
| $P_D$ | Power Dissipation | Dual-In-Line | 700 | | mW |
| | | Small Outline | 500 | | mW |
| $T_L$ | Lead Temperature | Soldering, 10 seconds | 260 | | ℃ |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for acutal device operation.
Note 2: VSS e 0V unless otherwise specified.

## Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| VDD | DC Supply Voltage | 5 | 15 | $V_{DC}$ |
| $V_{IN}$ | Input Voltage | 0 | - | $V_{DC}$ |
| $T_A$ | Operating Temperature Range | -40 | +85 | °C |

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | | -40°C | | +25°C | | | +85°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Typ | Max | Min | Max | |
| IDD | Quiescent Device Current | VDD=5V<br>VDD=10V<br>VDD=15V | VIH=VDD<br>VIL=VSS<br>All Outputs Open | | 20<br>40<br>80 | | 0.005<br>0.010<br>0.015 | 20<br>40<br>80 | | 150<br>300<br>600 | µA |
| VOL | Low Level Output Voltage | VDD=5V<br>VDD=10V<br>VDD=15V | Ilol<1 µA<br>VIH=VDD,ViL=Vss | | 0.05<br>0.05<br>0.05 | | 0<br>0<br>0 | 0.05<br>0.05<br>0.05 | | 0.05<br>0.05<br>0.05 | V |
| VOH | High Level Output Voltage | VDD=5V<br>VDD=10V<br>VDD=15V | Ilol<1 µA<br>VIH=VDD,ViL=Vss | 4.95<br>9.95<br>14.95 | | 4.95<br>9.95<br>14.95 | 5<br>10<br>15 | | 4.95<br>9.95<br>14.95 | | V |
| VIL | Low Level Input Voltage | Ilol<1 µA<br>VDD=5V,VO=0.5V of 4.5V<br>VDD=10V,VO=1.0V of 9.0V<br>VDD=15V,VO=1.5V of 13.5V | | | 1.5<br>3.0<br>4.0 | | 2.25<br>4.50<br>6.75 | 1.5<br>3.0<br>4.0 | | 1.5<br>3.0<br>4.0 | V |
| VIH | High Level Input Voltage | Ilol<1 µA<br>VDD=5V,VO=0.5V of 4.5V<br>VDD=10V,VO=1.0V of 9.0V<br>VDD=15V,VO=1.5V of 13.5V | | 3.5<br>7.0<br>11.0 | | 3.5<br>7.0<br>11.0 | 2.75<br>5.50<br>8.25 | | 3.5<br>7.0<br>11.0 | | V |
| IOL | Low Level Output Current (Note 3) | VDD=5V,VO 0.4V<br>VDD=10V,VO=0.5V<br>VDD=15V,VO=1.5V | VIH=VDD<br>VIL=VSS | 0.52<br>1.3<br>3.6 | | 0.44<br>1.1<br>3.0 | 0.88<br>2.25<br>8.8 | | 0.36<br>0.9<br>2.4 | | mA |
| IOH | High Level Output Current (Note 3) | VDD=5V,VO=4.6<br>VDD=10V,VO=9.5V<br>VDD=15V,VO=13.5V | VIL=VSS | -0.52<br>-1.3<br>-3.6 | | -0.44<br>-1.1<br>-3.0 | -0.88<br>-2.25<br>-8.8 | | -0.36<br>-0.9<br>-2.4 | | mA |
| IIN | Input Current, Pin2 or 14 | VDD=15V, VIN=0V or 15V | | | ±0.02 | | $\pm10^{-5}$ | ±0.05 | | ±0.5 | µA |
| IIN | Input Current Other Inputs | VDD=15V, VIN=0V or 15V | | | ±0.3 | | $\pm10^{-5}$ | ±0.3 | | ±1.0 | µA |

Note 3: IOH and IOL are tested one output at a time.

## AC Electrical Characteristics

* TA = 25°C, $C_L$= 50 pF, and tr= tf= 20 ns unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| tTLH, tTHL | Output Transition Time | $V_{DD}$=5V<br>$V_{DD}$=10V<br>$V_{DD}$=15V | | 100<br>50<br>40 | 200<br>100<br>80 | ns |
| tPLH, tPHL | Propagation Delay Time | Trigger Operation—<br>A orB toQ orQ̄<br>$V_{DD}$=5V<br>$V_{DD}$=10V<br>$V_{DD}$=15V<br>Reset Operation—<br>$C_D$ toQ orQ̄<br>$V_{DD}$=5V<br>$V_{DD}$=10V<br>$V_{DD}$=15V | | 300<br>150<br>100<br><br><br>250<br>125<br>95 | 600<br>300<br>220<br><br><br>500<br>250<br>190 | ns<br><br><br><br><br>ns |
| tWL, tWH | Minimum Input Pulse Width A, B, or $C_D$ | $V_{DD}$=5V<br>$V_{DD}$=10V<br>$V_{DD}$=15V | | 35<br>30<br>25 | 70<br>60<br>50 | ns |
| tRR | Minimum Retrigger Time | $V_{DD}$=5V<br>$V_{DD}$=10V<br>$V_{DD}$=15V | | <br>0<br> | 0<br>0<br>0 | ns |
| CIN | Input Capacitance | Pin 2 or 14<br>Other Inputs | | 10<br>5 | <br>7.5 | pF |
| PWOUT | Output Pulse Width (Q or Q̄) (**Note**: For Typical Distribution, see Figure 9 ) | RX=100 kΩ $V_{DD}$=5V / $V_{DD}$=10V / $V_{DD}$=15V | 208<br>211<br>216 | 226<br>230<br>235 | 244<br>248<br>254 | µS |
| | | RX=100 kΩ CX=0.1µF $V_{DD}$=5V / $V_{DD}$=10V / $V_{DD}$=15V | 8.83<br>9.02<br>9.20 | 9.60<br>9.80<br>10.00 | 10.37<br>10.59<br>10.80 | ms |
| | | RX=100kΩ CX=10.0 µF $V_{DD}$=5V / $V_{DD}$=10V / $V_{DD}$=15V | 0.87<br>0.89<br>0.91 | 0.95<br>0.97<br>0.99 | 1.03<br>1.05<br>1.07 | S |
| | Pulse Width Match between Circuits in the Same Package CX=0.1 µF, RX=100 kΩ | RX=100 kΩ CX=0.1 µF $V_{DD}$=5V / $V_{DD}$=10V / $V_{DD}$=15V | | ±1<br>±1<br>±1 | | % |
| Operating Conditions | | | | | | |
| RX<br>CX | External Timing Resistance<br>External Timing Capacitance | | 5.0<br>0 | | **<br>No Limit | kΩ<br>pF |

Note 4:AC parameters are guaranteed by DC correlated testing.

Note 5:The maximum usable resistance $R_X$ is a function of the leakage of the Capacitor $C_X$, leakage of the CD4538B, and leakage due to board layout, surface resistance, etc.
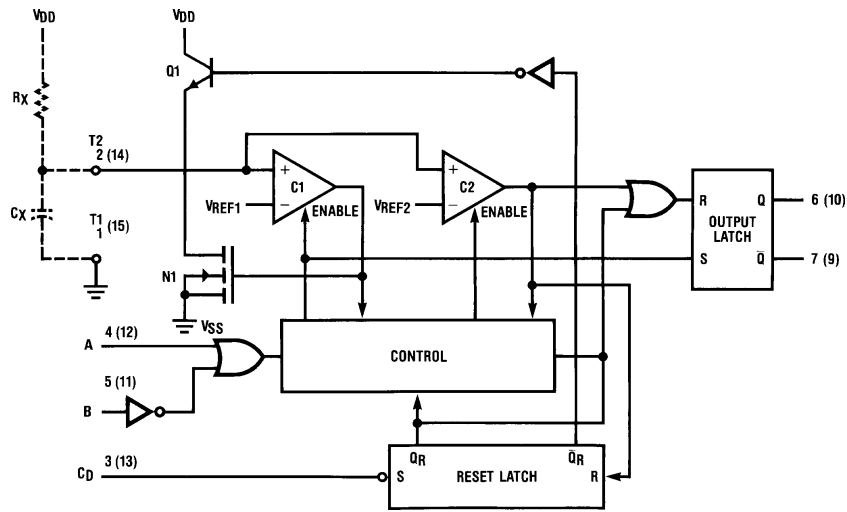
## Logic Diagram



**FIGURE 1**

## Theory of Operation



① POSITIVE EDGE TRIGGER ④ POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING)
② NEGATIVE EDGE TRIGGER ⑤ RESET (PULSE SHORTENING)
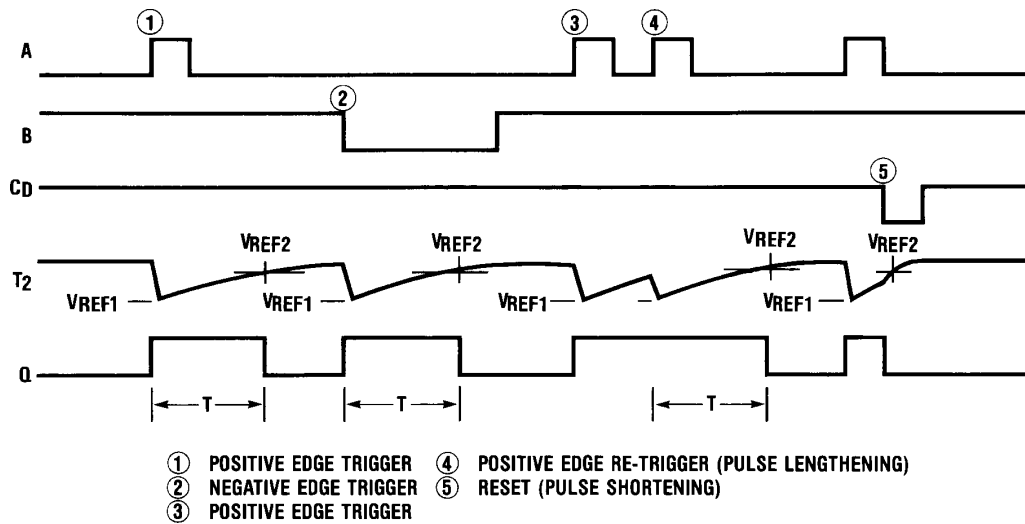③ POSITIVE EDGE TRIGGER

**FIGURE 2**

## Trigger Operation

The block diagram of the CD4538B is shown in Figure 1 , with circuit operation following.

As shown in Figures 1 and 2 , before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor $C_X$ completely charged to $V_{DD}$. When the trigger input A goes from $V_{SS}$ to $V_{DD}$ (while inputs B and $C_D$ are held to $V_{DD}$) a valid trigger is recog- nized, which turns on comparator C1 and N-Channel tran- sistor N1[①]. At the same time the output latch is set. With transistor N1 on, the capacitor $C_X$ rapidly discharges toward $V_{SS}$ until $V_{REF1}$ is reached. At this point the output of com- parator C1 changes state and transistor N1 turns off. Com- parator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor $C_X$ begins to charge through the timing resistor, RX, toward $V_{DD}$. When the voltage across $C_X$ equals $V_{REF2}$, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from $V_{DD}$ to $V_{SS}$ (while input A is at VSS and input CD is at $V_{DD}$)[②].

It should be noted that in the quiescent state $C_X$ is fully charged to $V_{DD}$, causing the current through resistor $R_X$ to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the CD4538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of $C_X$, $R_X$, or the duty cycle of the input waveform.

## Retrigger Operation

The CD4538B is retriggered if a valid trigger occurs [③] fol lowed by another valid triggerm [④] before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from $V_{REF1}$, but has not yet reached $V_{REF2}$, will cause an in crease in output pulse width T. When a valid retrigger is initiatedm[④], the voltage at T2 will again drop to $V_{REF1}$ before progressing along the RC charging curve toward $V_{DD}$. The Q output will remain high until time T, after the last valid retrigger.

## Reset Operation

The CD4538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on $C_D$ sets the reset latch and causes the capacitor to be fast charged to $V_{DD}$ by turning on transistor Q1[⑤]. When the voltage on the capacitor reaches $V_{REF2}$, the reset latch will clear and then be ready to accept another pulse. If the $C_D$ input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the $C_D$ input, the output pulse T can be made significantly shorter than the minimum pulse width specification
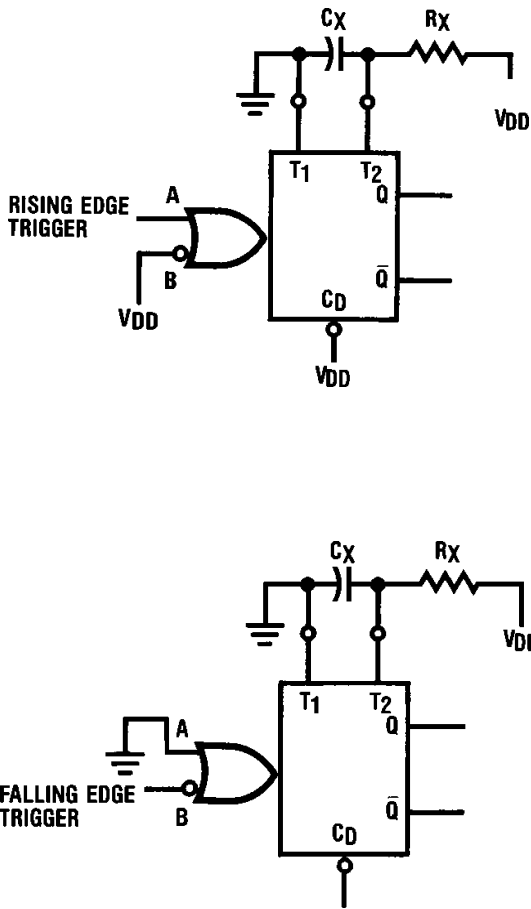
## Typical Applications



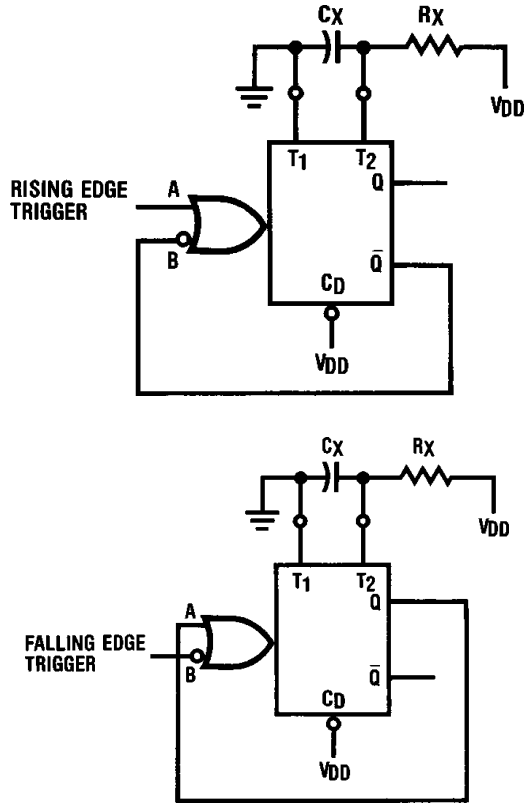FIGURE 3. Retriggerable Monostables Circuitry

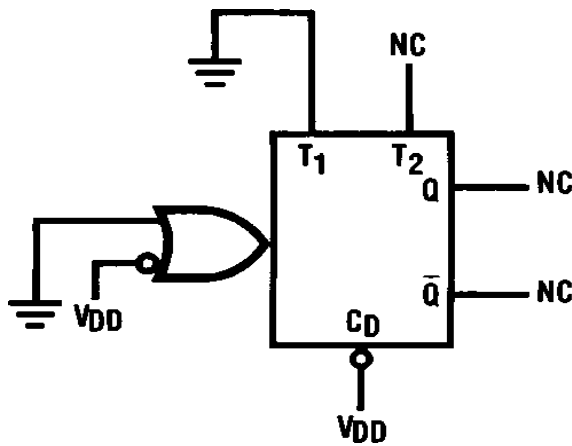FIGURE 4. Non-Retriggerable Monostables Circuitry



FIGURE 5. Connection of Unused Sections
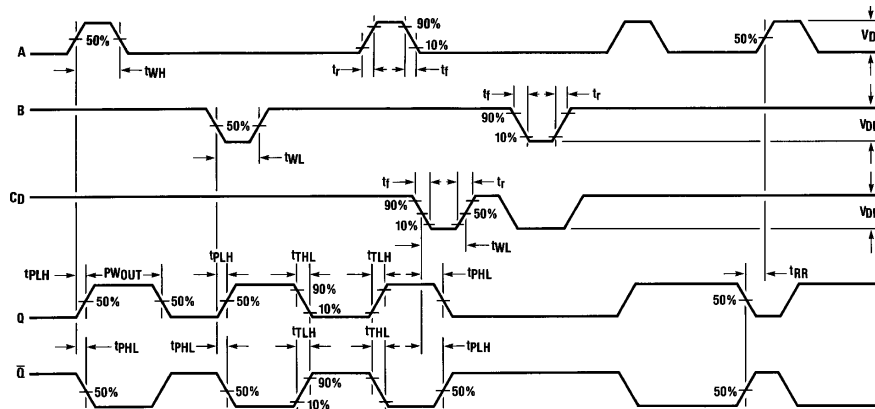
## Typical Applications



FIGURE 6. Switching Test Waveforms
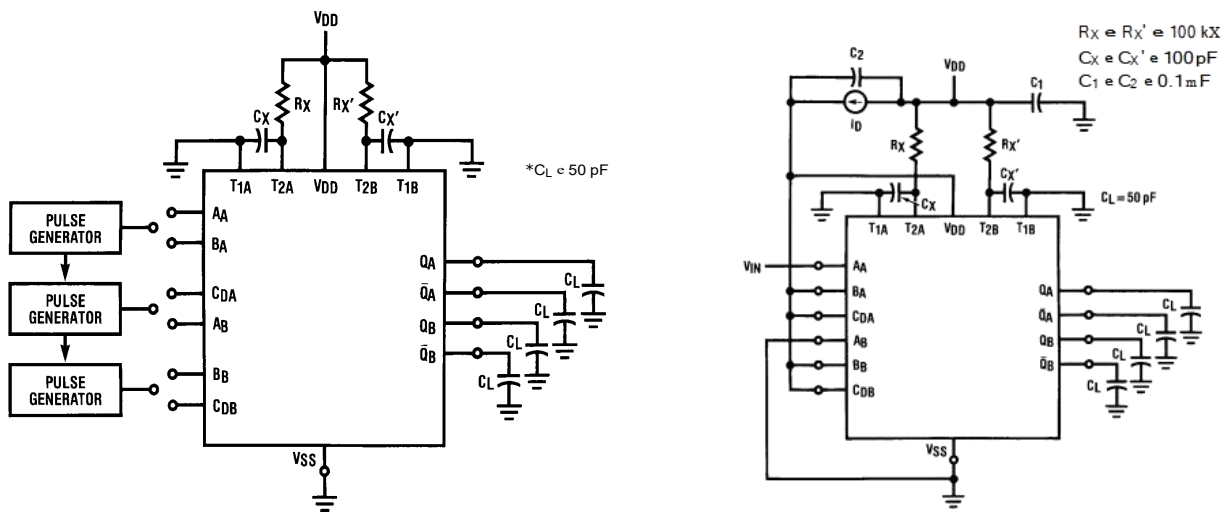


$R_X$ e $R_X'$ e $100\,k\Omega$
$C_X$ e $C_X'$ e $100\,pF$
$C_1$ e $C_2$ e $0.1\,mF$



### Input Connections

| Characteristics | CD | A | B |
|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$, $t_{TLH}$, $t_{THL}$ PW$_{OUT}$, $t_{WH}$, $t_{WL}$ | $V_{DD}$ | PG1 | $V_{DD}$ |
| $t_{PLH}$, $t_{PHL}$, $t_{TLH}$, $t_{THL}$ PW$_{OUT}$, $t_{WH}$, $t_{WL}$ | $V_{DD}$ | $V_{SS}$ | PG2 |
| $t_{PLH(R)}$, $t_{PHL(R)}$, $t_{WH}$, $t_{WL}$ | PG3 | PG1 | PG2 |

\*Includes capacitance of probes,
wiring, and fixture parasitic
Note: Switching test waveforms
for PG1, PG2, PG3 are
shown in *Figure 6*.
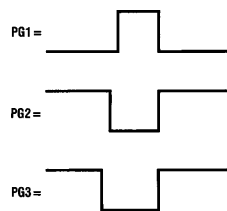


FIGURE 7. Switching Test Circuit
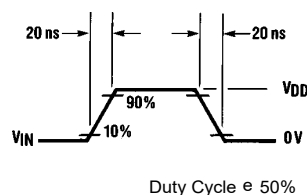
FIGURE8.Power Dissipation Test
Circuit and Waveforms

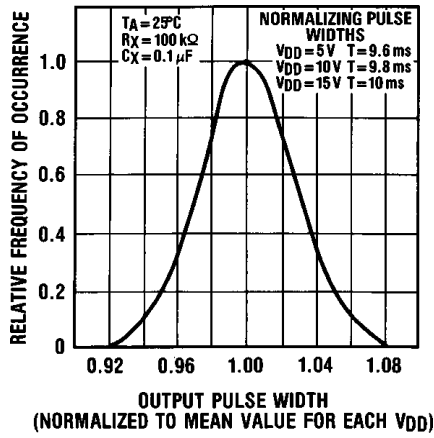## Typical Applications



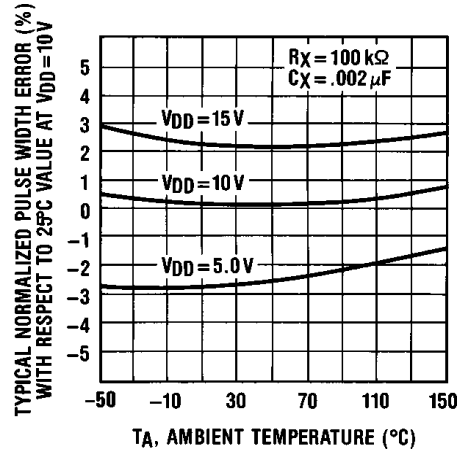FIGURE 9. Typical Normalized Distribution of Units for Output Pulse Width



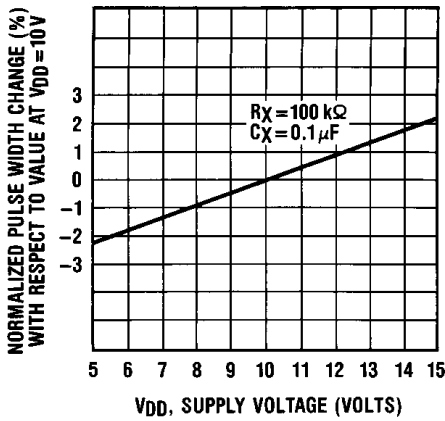FIGURE 12. Typical Pulse Width Error Versus Temperature



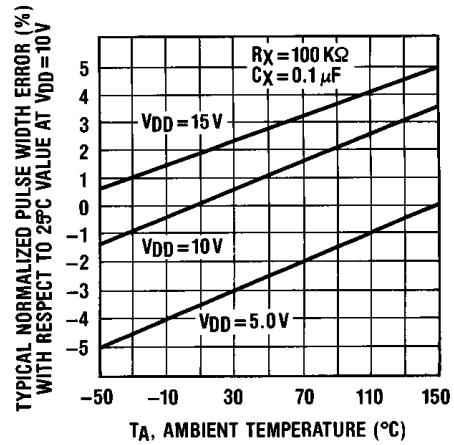FIGURE 10. Typical Pulse Width Variation as a Function of Supply Voltage $V_{DD}$



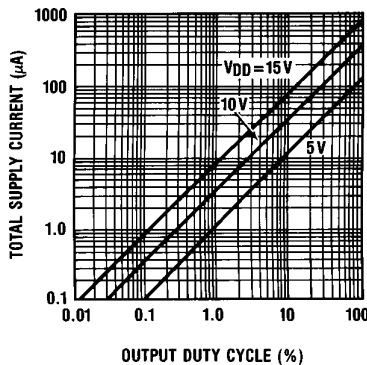FIGURE 13. Typical Pulse Width Error Versus Temperature



FIGURE 11. Typical Total Supply Current VersusFIGURE Output Duty Cycle, $R_X = 100$ kΩ, $C_L = 50$ pF, $C_X = 100$ pF, One Monostable Switching Only
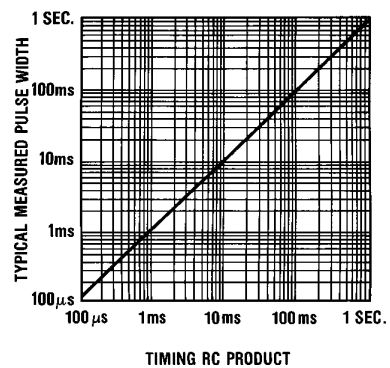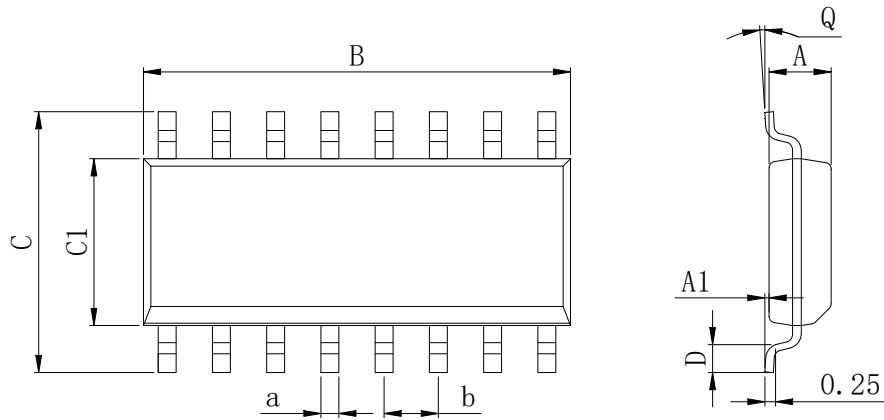


FIGURE 14. Typical Pulse Width Versus Timing RC Product

## Physical Dimensions

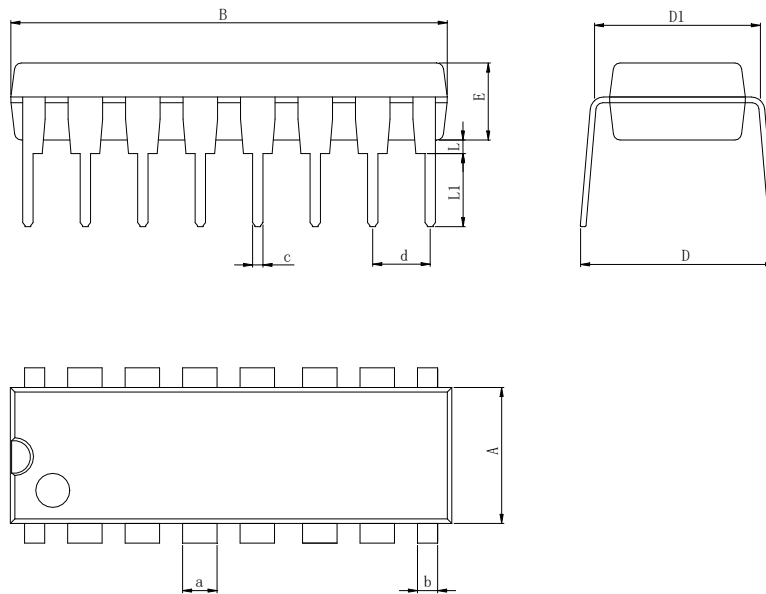SOP16



| Dimensions In Millimeters(SOP16) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Symbol： | A | A1 | B | C | C1 | D | Q | a | b |
| Min： | 1.35 | 0.05 | 9.80 | 5.80 | 3.80 | 0.40 | 0° | 0.35 | 1.27 BSC |
| Max： | 1.55 | 0.20 | 10.0 | 6.20 | 4.00 | 0.80 | 8° | 0.45 | |

DIP16



| Dimensions In Millimeters(DIP16) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Symbol： | A | B | D | D1 | E | L | L1 | a | b | c | d |
| Min： | 6.10 | 18.94 | 8.40 | 7.42 | 3.10 | 0.50 | 3.00 | 1.50 | 0.85 | 0.40 | 2.54 BSC |
| Max： | 6.68 | 19.56 | 9.00 | 7.82 | 3.55 | 0.70 | 3.60 | 1.55 | 0.90 | 0.50 | |

## Physical Dimensions

TSSOP16
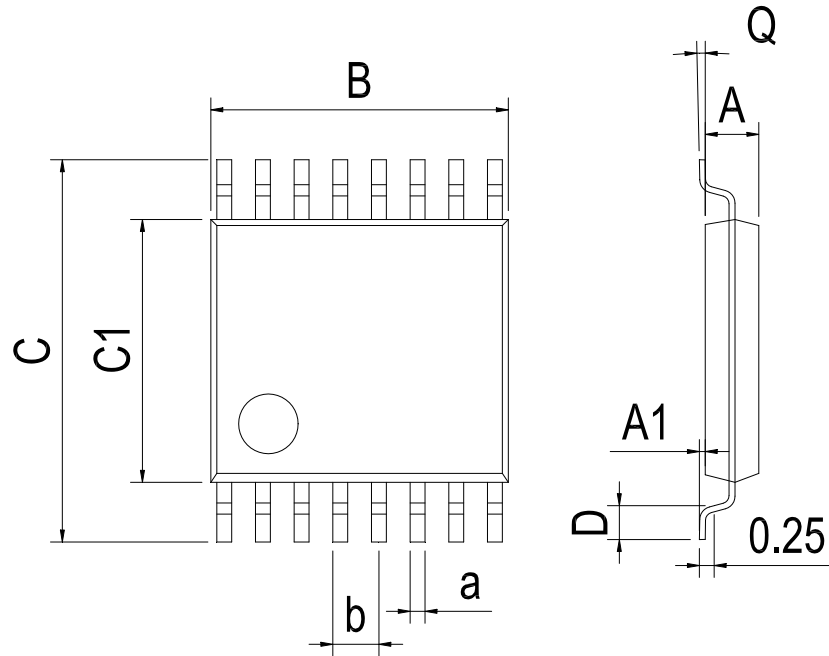


| Dimensions In Millimeters(TSSOP16) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol： | A | A1 | B | C | C1 | D | Q | a | b |
| Min： | 0.85 | 0.05 | 4.90 | 6.20 | 4.30 | 0.40 | 0° | 0.20 | 0.65 BSC |
| Max： | 0.95 | 0.20 | 5.10 | 6.60 | 4.50 | 0.80 | 8° | 0.25 | |

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AIP74HC574SA20.TR  74HC123MT/TR  74HC374M/TR  74HC123M/TR  CD40106DMT/TR  CD40106DE  CD4538BMT/TR
MC74HC73ADG  MC74HC73ADR2G  74LCX16374MTDX  74LVT74D,118  74VHCT9273FT(BJ)  JM38510/37202BEA  MM74HC374WM
74ALVCH162374PAG  74LVC1G175GS,132  74LVX74MTCX  TC7WZ74FK,LJ(CT  JM38510/30106BEA  JM38510/00204BEA
MM74HCT273WM  SN74LVC74AD  MC74HC73ADTR2G  SN74HC273DWR  M74HC374RM13TR  M74HC175B1R  M74HC174RM13TR
74ALVTH32374ZKER  74AUP1G74DC,125  74VHC374FT(BJ)  74VHCV374FT(BJ)  74VHCV574FT(BJ)  SN74LVC74ADR
SN74HC574PWR  SN74HC374AN  SN74AS574DWR