

±15kV ESD-Protected, Fail-Safe, High-Speed(10Mbps) Slew-Rate-Limited RS-485 Transceivers

General Description

The HG3485 is +/- 15kV electrostatic discharge (ESD) protected, high-speed transceiver for RS-485 communication that contain one driver and one receiver. The device features fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. This means that the receiver output will be logic-high even if all transmitters on a terminated bus are disabled. The HG3485 driver slew rate is not limited, making transmit speeds up to 10Mbps possible. All transmitter outputs and receiver inputs are protected to +/- 15kV using the Human Body Model. The transceiver typically draws 500 micron ampere of supply current when unloaded, or when fully loaded with the driver disabled. This device has a 1-unit-load receiver input impedance that allows up to 32 transceivers on the bus. The HG3485 is intended for half-duplex communications.

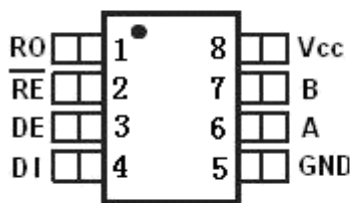
I/O ESD protection

Human Body Model: ±15kV

IEC 61000-4-2:

Contact discharge: ±12kV

Air discharge: ±15kV



DIP8/SOP8
HG3485 Pin figure

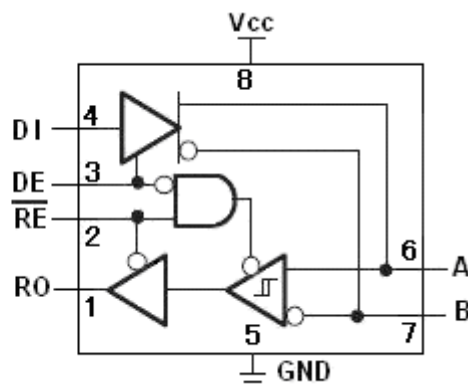
Features

- True Fail-Safe Receiver While Maintaining EIA/TIA-485 Compatibility
- Low Quiescent Supply Current: 500uA
- Allow Up to 32 Transceivers on the Bus
- 1nA Low-Current Shutdown Mode

Applications

- RS-485 Communications
- Level Translators
- Motor Controller
- Industrial Control Local Area Networks
- Energy Meter Networks
- Power Inverters
- Building Automation Networks
- Telecommunications Equipment

PIN Configuration



Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
HG3485EIN	DIP8	HG3485	TUBE	2000/box
HG3485EIM/TR	SOP8	HG3485	REEL	2500/reel

Pin Description

PIN	NAME	FUNCTION
1	RO	Receiver Output. When RE is low and if $A - B \geq -50\text{mV}$, RO will be high; if $A - B \leq -200\text{mV}$, RO will be low.
2	\overline{RE}	Receiver Output Enable. Drive \overline{RE} low to enable RO; RO is high impedance when \overline{RE} is high. Drive \overline{RE} high and DE low to enter low-power shutdown mode.
3	DE	Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive \overline{RE} high and DE low to enter low-power shutdown mode.
4	DI	Driver Input. With DE high, a low on DI forces non-inverting output low and inverting output high. Similarly, a high on DI forces non-inverting output high and inverting output low.
5	GND	Ground
6	A	Non-inverting Receiver Input and Non-inverting Driver Output.
7	B	Inverting Receiver Input and Inverting Driver Output.
8	VCC	Positive Supply $3.0\text{V} \leq VCC \leq 3.6\text{V}$.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	NUM	UNITS
Supply Voltage (VCC)	VCC	+6.5	V
Control Input Voltage (\overline{RE} , DE)	\overline{RE} , DE	-0.3 to VCC+0.3	V
Driver Input Voltage (DI)	DI	-0.3 to VCC+0.3	V
Driver Output Voltage (A, B)	A, B	± 13	V
Receiver Input Voltage (A, B)	A, B	± 13	V
Receiver Output Voltage (RO)	RO	-0.3~VCC+0.3	V
Continuous Power Dissipation	SOP8	471	mW
Operating Temperature Ranges		-40~+85	°C
Storage Temperature Range		-65~+150	°C
Lead Temperature (soldering, 10s)		300	°C

DC ELECTRICAL CHARACTERISTICS

(VCC = +3.3V ± 5%, TA = TMIN to TMAX, unless otherwise noted. Typical values are at VCC = +3.3V and TA = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Differential Driver Output (No Load)	VOD1	Figure 1	2.0			V
Differential Driver Output	VOD2	Figure 1, R = 27Ω	1.5			V
Change-in-Magnitude of Differential Output Voltage (Note 2)	ΔVOD	Figure 1, R = 27Ω			0.2	V
Driver Common-Mode Output Voltage	VOC	Figure 1, R = 27Ω	1		3	V

Change-in-Magnitude of Common-Mode Voltage (Note 2)	ΔV_{OC}	Figure 1, $R = 27\Omega$			0.2	V	
Input High Voltage	V_{IH1}	DE, DI, \overline{RE}	2.0			V	
Input Low Voltage	V_{IL1}	DE, DI, \overline{RE}			0.8	V	
DI Input Hysteresis	V_{HYS}			100		mV	
Input Current (A and B)	I_{IN1}	DE = GND, VCC = GND or 3.3V	$V_{IN} = 12V$		500	μA	
			$V_{IN} = -7V$	-500			
Driver Short-Circuit Output Current (Note 3)	I_{OSD}	$-7V \leq V_{OUT} \leq VCC$	-250			mA	
		$0V \leq V_{OUT} \leq 12V$			250		
		$0V \leq V_{OUT} \leq VCC$	± 25				
RECEIVER							
Receiver Differential Threshold Voltage	V_{TH}	$-7V \leq V_{CM} \leq 12V$	-200	-110	-50	mV	
Receiver Input Hysteresis	ΔV_{TH}			30		mV	
Receiver Output High Voltage	V_{OH}	$I_O = -4mA, V_{ID} = -50mV$	$V_{CC} - 0.4$			V	
Receiver Output Low Voltage	V_{OL}	$I_O = 4mA, V_{ID} = -200mV$			0.4	V	
Three-State Output Current at Receiver	I_{OZR}	$0.4V \leq V_O \leq 2.4V$			± 1	μA	
Receiver Input Resistance	R_{IN}	$-7V \leq V_{CM} \leq 12V$	12			k Ω	
Receiver Output Short-Circuit Current	I_{OSR}	$0V \leq V_{RO} \leq VCC$	± 7		± 95	mA	
SUPPLY CURRENT							
Supply Current	I_{CC}	No load, $\overline{RE} =$ DI = GND or VCC	DE = VCC		500	900	μA
			DE = GND		400	600	μA
Supply Current in Shutdown Mode	I_{SHDN}	DE = GND, $V_{\overline{RE}} = VCC$			0.001	1	μA
ESD Protection for A, B		Human Body Model			± 15		kV

SWITCHING CHARACTERISTICS

(VCC = +3.3V \pm 5%, TA = TMIN to TMAX, unless otherwise noted. Typical values are at VCC = +3.3V and TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{DPLH}	Figure 3 and 5, $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$		20	40	ns
	t_{DPHL}			20	40	
Driver Output Skew $t_{DPLH} - t_{DPHL}$	t_{DSKEW}	Figure 3 and 5, $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$		-3	± 10	ns
Driver Rise or Fall Time	t_{DR}, t_{DF}	Figure 3 and 5, $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$		12	25	ns

Maximum Data Rate	f_{MAX}		10			Mbps
Driver Enable to Output High	t_{DZH}	Figure 4 and 6, $C_L=100pF$, S2 closed			150	ns
Driver Enable to Output Low	t_{DZL}	Figure 4 and 6, $C_L=100pF$, S1 closed			150	ns
Driver Disable Time from Low	t_{DLZ}	Figure 4 and 6, $C_L=15pF$, S1 closed			100	ns
Driver Disable Time from High	t_{DHZ}	Figure 4 and 6, $C_L=15pF$, S2 closed			100	ns
Receiver Input to Output	t_{RPLH} , t_{RPHL}	Figure 9, $ V_{ID} \cong 2.0V$ rise and fall time of $V_{ID} \cong 15ns$		50		ns
$ t_{RPLH} - t_{RPHL} $ Differential Receiver Skew	t_{RSKD}	Figure 9, $ V_{ID} \cong 2.0V$ rise and fall time of $V_{ID} \cong 15ns$		0	± 10	ns
Receiver Enable to Output Low	t_{RZL}	Figure 2, $C_L=100pF$, S1 closed		20	50	ns
Receiver Enable to Output High	t_{RHZ}	Figure 2, $C_L=100pF$, S2 closed		20	50	ns
Receiver Disable Time from Low	t_{RLZ}	Figure 2, $C_L=100pF$, S1 closed		20	50	ns
Receiver Disable Time from High	t_{RHZ}	Figure 2, $C_L=100pF$, S2 closed		20	50	ns
Time to Shutdown	t_{SHDN}	(Note 4)	50	200	600	ns
Driver Enable from Shutdown-to-Output High	$t_{DZH(SHDN)}$	Figure 4, $C_L=15pF$, S2 closed			250	ns
Driver Enable from Shutdown-to-Output Low	$t_{DZL(SHDN)}$	Figure 4, $C_L=15pF$, S1 closed			250	ns
Receiver Enable from Shutdown-to-Output High	$t_{RZH(SHDN)}$	Figure 2, $C_L=100pF$, S2 closed			3500	ns
Receiver Enable from Shutdown-to-Output Low	$t_{RZL(SHDN)}$	Figure 2, $C_L=100pF$, S1 closed			3500	ns

Note 1: All currents into the device are positive; all currents out of the device are negative. All voltages are referred to device ground unless otherwise noted.

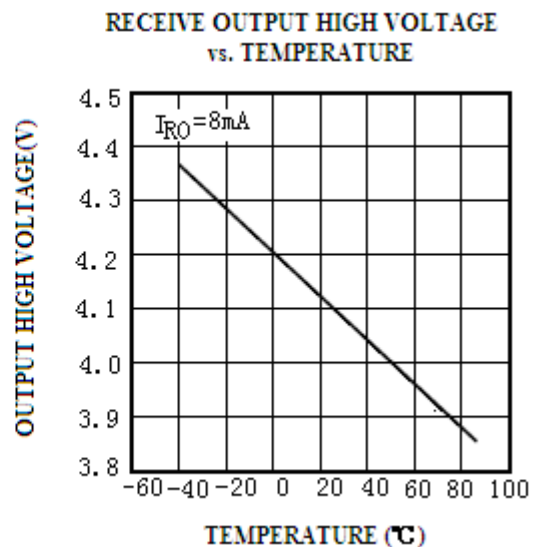
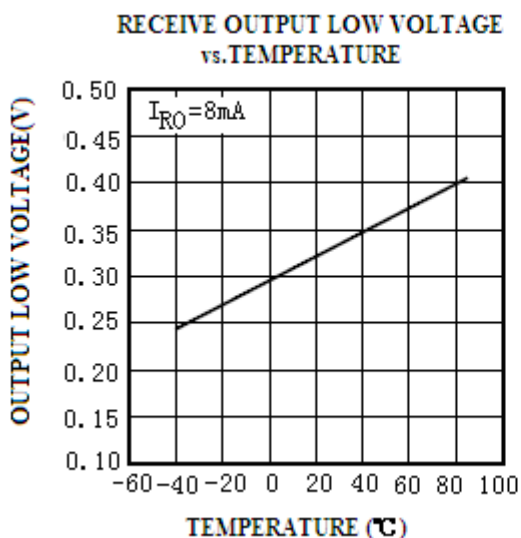
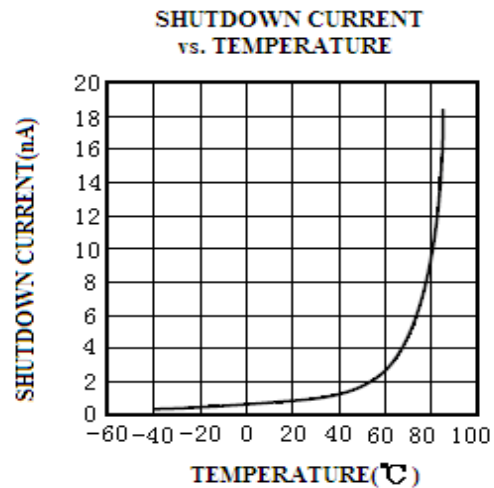
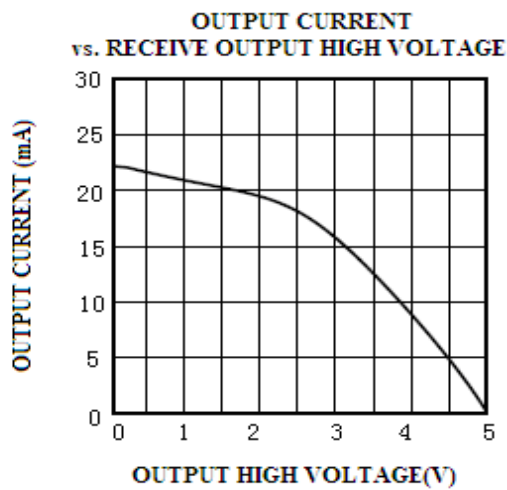
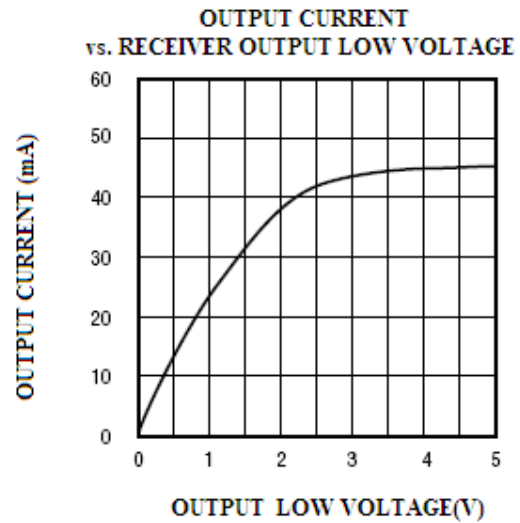
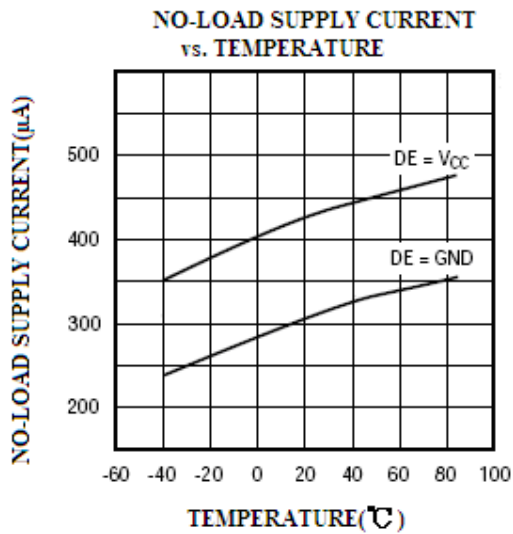
Note 2: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC} , respectively, when the DI input changes state.

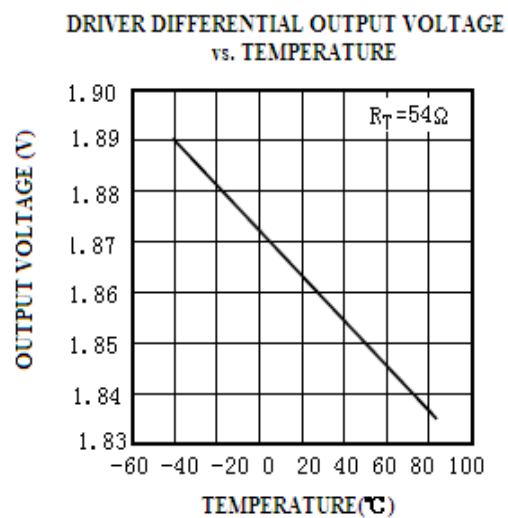
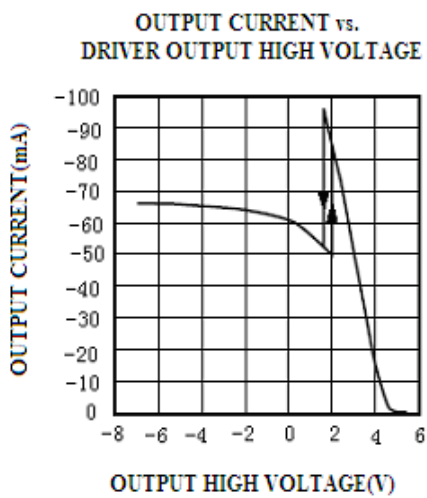
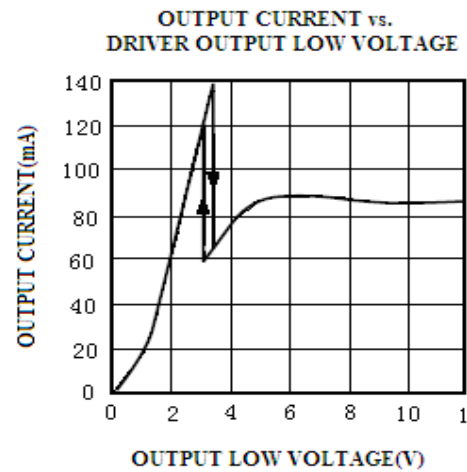
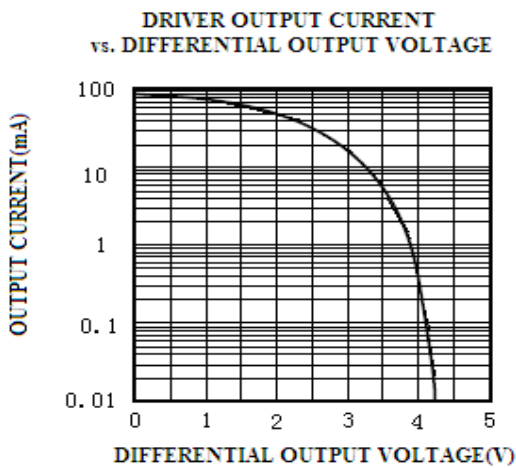
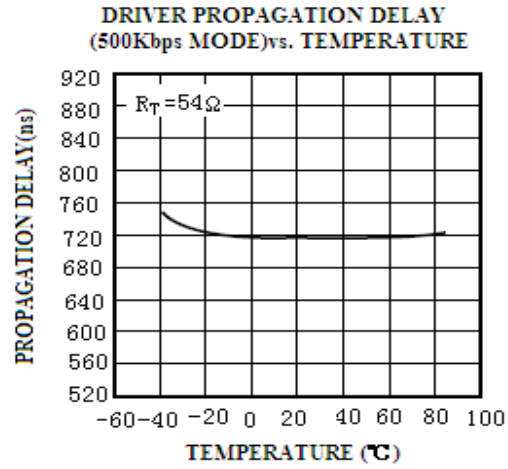
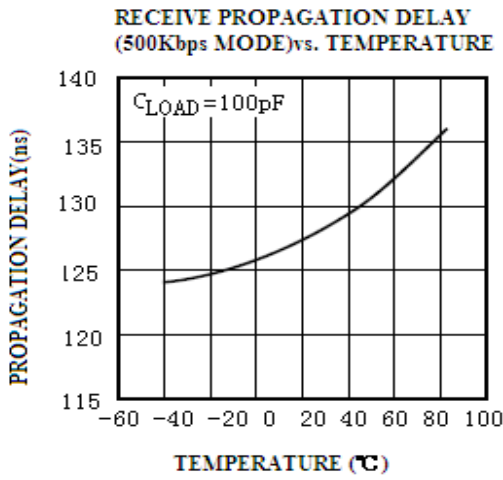
Note 3: Maximum current level applies to peak current just prior to fold-back current limiting; minimum current level applies during current limiting.

Note 4: The device is put into shutdown by bringing \overline{RE} high and DE low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 600ns, the device is guaranteed to have entered shutdown.

Typical Operating Characteristics

(VCC = +3.3V, TA = +25°C, unless otherwise noted.)





Function Tables

TRANSMITTING				
INPUTS			OUTPUTS	
\overline{RE}	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	Shutdown	
RECEIVING				
INPUTS			OUTPUTS	
\overline{RE}	DE	A - B	RO	
0	X	$\cong -0.2V$	1	
0	X	$\cong -0.2V$	0	
0	X	Open/shorted	1	
1	1	X	High-Z	
1	0	X	Shutdown	

X = Don't care
Shutdown mode, driver and receiver outputs high impedance

Test Circuits

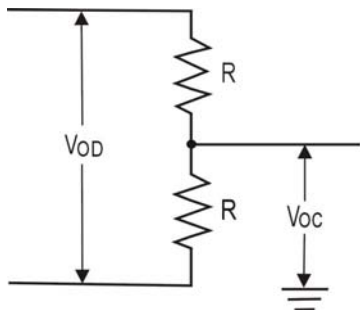


Figure1. Driver DC Test Load

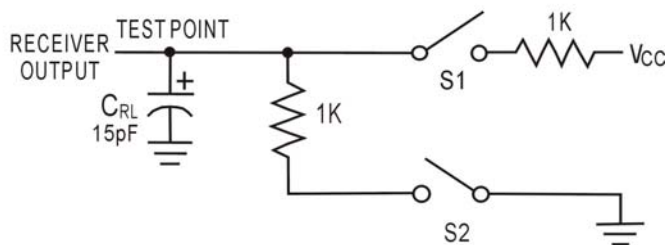


Figure 2. Receiver Enable/Disable Timing Test Load

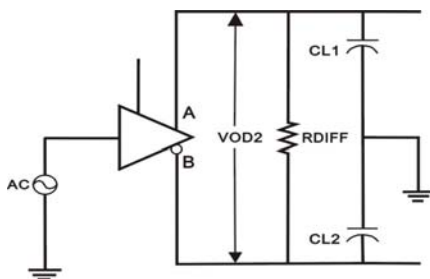


Figure3. Driver Timing Test Load

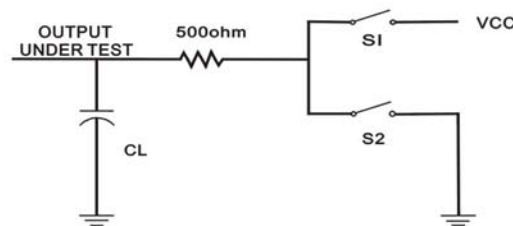


Figure 4. Driver Enable/Disable Timing Test Load

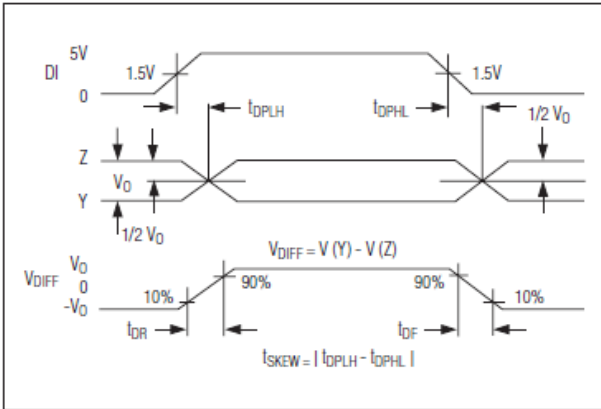


Figure 5. Driver Propagation Delays

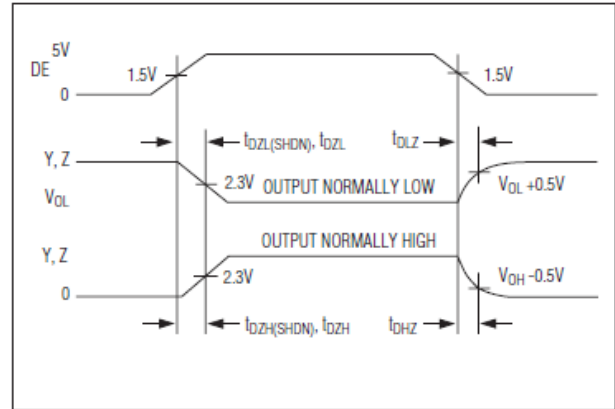


Figure 6. Driver Enable and Disable Times

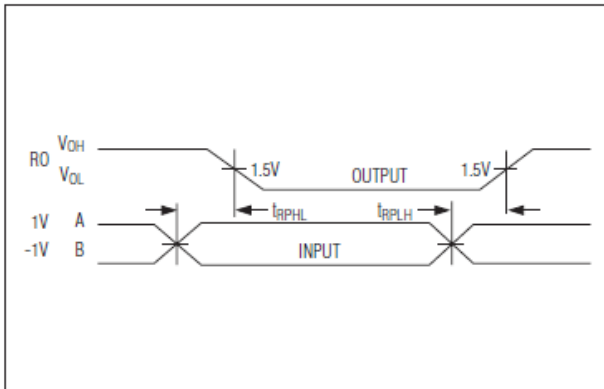


Figure 7. Receiver Propagation Delays

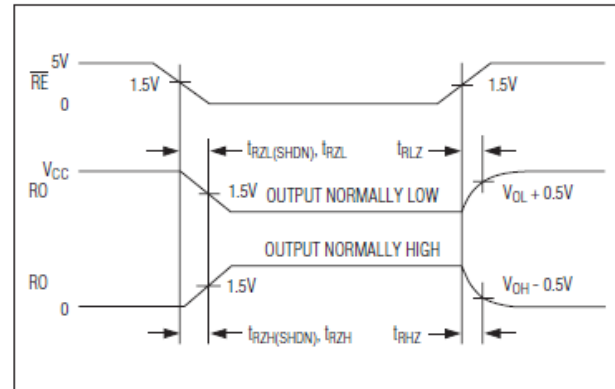


Figure 8. Receiver Enable and Disable Times

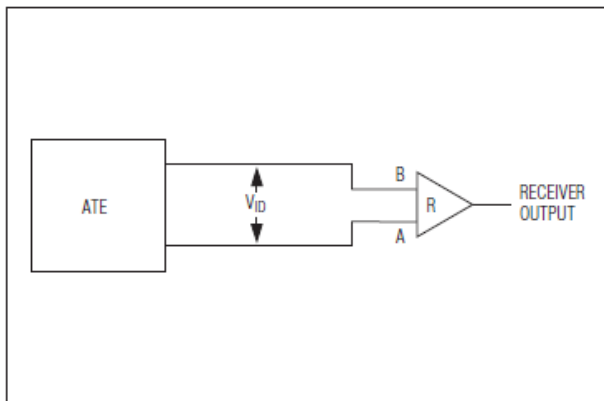


Figure 9. Receiver Propagation Delay Test Circuit

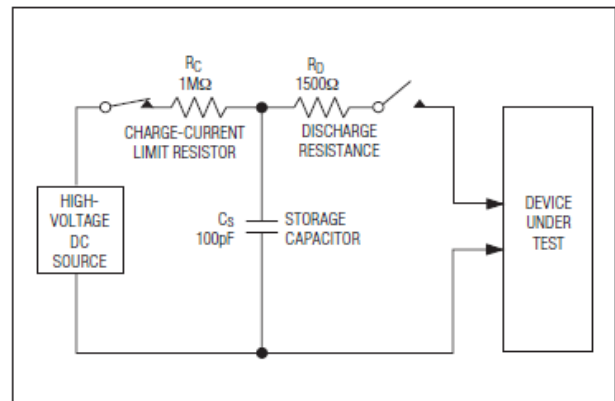


Figure 10a. Human Body ESD Test Model

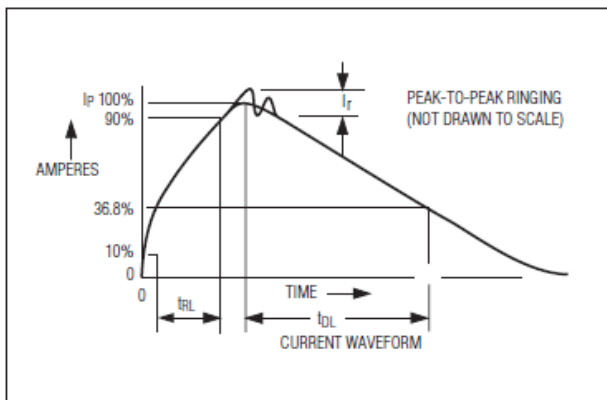


Figure 10b. Human Body Current Waveform

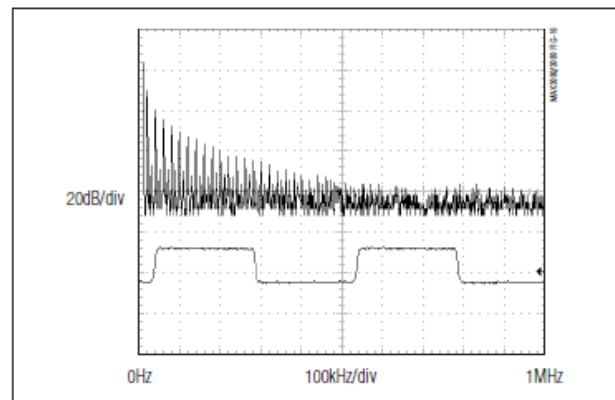


Figure 11. Driver Output Waveform and FFT Plot

Detailed Description

The HG3485 high - speed transceiver for RS-485 communication contains one driver and one receiver. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the Fail-Safe section). The HG3485 driver slew rate is not limited, making transmit speeds up to 10Mbps possible. The HG3485 is a half-duplex transceiver. The voltage operates from a single +3.3V supply. Drivers are output short-circuit current limited. Thermal shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal shutdown circuitry places the driver outputs into a high impedance state.

Fail-Safe

The HG3485 guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver threshold between -50mV and -200mV. If the input voltage of differential receiver (A-B) is greater than or equal to -50mV, RO is logic high. If A-B is less than or equal to -200mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the receiver differential input voltage is pulled to 0V by the termination. With the receiver threshold of the HG3485, this results in a logic high with a

50mV minimum noise margin. Unlike previous fail-safe devices, the -50mV to -200mV threshold complies with the +/-200mV EIA/TIA-485 standard.

ESD Protection

As with HG3485, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver output and receiver input of the HG3485 has extra protection against static electricity. The ESD-protected pins are tested with reference to the ground pin in a powered-down condition. They are tested to +/- 15kV using the Human Body Model.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 10a shows the Human Body Model, and Figure 10b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly. All pins require this protection,

not just RS-485 inputs and outputs.

Applications Information

32 Transceivers on the Bus

The standard RS-485 receiver input impedance is $12k\Omega$ (one-unit load), and the standard driver can drive up to 32 unit loads. The HG3485 has a one-unit-load receiver input impedance ($12k\Omega$), allowing up to 256 transceivers to be connected in parallel on one communication line. Any combination of this device and/or other RS-485 transceivers with a total of 32 unit loads or less can be connected to the line.

Reduced EMI and Reflections

The HG3485, driver slew rate is not limited, High-frequency harmonic components with large amplitudes are evident. transmitting under the same conditions. Figure 11 shows driver output waveform and its Fourier analysis of a 20kHz signal transmitted by a HG3485, In general, a transmitter's rise time relates directly to the length of an unterminated stub, which can be driven with only minor waveform reflections. The following equation expresses this relationship conservatively:

$$\text{Length} = t_{\text{RISE}} / (10 \times 1.5\text{ns/ft})$$

where t_{RISE} is the transmitter's rise time. For example, the HG3485's rise time is typically 14ns, which results in excellent waveforms with a stub length up to 1 feet. A system can work well with longer unterminated stubs, even with severe reflections, if the waveform settles out before the UART samples them.

Low-Power Shutdown Mode

When both the driver and receiver are disabled (DE low and \overline{RE} high) the device is in shutdown mode. If the enable inputs are in this state for less than 60 ns, the device does not

enter shutdown mode. This guards against inadvertently entering shutdown mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in shutdown mode. In this low-power shutdown mode, most internal circuitry is powered down except over temperature protection circuit, and the supply current is typically 40 micron ampere. When either the driver or the receiver is re-enabled, the internal circuitry becomes active. If only the driver is re-enabled (DE changed to high) the driver outputs are driven according to the DI input after the enable times given by $t_{\text{PZH}}(\text{SHDN})$ and $t_{\text{PZL}}(\text{SHDN})$ in the driver switching characteristics. If the DI input is open when the driver is enabled, the driver outputs defaults to A high and B low, in accordance with the driver failsafe feature. If only the receiver is re-enabled (\overline{RE} changed to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable time given by $t_{\text{PZH}}(\text{SHDN})$ and $t_{\text{PZL}}(\text{SHDN})$ in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section. If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the DI input. Note that the state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a fold back current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature becomes excessive.

110kHz into 120Ω loads.

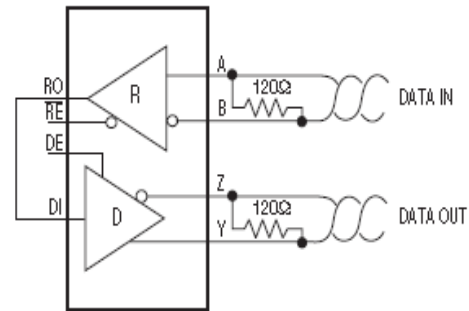


Figure 12. Line Repeater for HG3485

Line Length vs Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. For line lengths greater than 4000 feet, use the repeater application

shows in Figure 12. Figure 13 shows the system differential voltage for the parts driving 4000 feet of 26AWG twistedpair wire at

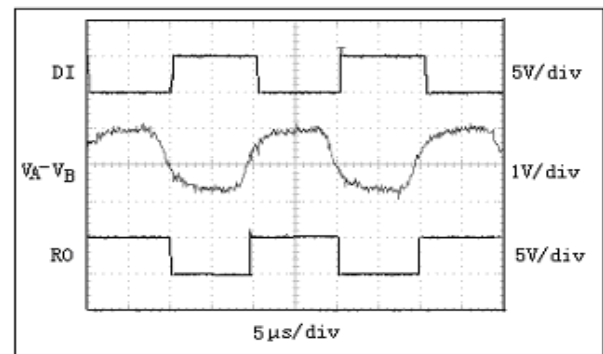


Figure 13. HG3485 System Differential Voltage at 50kHz
Driving 4000ft of Cable

Applications

The HG3485 transceiver is designed for bidirectional data communications on multipoint bus transmission lines. Figures 14 shows typical network applications circuits. To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited HG3485 is more tolerant of imperfect termination.

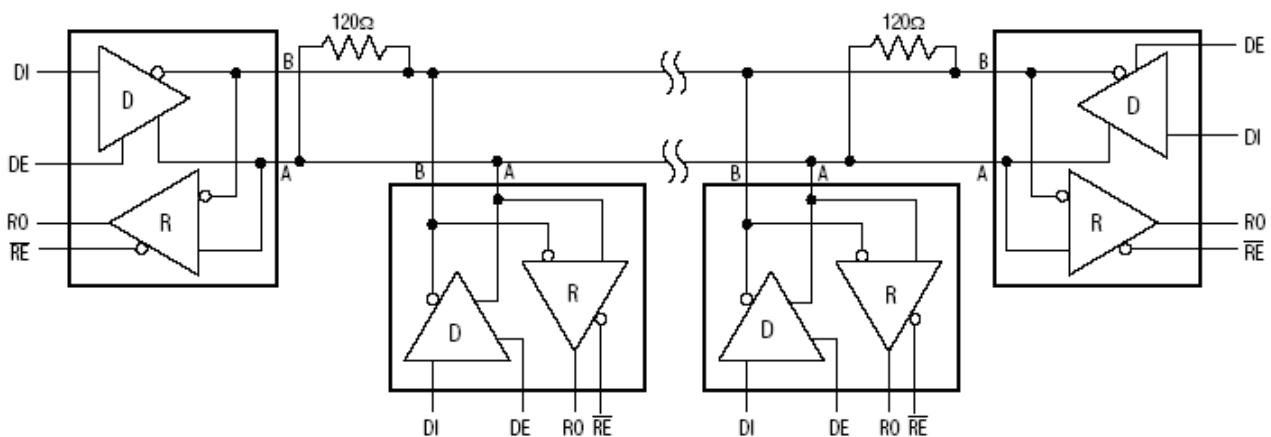


Figure 14. HG3485 Pin Configuration and Typical Half-Duplex Operating C circuit

Package

SOP8

Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	1.225	1.570	D	0.400	0.950
A1	0.100	0.250	Q	0°	8°
B	4.800	5.100	a	0.420 TYP	
C	5.800	6.250	b	1.270 TYP	
C1	3.800	4.000			

DIP8

Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	6.100	6.680	L1	3.000	3.600
B	9.000	9.500	a	1.524 TYP	
D	8.400	9.000	b	0.889 TYP	
D1	7.420	7.820	c	0.457 TYP	
E	3.100	3.550	d	2.540 TYP	
L	0.500	0.700			

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[ISL8487EIB](#) [ISL8489EIB](#) [ISL8491IP](#) [ADM489AN](#) [CA-IF4820HM](#) [CS48505M](#) [CS485S](#) [CS817x22HS](#) [MAX485ESA-MS](#) [MAX3085](#)
[ADM3485EARZ](#) [SP3485EEN](#) [TP3485ES8](#) [MAX3485ESA](#) [ST3485EBDR](#) [ADM485ARZ](#) [CA-IF4820HD](#) [CA-IF1042S-Q1](#) [CA-IF1021D-Q1](#)
[CS48520D](#) [SN65HVD78EIMM/TR](#) [HGX3085ECMM/TR](#) [SP3085EIMM/TR](#) [HGX3085EIMM/TR](#) [SN65HVD72EIMM/TR](#) [HGX485EIN](#)
[RS1905XK](#) [SIT1044QTK](#) [THVD1420DR](#) [MAX3490EESA+T](#) [UM3483EESA](#) [HD588L](#) [HD568N](#) [HD688ADR](#) [CA-IS3080WX](#) [CA-](#)
[IS3086WX](#) [CS817x20HS](#) [CA-IF1044S-Q1](#) [CA-IF4820FS](#) [CA-IF4850HS](#) [GM3490E](#)