3-Pin Microprocessor Reset Monitors

The HG809 and HG810 are cost–effective system supervisor circuits designed to monitor V_{CC} in digital systems and provide a reset signal to the host processor when necessary. No external components are required.

The reset output is driven active within 20 µsec of V_{CC} falling through the reset voltage threshold. Reset is maintained active for a minimum of 140msec after V_{CC} rises above the reset threshold. The HG810 has an active–high RESET output while the HG809 has an active–low $\overline{\text{RESET}}$ output. The output of the HG809 is guaranteed valid down to V_{CC} = 1V. Both devices are available in a SOT–23 package.

The HG809/810 are optimized to reject fast transient glitches on the V_{CC} line. Low supply current of 17µA (V_{CC} = 3.3V) makes these devices suitable for battery powered applications.

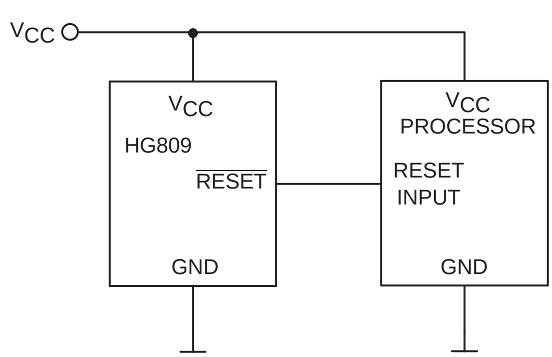
Features

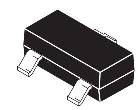
- Precision V_{CC} Monitor for 3.0V, 3.3V, and 5.0V Supplies
- 140msec Guaranteed Minimum $\overline{\text{RESET}}$, RESET Output Duration
- $\overline{\text{RESET}}$ Output Guaranteed to V_{CC} = 1.0V (HG809)
- Low 17µA Supply Current
- V_{CC} Transient Immunity
- Small SOT–23 Package
- No External Components
- Wide Operating Temperature: –40°C to 85°C

Typical Applications

- Computers
- Embedded Systems
- Battery Powered Equipment
- Critical µP Power Supply Monitoring

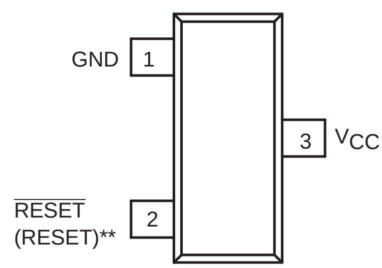
TYPICAL APPLICATION DIAGRAM





SOT–23
(TO–236)
CASE 318

PIN CONFIGURATION
(Top View)



SOT–23*

NOTE: *SOT–23 is equivalent to JEDEC (TO–236)
** $\overline{\text{RESET}}$ is for HG809
** RESET is for HG810

NOTE: The "x" denotes a suffix for V_{CC} threshold – see table below

Suffix	Reset V_{CC} Threshold (V)
L	4.63
M	4.38
J*	4.00
T	3.08
S	2.93
R	2.63

NOTE: *J version is available for HG809 only

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
	Supply Voltage (V_{CC} to GND)	6.0	V
	$\overline{RESET}$, RESET	–0.3 to (V_{CC} + 0.3)	V
	Input Current, V_{CC}	20	mA
	Output Current, $\overline{RESET}$, RESET	20	mA
	dV/dt (V_{CC})	100	V/µsec
P_D	Power Dissipation ($T_A \leq 70°C$) SOT–23 (derate 4mW/°C above +70°C)	230	mW
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_{sol}	Lead Temperature (Soldering, 10 Seconds)	+260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

ELECTRICAL CHARACTERISTICS (V_{CC} = Full Range, T_A = –40°C to +85°C unless otherwise noted. typical values are at T_A = +25C, V_{CC} = 5V for L/M/J, 3.3V for T/S, 3.0V for R) (Note NO TAG)

Symbol	Characteristic	Min	Typ	Max	Unit
	V_{CC} Range T_A = 0°C to +70°C T_A = –40°C to +85°C	 1.0 1.2	 — —	 5.5 5.5	V
I_{CC}	Supply Current HG8xxL/M/J: V_{CC} < 5.5V HG8xxR/S/T: V_{CC} < 3.6V	 — —	 24 17	 60 50	µA
V_{TH}	Reset Threshold (Note NO TAG) HG8xxL: T_A = 25°C T_A = –40°C to +85°C HG8xxM: T_A = 25°C T_A = –40°C to +85°C HG809J: T_A = 25°C T_A = –40°C to +85°C HG8xxT: T_A = 25°C T_A = –40°C to +85°C HG8xxS: T_A = 25°C T_A = –40°C to +85°C HG8xxR: T_A = 25°C T_A = –40°C to +85°C	 4.56 4.50 4.31 4.25 3.93 3.89 3.04 3.00 2.89 2.85 2.59 2.55	 4.63 — 4.38 — 4.00 — 3.08 — 2.93 — 2.63 —	 4.70 4.75 4.45 4.50 4.06 4.10 3.11 3.15 2.96 3.00 2.66 2.70	V
	Reset Threshold Temperature Coefficient	—	30	—	ppm/°C
	V_{CC} to Reset Delay V_{CC} = V_{TH} to (V_{TH} – 100mV)	—	20	—	µsec
	Reset Active Timeout Period	140	240	560	msec
V_{OL}	$\overline{RESET}$ Output Voltage Low (HG809) HG809R/S/T: V_{CC} = V_{TH} min, I_{SINK} = 1.2mA HG809L/M/J: V_{CC} = V_{TH} min, I_{SINK} = 3.2mA V_{CC} > 1.0V, I_{SINK} = 50µA	 — — —	 — — —	 0.3 0.4 0.3	V
V_{OH}	$\overline{RESET}$ Output Voltage High (HG809) HG809R/S/T: V_{CC} > V_{TH} max, I_{SOURCE} = 500µA HG809L/M/J: V_{CC} > V_{TH} max, I_{SOURCE} = 800µA	 0.8 V_{CC} V_{CC} – 1.5	 — —	 — —	V
V_{OL}	RESET Output Voltage Low (HG810) HG810R/S/T: V_{CC} = V_{TH} max, I_{SINK} = 1.2mA HG810L/M/J: V_{CC} = V_{TH} max, I_{SINK} = 3.2mA	 — —	 — —	 0.3 0.4	V
V_{OH}	RESET Output Voltage High (HG810) 1.8 < V_{CC} < V_{TH} min, I_{SOURCE} = 150µA	 0.8 V_{CC}	 —	 —	V

1. Production testing done at T_A = 25°C, over temperature limits guaranteed by design.

PIN DESCRIPTION

Pin No.	Symbol	Description
1	GND	Ground
2	$\overline{RESET}$ (HG809)	$\overline{RESET}$ output remains low while V_{CC} is below the reset voltage threshold, and for 240msec (typ.) after V_{CC} rises above reset threshold
2	RESET (HG810)	RESET output remains high while V_{CC} is below the reset voltage threshold, and for 240msec (typ.) after V_{CC} rises above reset threshold
3	V_{CC}	Supply Voltage (typ.)

APPLICATIONS INFORMATION

V_{CC} Transient Rejection

The HG809/810 provides accurate V_{CC} monitoring and reset timing during power–up, power–down, and brownout/sag conditions, and rejects negative–going transients (glitches) on the power supply line. Figure 1 shows the maximum transient duration vs. maximum negative excursion (overdrive) for glitch rejection. Any combination of duration and overdrive which lies **under** the curve will **not** generate a reset signal. Combinations above the curve are detected as a brownout or power–down. Transient immunity can be improved by adding a capacitor in close proximity to the V_{CC} pin of the HG809/810.

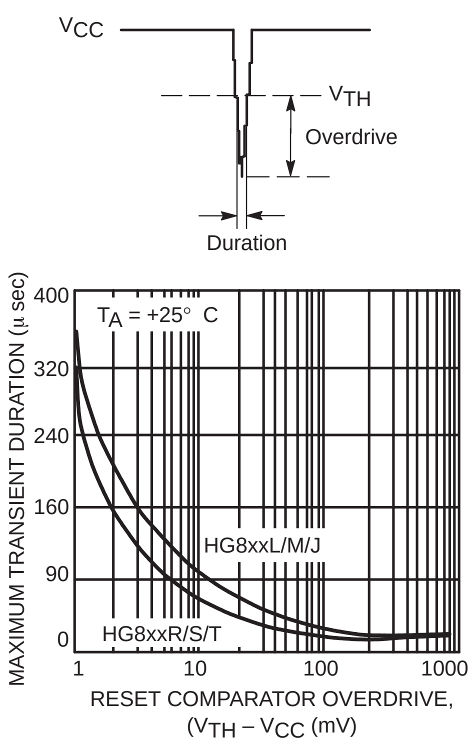


Figure 1. Maximum Transient Duration vs. Overdrive for Glitch Rejection at 25° C

$\overline{\text{RESET}}$ Signal Integrity During Power–Down

The HG809 $\overline{\text{RESET}}$ output is valid to V_{CC} = 1.0V. Below this voltage the output becomes an ”open circuit” and does not sink current. This means CMOS logic inputs to the μP will be floating at an undetermined voltage. Most digital systems are completely shutdown well above this voltage. However, in situations where $\overline{\text{RESET}}$ must be maintained valid to V_{CC} = 0V, a pull–down resistor must be connected from $\overline{\text{RESET}}$ to ground to discharge stray capacitances and hold the output low (Figure 2). This resistor value, though not critical, should be chosen such that it does not appreciably load $\overline{\text{RESET}}$ under normal operation (100kΩ will be suitable for most applications). Similarly, a pull–up resistor to V_{CC} is required for the HG810 to ensure a valid high $\overline{\text{RESET}}$ for V_{CC} below 1.0V.

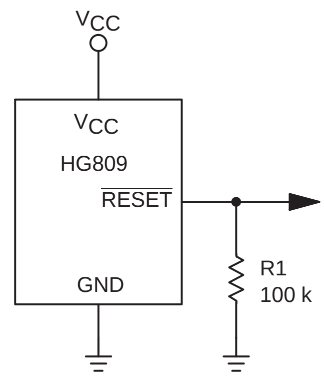


Figure 2. Ensuring RESET Valid to V_{CC} = 0 V

Processors With Bidirectional I/O Pins

Some μP's (such as Motorola 68HC11) have bi–directional reset pins. Depending on the current drive capability of the processor pin, an indeterminate logic level may result if there is a logic conflict. This can be avoided by adding a 4.7kΩ resistor in series with the output of the HG809/810 (Figure 3). If there are other components in the system which require a reset signal, they should be buffered so as not to load the reset line. If the other components are required to follow the reset I/O of the μP, the buffer should be connected as shown with the solid line.

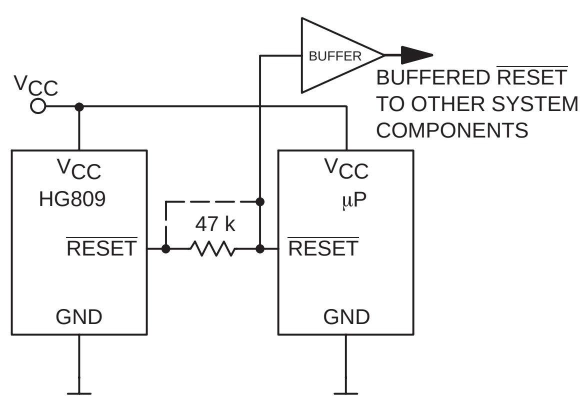


Figure 3. Interfacing to Bidirectional Reset I/O

TYPICAL CHARACTERISTICS

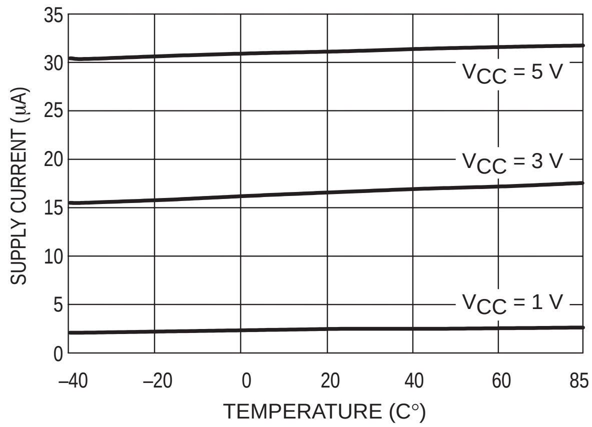


Figure 4. Supply Current vs Temperature (No Load, HG8xxR/S/T)

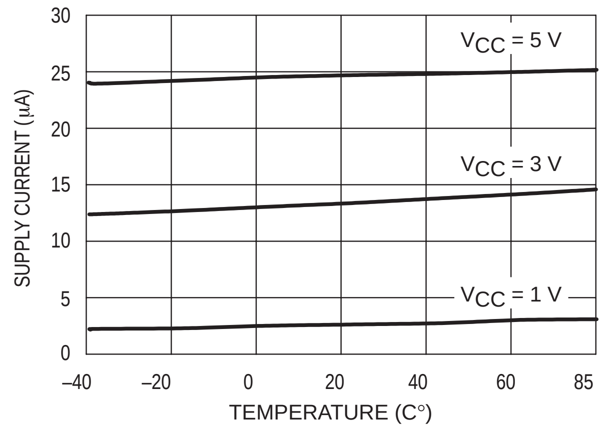


Figure 5. Supply Current vs Temperature (No Load,HG8xxL/M/J/)

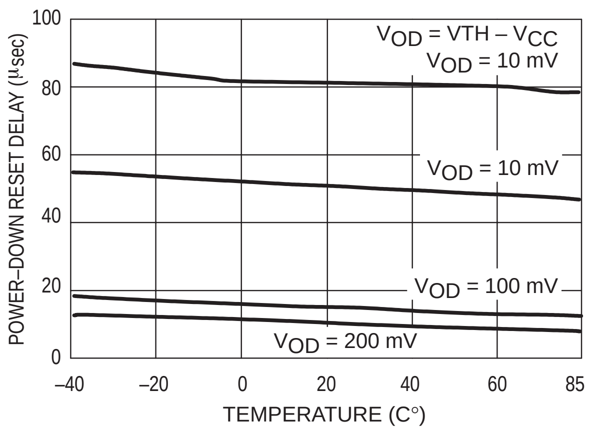


Figure 6. Power–Down Reset Delay vs Temperature and Overdrive (HG8xxR/S/T)

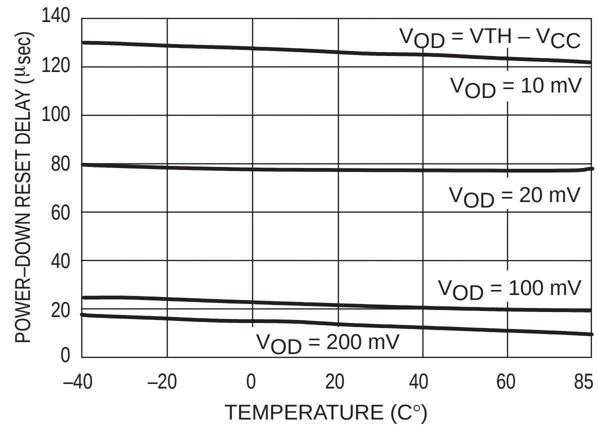


Figure 7. Power–Down Reset Delay vs Temperature and Overdrive (HG8xxL/M/J)

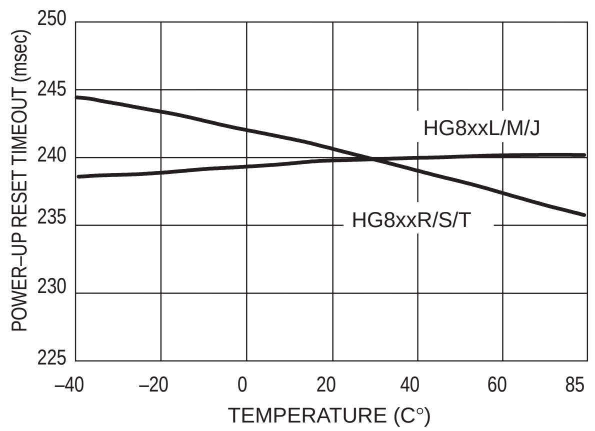


Figure 8. Power–Up Reset Timeout vs Temperature

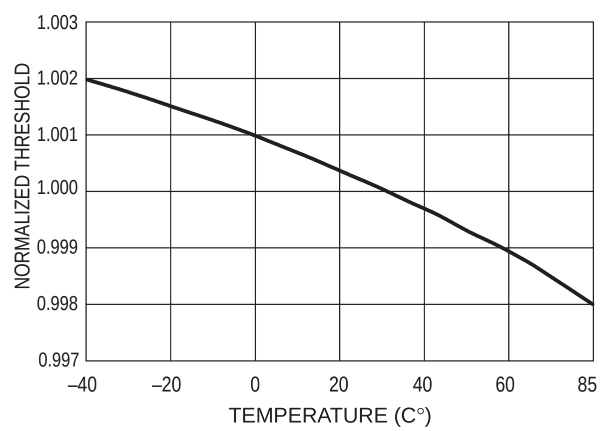


Figure 9. Normalized Reset Threshold vs Temperature

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