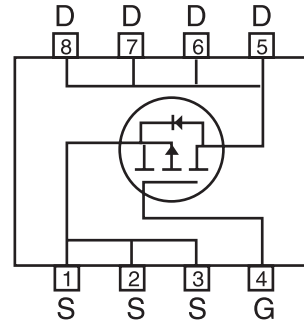
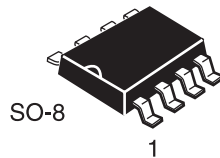


## P-Channel Enhancement Mode MOSFET

### FEATURES

- -30V , -5.3A ,  $R_{DS(ON)}=50m\Omega$  @  $V_{GS}=-10V$ .  
 $R_{DS(ON)}=90m\Omega$  @  $V_{GS}=-4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Surface Mount Package.



### ABSOLUTE MAXIMUM RATINGS ( $T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous <sup>a</sup> @ $T_J=125^{\circ}C$ -Pulsed <sup>b</sup>	$I_D$	$\pm 5.3$	A
	$I_{DM}$	$\pm 20$	A
Drain-Source Diode Forward Current <sup>a</sup>	$I_S$	-1.9	A
Maximum Power Dissipation <sup>a</sup>	$P_D$	2.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^{\circ}C$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	50	C/W
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**ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V			-1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS<sup>b</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = -250μA	-1		-3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -5.3A		40	50	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.2A		67	90	mΩ
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> = -5V, V <sub>GS</sub> = -10V	-20			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -15V, I <sub>D</sub> = -5.3A	4	8.3		S
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V f = 1.0MHz		860	1120	pF
Output Capacitance	C <sub>OSS</sub>			458	600	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			140	190	pF
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>D</sub> = -15V, I <sub>D</sub> = -1A, V <sub>GEN</sub> = -10V, R <sub>GEN</sub> = 6Ω		9	30	ns
Rise Time	t <sub>r</sub>			16	60	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			75	120	ns
Fall Time	t <sub>f</sub>			40	100	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -15V, I <sub>D</sub> = -5.3A, V <sub>GS</sub> = -10V		29	40	nC
Gate-Source Charge	Q <sub>gs</sub>			3		nC
Gate-Drain Charge	Q <sub>gd</sub>			9		nC

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = -5.3A		-0.84	-1.3	V

Notes

- a. Surface Mounted on FR4 Board, t ≤ 10sec.
- b. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- c. Guaranteed by design, not subject to production testing.

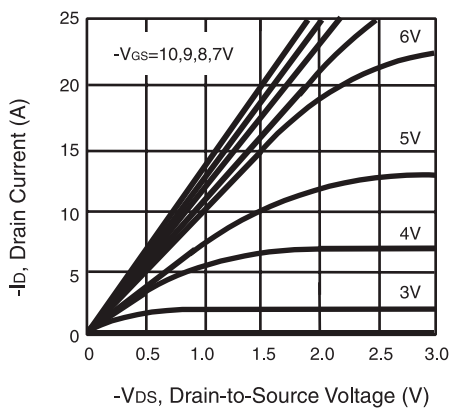


Figure 1. Output Characteristics

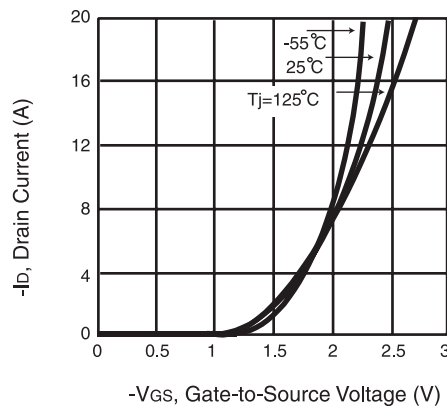


Figure 2. Transfer Characteristics

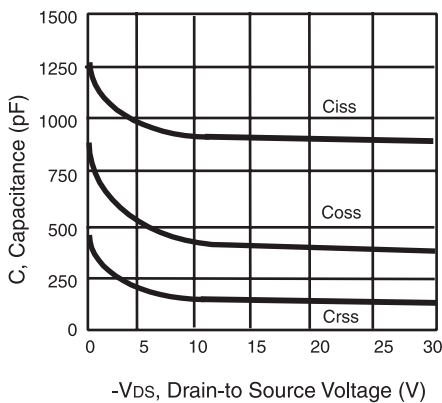


Figure 3. Capacitance

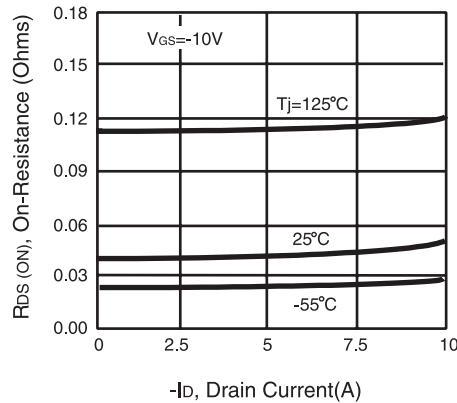
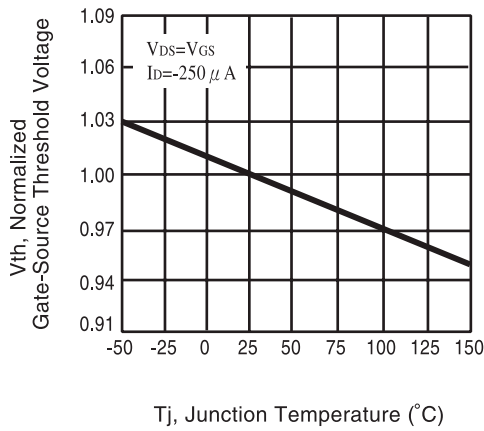
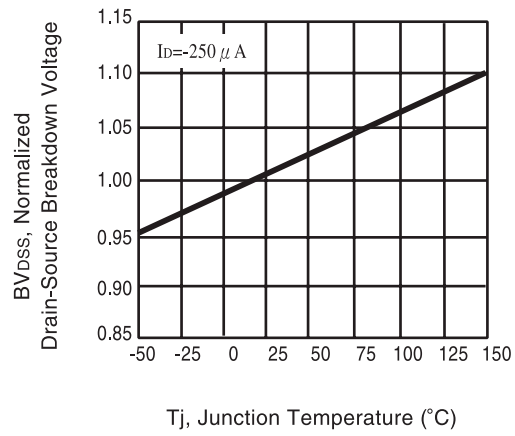


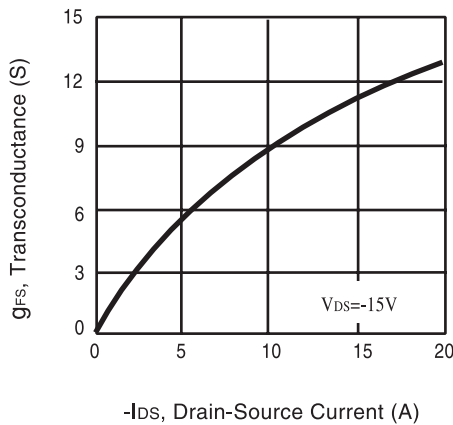
Figure 4. On-Resistance Variation with Drain Current and Temperature



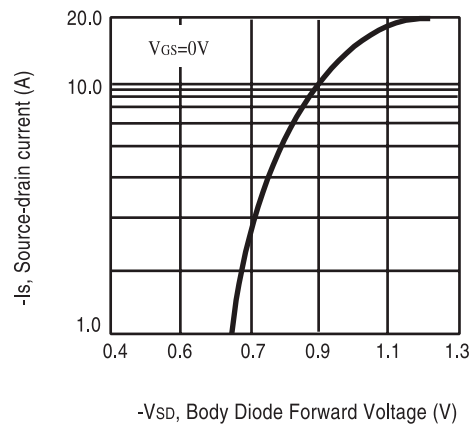
**Figure 5. Gate Threshold Variation with Temperature**



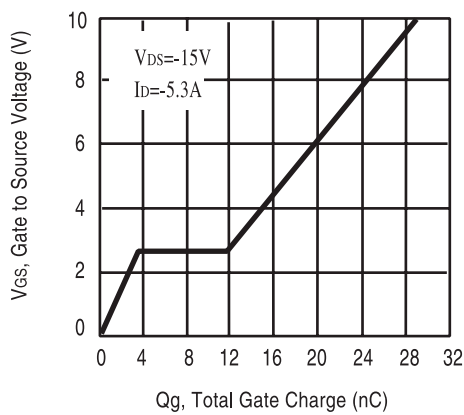
**Figure 6. Breakdown Voltage Variation with Temperature**



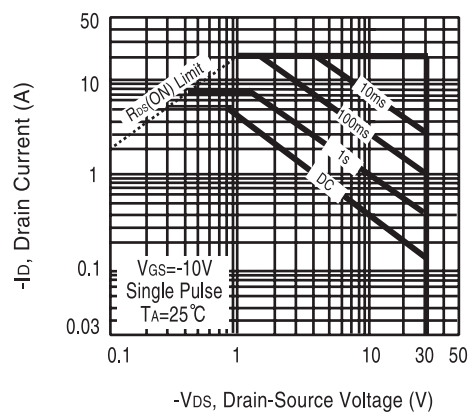
**Figure 7. Transconductance Variation with Drain Current**



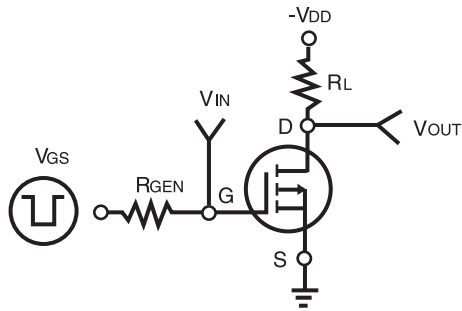
**Figure 8. Body Diode Forward Voltage Variation with Source Current**



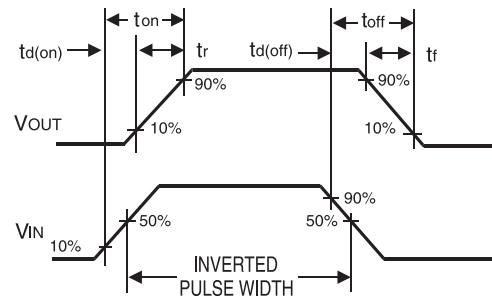
**Figure 9. Gate Charge**



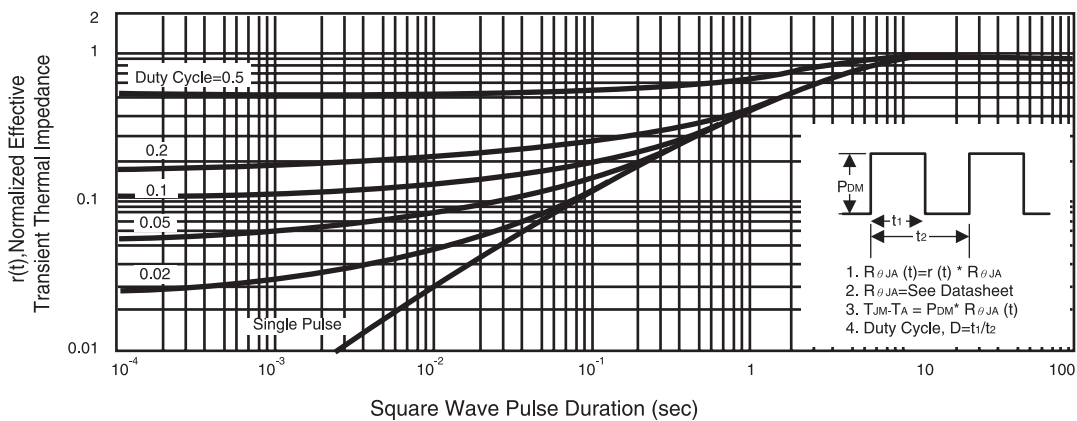
**Figure 10. Maximum Safe Operating Area**



**Figure 11. Switching Test Circuit**



**Figure 12. Switching Waveforms**



**Figure 13. Normalized Thermal Transient Impedance Curve**

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