65HVD308xE Low-Power RS-485 Transceivers, Available in a Small MSOP-8 Package

Features

- Available in a Small MSOP-8 Package
- Meets or Exceeds the Requirements of the TIA/EIA-485A Standard
- Low Quiescent Power
  - 0.3-mA Active Mode
  - 1-nA Shutdown Mode
- 1/8 Unit Load up to 256 Nodes on a Bus
- Bus-Pin ESD Protection up to 15 kV
- Industry-Standard HG75176 Footprint
- Failsafe Receiver (Bus Open, Bus Shorted, Bus Idle)
- Glitch-Free Power-Up and Power-Down Bus Inputs and Outputs

Applications

- Energy Meter Networks
- Motor Control
- Power Inverters
- Industrial Automation
- Building Automation Networks
- Battery-Powered Applications
- Telecommunications Equipment

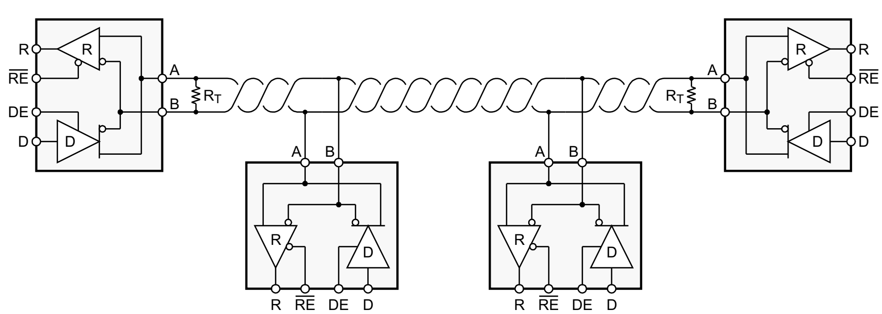
Description

The 65/75HVD308xE devices are half-duplex transceivers designed for RS-485 data bus networks. Powered by a 5-V supply, they are fully compliant with TIA/EIA-485A standard. With controlled transition times, these devices are suitable for transmitting data over long twisted-pair cables. 65HVD3082E and 75HVD3082E devices are optimized for signaling rates up to 200 kbps. The 65HVD3085E device is suitable for data transmission up to 1 Mbps, whereas the 65HVD3088E device is suitable for applications that require signaling rates up to 20 Mbps.

These devices are designed to operate with very low supply current, typically 0.3 mA, exclusive of the load. When in the inactive-shutdown mode, the supply current drops to a few nanoamps, which makes these devices ideal for power-sensitive applications.

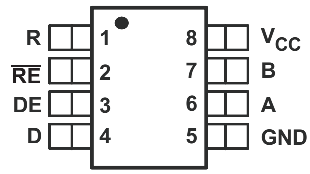
The wide common-mode range and high ESD-protection levels of these devices makes them suitable for demanding applications such as energy meter networks, electrical inverters, status and command signals across telecom racks, cabled chassis interconnects, and industrial automation networks where noise tolerance is essential. These devices match the industry-standard footprint of the HG75176 device. Power-on-reset circuits keep the outputs in a high-impedance state until the supply voltage has stabilized. A thermal-shutdown function protects the device from damage due to system fault conditions. The 75HVD3082E is characterized for operation from 0°C to 70°C and 65HVD308xE are characterized for operation from –40°C to 85°C air temperature. The D package version of the 65HVD3082E has been characterized for operation from –40°C to 105°C.

Simplified Schematic



Pin Configuration and Functions

D, P, and DGK Packages
8-Pin SOIC, VSSOP, and PDIP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V_{CC}	8	Supply	4.5-V to 5.5-V supply

Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1) (2)

	MIN	MAX	UNIT
Supply voltage, V_{CC}	–0.5	7	V
Voltage at A or B	–9	14	V
Voltage at any logic pin	–0.3	V_{CC} + 0.3	V
Receiver output current	–24	24	mA
Voltage input, transient pulse, A and B, through 100 Ω (see Figure 20)	–50	50	V
Junction Temperature, T_J		170	°C
Storage temperature, T_{stg}		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus pins and GND	±15000	V
			All pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	
		Electrical Fast Transient/Burst, A, B, and GND(3)		±4000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Tested in accordance with IEC 61000-4-4.

Recommended Operating Conditions

over operating free-air temperature range unless otherwise noted[(1)]

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		5.5	V
Voltage at any bus terminal (separately or common mode) , V_I		–7		12	
High-level input voltage (D, DE, or $\overline{RE}$ inputs), V_{IH}		2		V_{CC}	V
Low-level input voltage (D, DE, or $\overline{RE}$ inputs), V_{IL}		0		0.8	V
Differential input voltage, V_{ID}		–12		12	V
Output current, I_O	Driver	–60		60	mA
	Receiver	–8		8	
Differential load resistance, R_L		54	60		Ω
Signaling rate, $1/t_{UI}$	65HVD3082E, 75HVD3082E			0.2	Mbps
	65HVD3085E			1	
	65HVD3088E			20	
Operating free-air temperature, T_A	65HVD3082E (D package)	–40		105	°C
	65HVD3082E (DGK and P packages), 65HVD3085E, 65HVD3088E	–40		85	
	75HVD3082E	0		70	
Junction temperature, T_J		–40		130	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

Thermal Information

THERMAL METRIC[(1)]		65HVD3082E, 75HVD3082E, 65HVD3085E, 65HVD3088E		65HVD3082E, 65HVD3088E	UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	180	70	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80	66	80	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55	110	40	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.9	4.6	17.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47	73.1	28.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Electrical Characteristics: Driver

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage	I_O = 0, No Load	3	4.3		V
		R_L = 54 Ω (see Figure 8)	1.5	2.3		
		R_L = 100 Ω	2			
		V_{TEST} = –7 V to 12 V (see Figure 9)	1.5			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	See Figure 8 and Figure 9	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 10	1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		–0.1	0	0.1	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 10		500		mV
I_{OZ}	High-impedance output current	See receiver input currents in *Electrical Characteristics: Receiver*				
I_I	Input current	D, DE	–100		100	µA
I_{OS}	Short-circuit output current	−7 V ≤ V_O ≤ 12 V (see Figure 14)	–250		250	mA

(1) All typical values are at 25°C and with a 5-V supply.

Electrical Characteristics: Receiver

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage	I_O = –8 mA		–85	–10	mV
V_{IT-}	Negative-going differential input threshold voltage	I_O = 8 mA	–200	–115		mV
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})			30		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA (see Figure 15)	4	4.6		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_O = 8 mA (see Figure 15)		0.15	0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0 or V_{CC}, $\overline{RE}$ = V_{CC}	–1		1	µA
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V		0.04	0.1	mA
		V_{IH} = 12 V, V_{CC} = 0 V		0.06	0.125	
		V_{IH} = –7 V, V_{CC} = 5 V	–0.1	–0.04		
		V_{IH} = –7 V, V_{CC} = 0 V	–0.05	–0.03		
I_{IH}	High-level input current, ($\overline{RE}$)	V_{IH} = 2 V	–60	–30		µA
I_{IL}	Low-level input current, ($\overline{RE}$)	V_{IL} = 0.8 V	–60	–30		µA
C_{diff}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		7		pF

(1) All typical values are at 25°C and with a 5-V supply.

Power Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
I_{CC}	Driver and receiver enabled	D at V_{CC} or open, DE at V_{CC}, $\overline{RE}$ at 0 V, No load			425	900	µA
	Driver enabled, receiver disabled	D at V_{CC} or open, DE at V_{CC}, $\overline{RE}$ at V_{CC}, No load			330	600	µA
	Receiver enabled, driver disabled	D at V_{CC} or open, DE at 0 V, $\overline{RE}$ at 0 V, No load			300	600	µA
	Driver and receiver disabled	D at V_{CC} or open, DE at 0 V, $\overline{RE}$ at V_{CC}			0.001	2	µA
$P_{(AVG)}$	Average power dissipation	Input to D is a 50% duty cycle square wave at max specified signal rate R_L = 54 Ω V_{CC} = 5.5 V, T_J = 130°C	ALL HVD3082E			203	mW
			ALL HVD3085E			205	
			ALL HVD3088E			276	

(1) All typical values are at 25°C and with a 5-V supply.

Switching Characteristics: Driver

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	R_L = 54 Ω, C_L = 50 pF (see Figure 11)	HVD3082E		700	1300	ns
			HVD3085E		150	500	
			HVD3088E		12	20	
t_r t_f	Differential output signal rise time Differential output signal fall time	R_L = 54 Ω, C_L = 50 pF (see Figure 11)	HVD3082E	500	900	1500	ns
			HVD3085E		200	300	
			HVD3088E		7	15	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	R_L = 54 Ω, C_L = 50 pF (see Figure 11)	HVD3082E		20	200	ns
			HVD3085E		5	50	
			HVD3088E		1.4	2	
t_{PZH} t_{PZL}	Propagation delay time, high-impedance-to-high-level output Propagation delay time, high-impedance-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V (see Figure 12 and Figure 13)	HVD3082E		2500	7000	ns
			HVD3085E		1000	2500	
			HVD3088E		13	30	
t_{PHZ} t_{PLZ}	Propagation delay time, high-level-to-high-impedance output Propagation delay time, low-level-to-high-impedance output	R_L = 110 Ω, $\overline{RE}$ at 0 V (see Figure 12 and Figure 13)	HVD3082E		80	200	ns
			HVD3085E		60	100	
			HVD3088E		12	30	
$t_{PZH(SHDN)}$ $t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-high-level output Propagation delay time, shutdown-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at V_{CC} (see Figure 12)	HVD3082E		3500	7000	ns
			HVD3085E		2500	4500	
			HVD3088E		1600	2600	

Switching Characteristics: Receiver

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF (see Figure 16)	HVD3082E HVD3085E		75	200	ns
			HVD3086E			100	
t_{PHL}	Propagation delay time, high-to-low-level output		HVD3082E HVD3085E		79	200	ns
			HVD3088E			100	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)		HVD3082E HVD3085E		4	30	ns
			HVD3088E			10	
t_r	Output signal rise time	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF (see Figure 16)			1.5	3	ns
t_f	Output signal fall time				1.8	3	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, DE at 3 V (see Figure 17 and Figure 18)	HVD3082E HVD3085E		5	50	ns
			HVD3088E			30	
t_{PZL}	Output enable time to low level		HVD3082E HVD3085E		10	50	ns
			HVD3088E			30	
t_{PHZ}	Output enable time from high level		HVD3082E HVD3085E		5	50	ns
			HVD3088E			30	
t_{PLZ}	Output disable time from low level		HVD3082E HVD3085E		8	50	ns
			HVD3088E			30	
$t_{PZH(SHDN)}$	Propagation delay time, shutdown-to-high-level output	C_L = 15 pF, DE at 0 V, (see Figure 19)			1600	3500	ns
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output				1700	3500	ns

Typical Characteristics

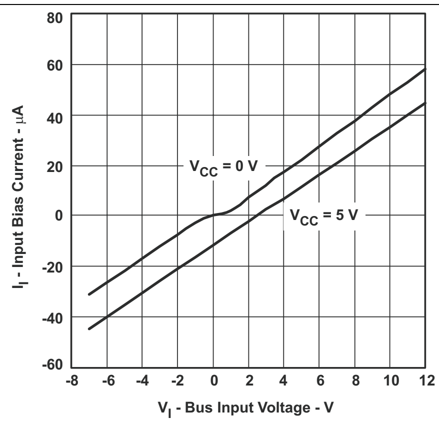


Figure 1. Bus Input Current versus Bus Input Voltage

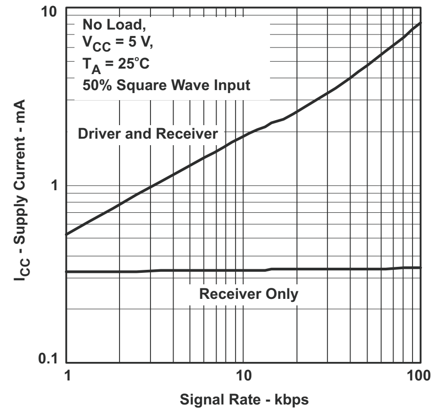


Figure 2. 65HVD3082E RMS Supply Current versus Signaling Rate

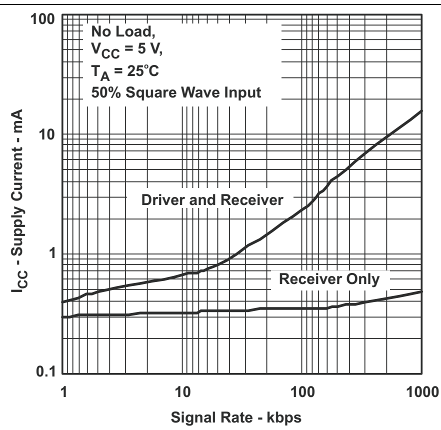


Figure 3. 65HVD3085E RMS Supply Current versus Signaling Rate

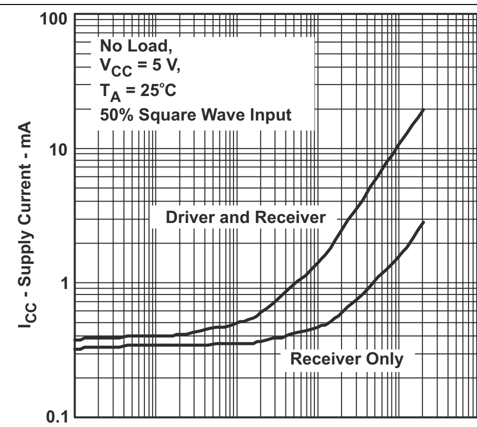


Figure 4. 65HVD3088E RMS Supply Current versus Signal Rate

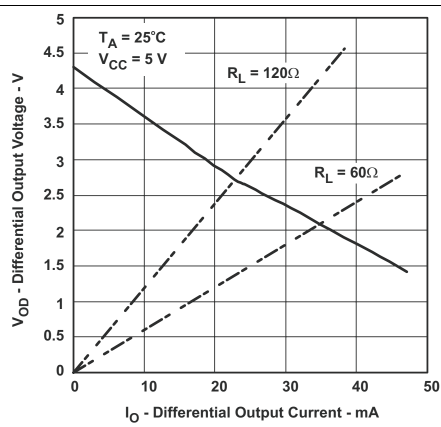


Figure 5. Driver Differential Output Voltage versus Driver Output Current

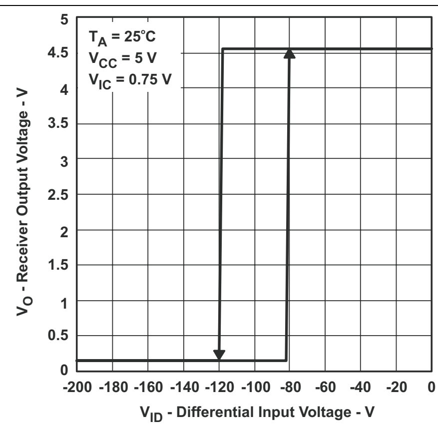


Figure 6. Receiver Output Voltage versus Differential Input Voltage

Typical Characteristics (continued)

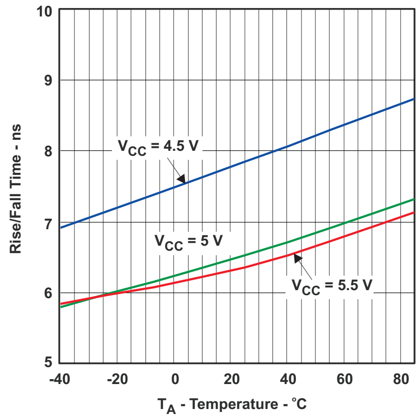


Figure 7. 65HVD3088E Driver Rise and Fall Time versus Temperature

Parameter Measurement Information

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50% duty cycle. Z_O = 50 Ω (unless otherwise specified).

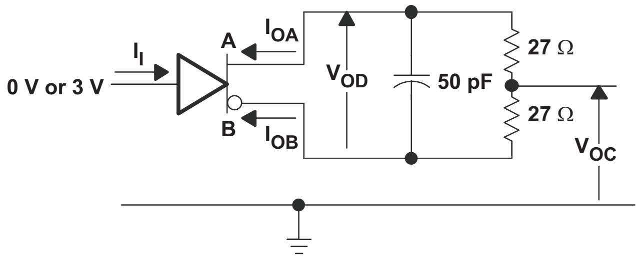


Figure 8. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

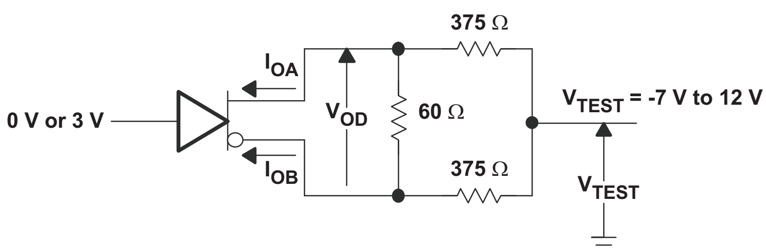


Figure 9. Driver Test Circuit, V_{OD} With Common-Mode Loading

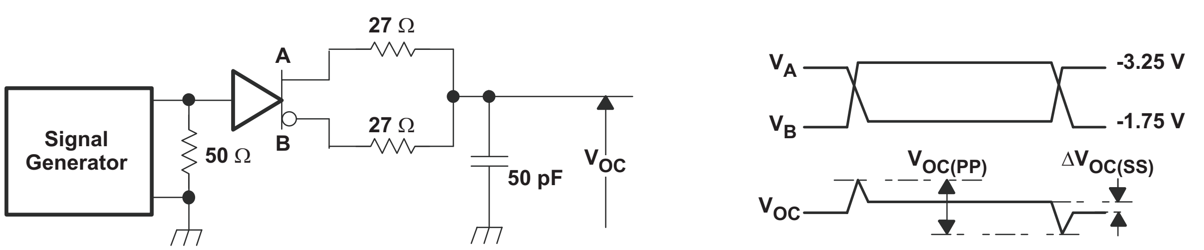


Figure 10. Driver V_{OC} Test Circuit and Waveforms

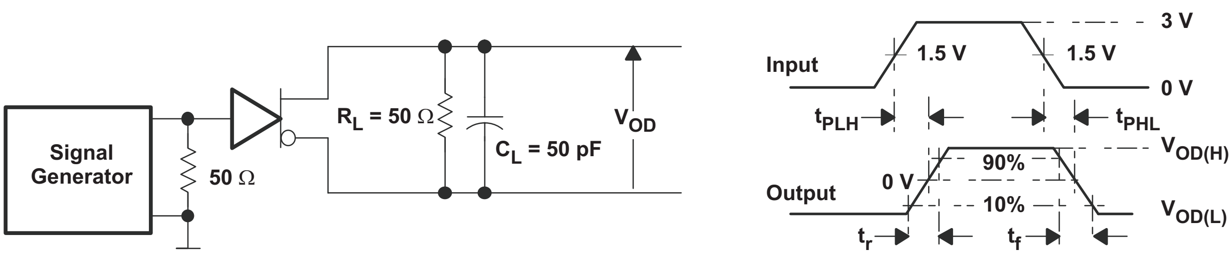


Figure 11. Driver Switching Test Circuit and Waveforms

Parameter Measurement Information (continued)

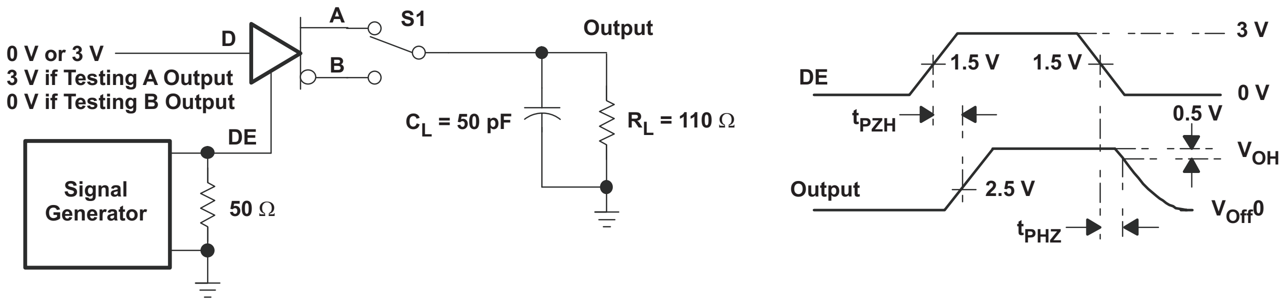


Figure 12. Driver Enable and Disable Test Circuit and Waveforms, High Output

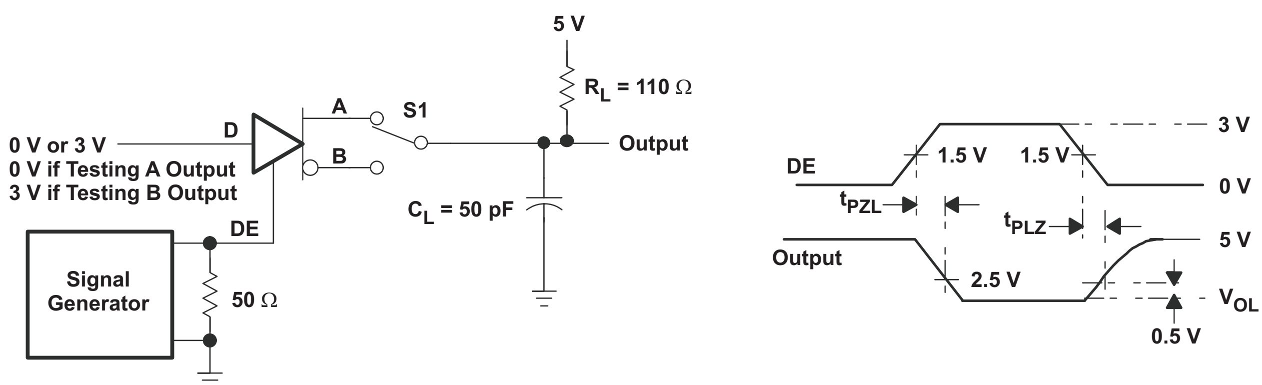


Figure 13. Driver Enable and Disable Test Circuit and Waveforms, Low Output

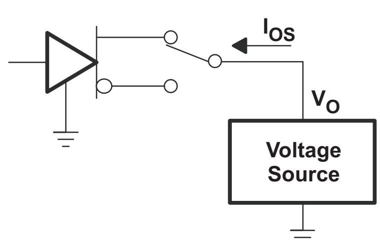


Figure 14. Driver Short-Circuit

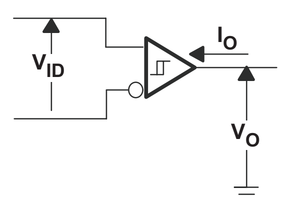


Figure 15. Receiver Switching Test Circuit and Waveforms

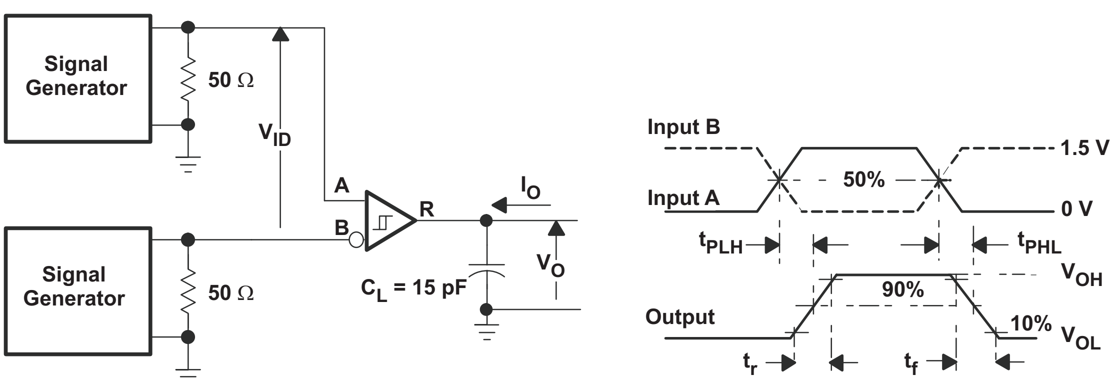


Figure 16. Receiver Switching Test Circuit and Waveforms

Parameter Measurement Information (continued)

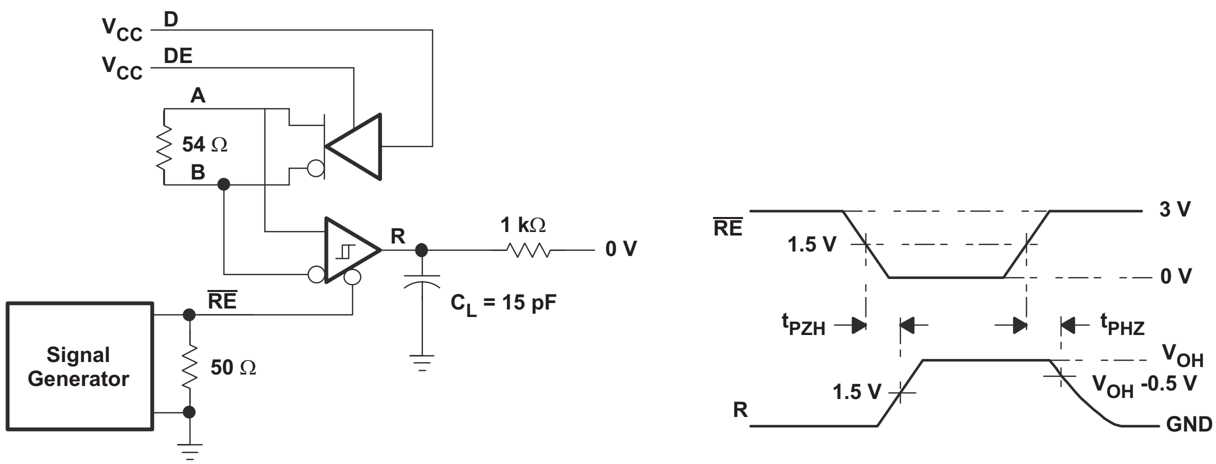


Figure 17. Receiver Enable and Disable Test Circuit and Waveforms, Data Output High

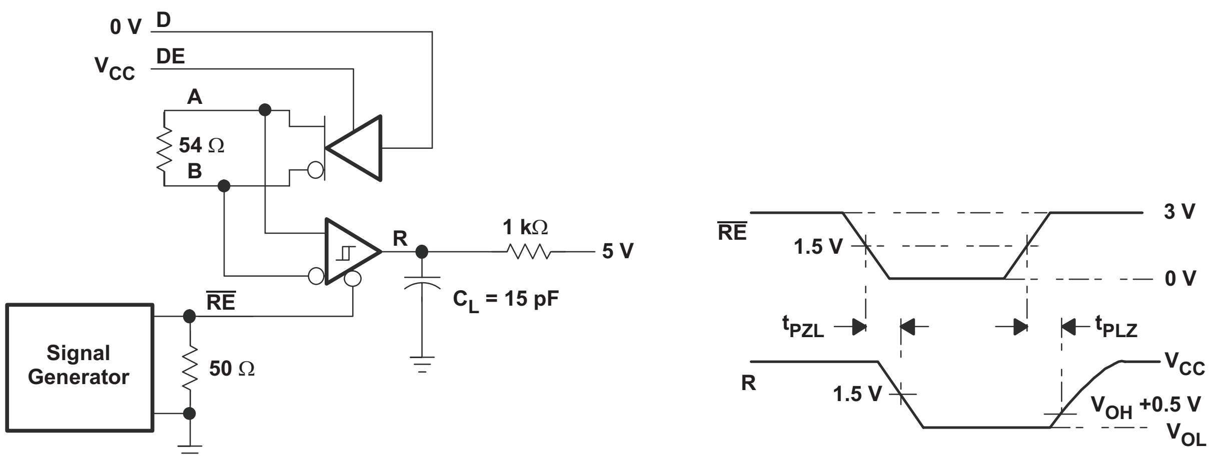


Figure 18. Receiver Enable and Disable Test Circuit and Waveforms, Data Output Low

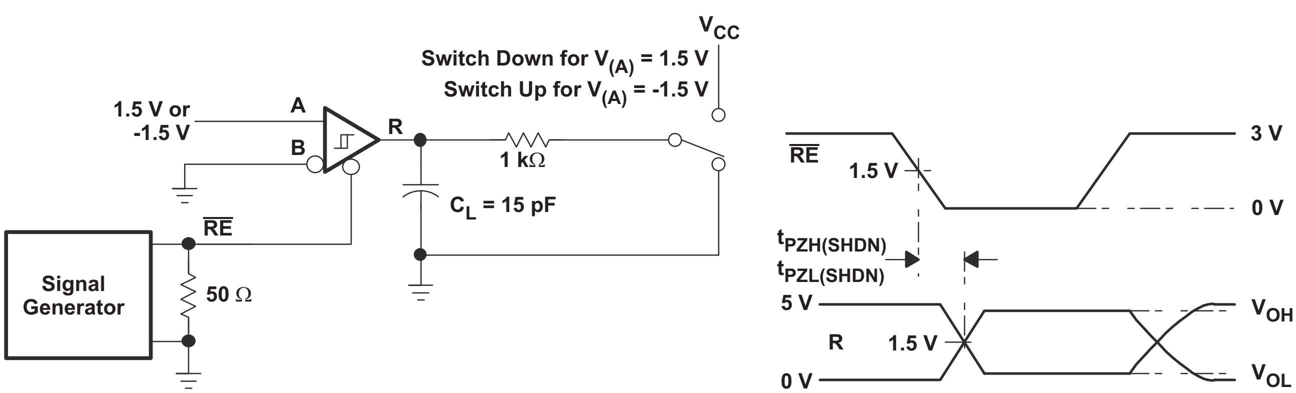


Figure 19. Receiver Enable From Shutdown Test Circuit and Waveforms

Parameter Measurement Information (continued)

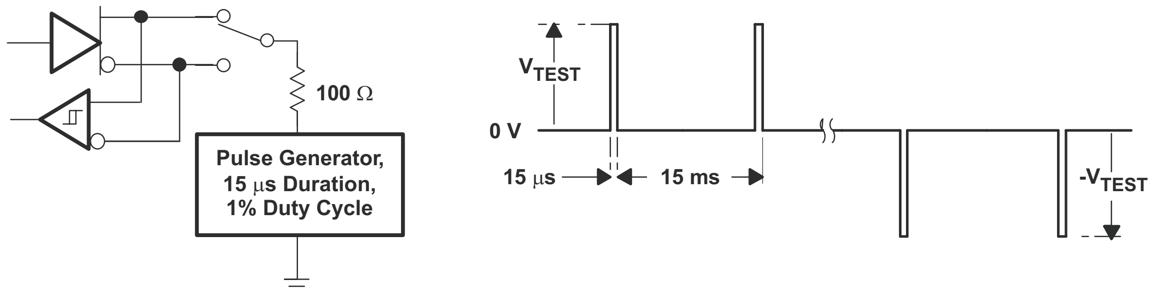


Figure 20. Test Circuit and Waveforms, Transient Overvoltage Test

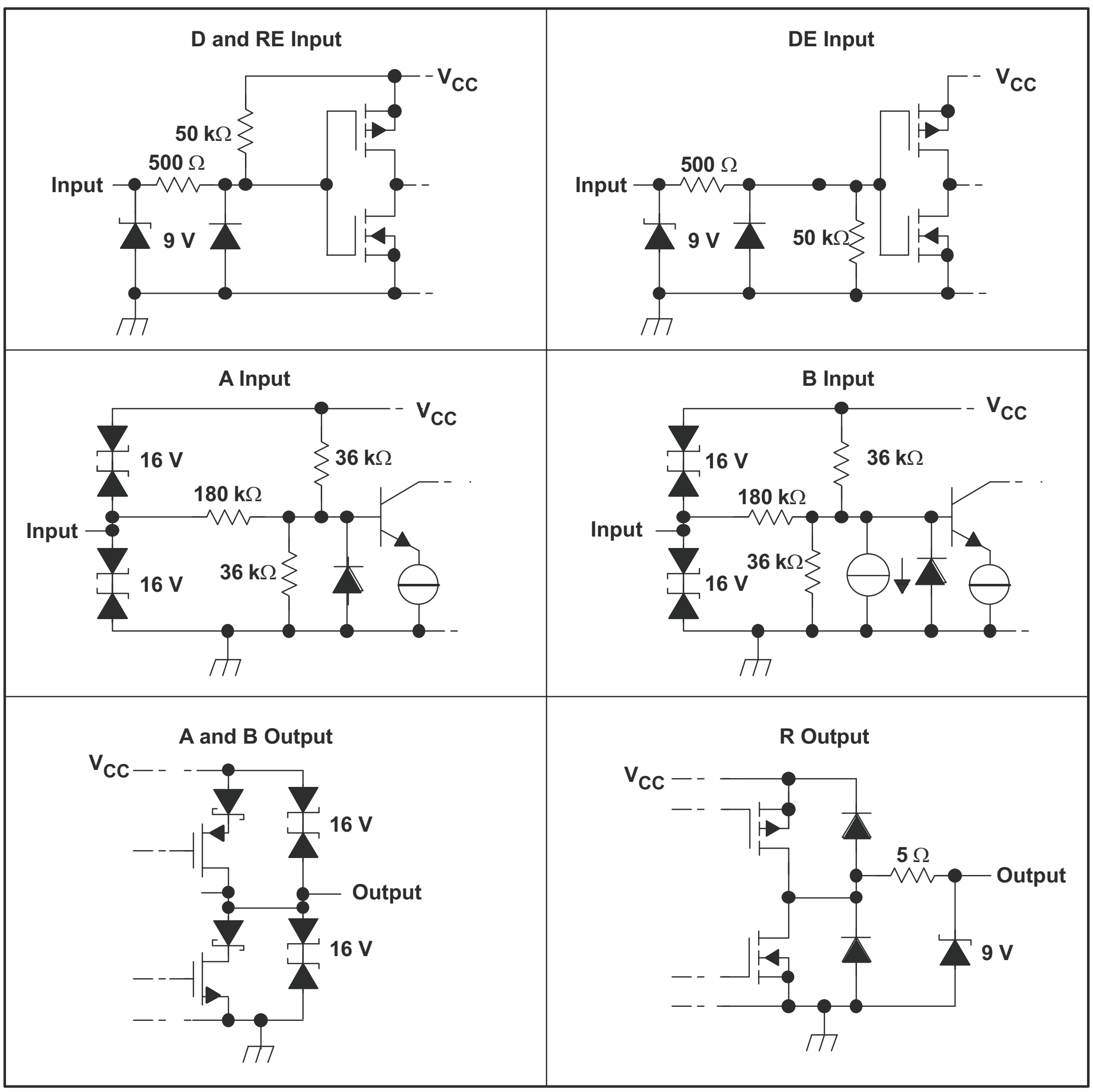
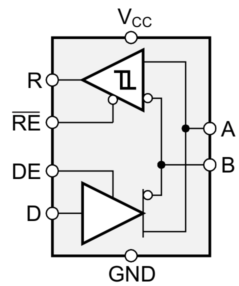


Figure 21. Equivalent Input and Output Schematic Diagrams

Overview

The 65/75HVD308xE family of half-duplex RS-485 transceivers is suitable for data transmission at rates up to 200 kbps (for 65HVD3082E and 75HVD3082E), 1 Mbps (for 65HVD3085E), or 20 Mbps (for 65HVD3088E) over controlled-impedance transmission media (such as twisted-pair cabling). Up to 256 units of 65/75HVD308xE may share a common RS-485 bus due to the family's low bus input currents. The devices also feature a high degree of ESD protection and typical standby current consumption of 1 nA.

Functional Block Diagram



Feature Description

The 65/75HVD308xE provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions. It features a typical hysteresis of 30 mV in order to improve noise immunity. Internal ESD protection circuits protect the transceiver bus terminals against ±15-kV Human Body Model (HBM) electrostatic discharges.

The devices protect themselves against damage due to overtemperature conditions through use a of a thermal shutdown feature. Thermal shutdown is entered at 165°C (nominal) and causes the device to enter a low-power state with high-impedance outputs.

Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 1. Driver Function Table

INPUT	ENABLE(1)	OUTPUTS(1)		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	$\overline{RE}$	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT–} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT–}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

Application Information

The 65/75HVD308xE devices are half-duplex RS-485 transceivers commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.

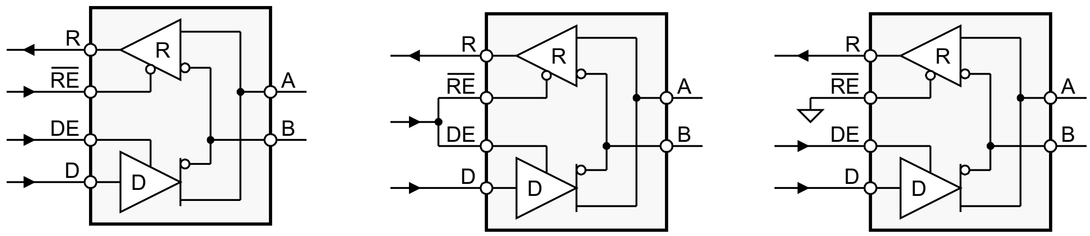


Figure 22. Half-Duplex Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

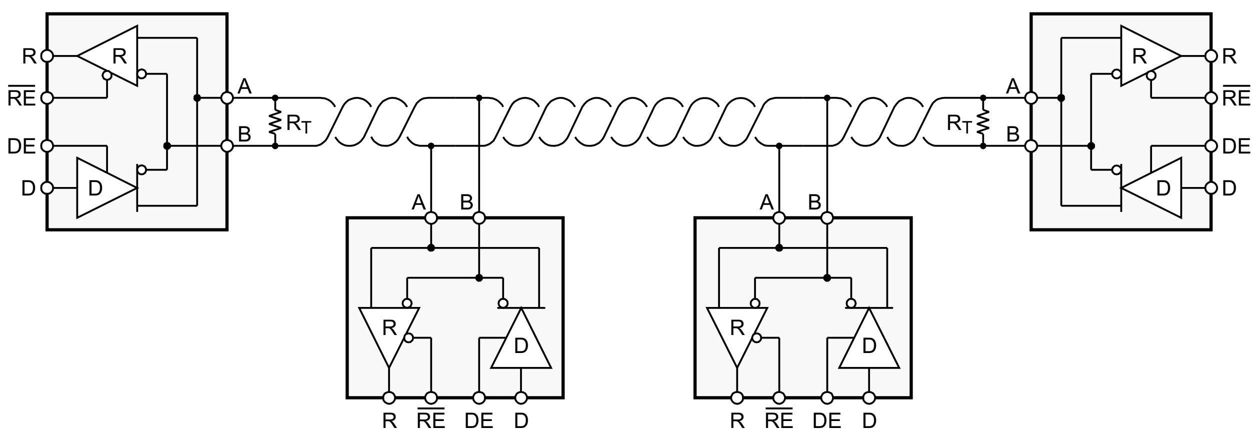


Figure 23. Typical Application Circuit

Typical Application (continued)

Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4,000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

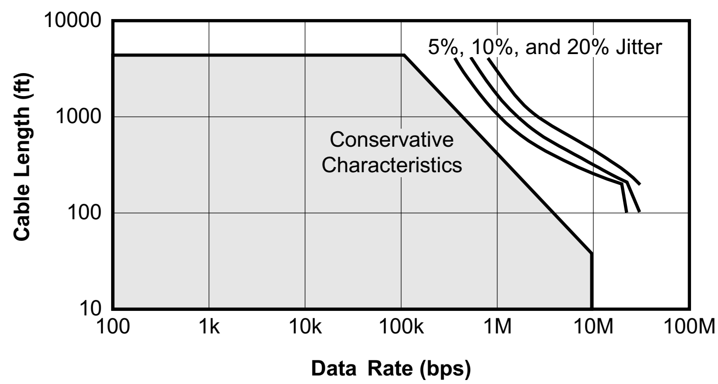


Figure 24. Cable Length vs Data Rate Characteristic

Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, must be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub must be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$L_{stub} \leq 0.1 \times t_r \times v \times c$

where:

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c (1)

Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the 65/75HVD308xE is a 1/8 UL transceiver, it is possible to connect up to 256 receivers to the bus.

Typical Application (continued)

Receiver Failsafe

The differential receiver is fail-safe to invalid bus states caused by:

- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than +200 mV, and must output a Low when the V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and V_{IT-} and V_{HYS}. As seen in the table, differential signals more negative than –200 mV will always cause a Low receiver output. Similarly, differential signals more positive than +200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output is High. Only when the differential input is more negative than V_{IT-} will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary.

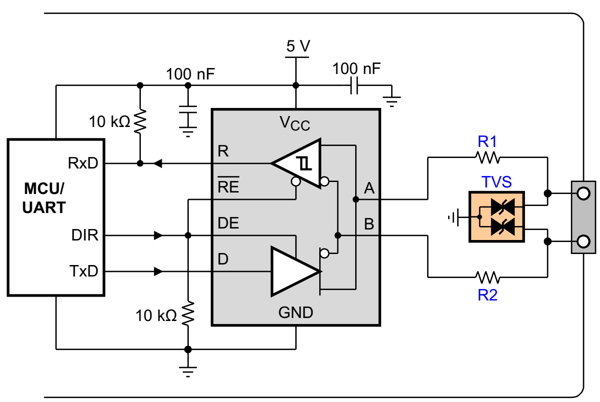


Figure 25. Transient Protection Against ESD, EFT, and Surge Transients

Power Usage in an RS-485 Transceiver

Power consumption is a concern in many applications. Power supply current is delivered to the bus load as well as to the transceiver circuitry. For a typical RS-485 bus configuration, the load that an active driver must drive consists of all of the receiving nodes, plus the termination resistors at each end of the bus.

The load presented by the receiving nodes depends on the input impedance of the receiver. The TIA/EIA-485-A standard defines a unit load as allowing up to 1 mA. With up to 32 unit loads allowed on the bus, the total current supplied to all receivers can be as high as 32 mA. The HVD308xE is rated as a 1/8 unit load device. As shown in , the bus input current is less than 1/8 mA, allowing up to 256 nodes on a single bus.

The current in the termination resistors depends on the differential bus voltage. The standard requires active drivers to produce at least 1.5 V of differential signal. For a bus terminated with one standard 120-Ω resistor at each end, this sums to 25 mA differential output current whenever the bus is active. Typically the HVD308xE can drive more than 25-mA to a 60-Ω load, resulting in a differential output voltage higher than the minimum required by the standard (see Figure 3).

Overall, the total load current can be 60 mA to a loaded RS-485 bus. This is in addition to the current required by the transceiver itself; the HVD308xE circuitry requires only about 0.4 mA with both driver and receiver enabled, and only 0.3 mA with either the driver enabled or with the receiver enabled. In low-power shutdown mode, neither the driver nor receiver is active, and the supply current is low.

Supply current increases with signaling rate primarily due to the totem pole outputs of the driver (see Figure 2). When these outputs change state, there is a moment when both the high-side and low-side output transistors are conducting and this creates a short spike in the supply current. As the frequency of state changes increases, more power is used.

Low-Power Shutdown Mode

When both the driver and receiver are disabled (DE low and $\overline{RE}$ high) the device is in shutdown mode. If the enable inputs are in this state for less than 60 ns, the device does not enter shutdown mode. This guards against inadvertently entering shutdown mode during driver or receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in shutdown mode. In this low-power shutdown mode, most internal circuitry is powered down, and the supply current is typically 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

If only the driver is re-enabled (DE transitions to high) the driver outputs are driven according to the D input after the enable times given by $t_{PZH(SHDN)}$ and $t_{PZL(SHDN)}$ in the driver switching characteristics. If the D input is open when the driver is enabled, the driver outputs defaults to A high and B low, in accordance with the driver failsafe feature.

If only the receiver is re-enabled (RE transitions to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by $t_{PZH(SHDN)}$ and $t_{PZL(SHDN)}$ in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input.

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