

## DIFFERENTIAL TRANSCEIVER WITH TRANSIENT VOLTAGE SUPPRESSION

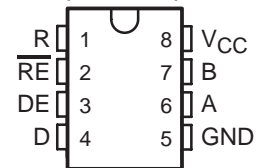
- Integrated Transient Voltage Suppression
- ESD Protection for Bus Terminals Exceeds:
  - ±30 kV IEC 61000-4-2, Contact Discharge
  - ±15 kV IEC 61000-4-2, Air-Gap Discharge
  - ±15 kV EIA/JEDEC Human Body Model
- Circuit Damage Protection of 400-W Peak (Typical) Per IEC 61000-4-5
- Controlled Driver Output-Voltage Slew Rates Allow Longer Cable Stub Lengths
- 250-kbps in Electrically Noisy Environments
- Open-Circuit Fail-Safe Receiver Design
- 1/4 Unit Load Allows for 128 Devices Connected on Bus
- Thermal Shutdown Protection
- Power-Up/-Down Glitch Protection
- Each Transceiver Meets or Exceeds the Requirements of TIA/EIA-485 (RS-485) and ISO/IEC 8482:1993(E) Standards
- Low Disabled Supply Current 300  $\mu$ A Max
- Pin Compatible With SN75176
- Applications:
  - Industrial Networks
  - Utility Meters
  - Motor Control

### description

The SN75LBC184 and SN65LBC184 are differential data line transceivers in the trade-standard footprint of the SN75176 with built-in protection against high-energy noise transients. This feature provides a substantial increase in reliability for better immunity to noise transients coupled to the data cable over most existing devices. Use of these circuits provides a reliable low-cost direct-coupled (with no isolation transformer) data line interface without requiring any external components.

The SN75LBC184 and SN65LBC184 can withstand overvoltage transients of 400-W peak (typical). The conventional combination wave called out in IEC 61000-4-5 simulates the overvoltage transient and models a unidirectional surge caused by overvoltages from switching and secondary lightning transients.

SN65LBC184D (Marked as 6LB184)  
 SN75LBC184D (Marked as 7LB184)  
 SN65LBC184P (Marked as 65LBC184)  
 SN75LBC184P (Marked as 75LBC184)  
 (TOP VIEW)



### functional logic diagram (positive logic)

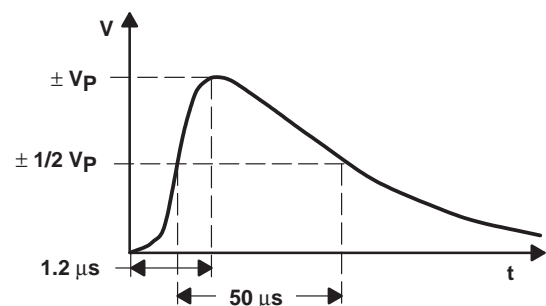
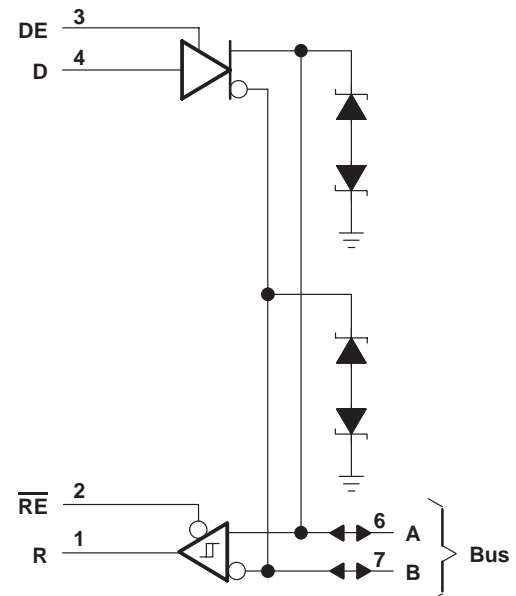


Figure 1. Surge Waveform — Combination Wave

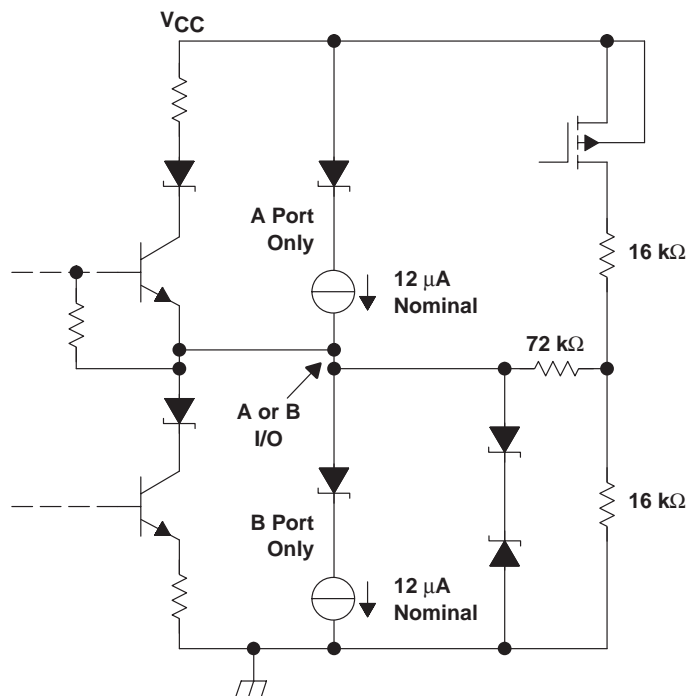
**description (continued)**

A biexponential function defined by separate rise and fall times for voltage and current simulates the combination wave. The standard 1.2  $\mu$ s/50  $\mu$ s combination waveform is shown in Figure 1 and in the test description in Figure 15.

The device also includes additional desirable features for party-line data buses in electrically noisy environment applications including industrial process control. The differential-driver design incorporates slew-rate-controlled outputs sufficient to transmit data up to 250 kbps. Slew-rate control allows longer unterminated cable runs and longer stub lengths from the main backbone than possible with uncontrolled and faster voltage transitions. A unique receiver design provides a fail-safe output of a high level when the inputs are left floating (open circuit). The SN75LBC184 and SN65LBC184 receiver also includes a high input resistance equivalent to one-fourth unit load allowing connection of up to 128 similar devices on the bus.

The SN75LBC184 is characterized for operation from 0°C to 70°C. The SN65LBC184 is characterized from -40°C to 85°C.

**schematic of inputs and outputs**



**DRIVER FUNCTION TABLE**

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

**RECEIVER FUNCTION TABLE**

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A - B	$\overline{RE}$	R
$V_{ID} \geq 0.2 V$	L	H
$-0.2 V < V_{ID} < 0.2 V$	L	?
$V_{ID} \leq -0.2 V$	L	L
X	H	Z
Open	L	H

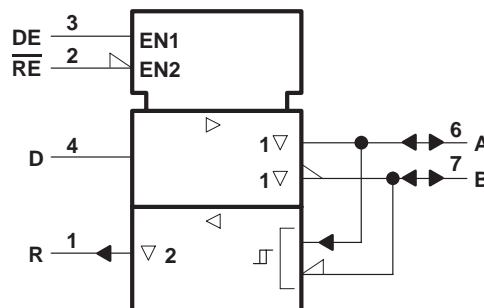
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

**AVAILABLE OPTIONS**

T <sub>A</sub>	PACKAGE	
	PLASTIC SMALL-OUTLINE† (JEDEC MS-012)	PLASTIC DUAL-IN-LINE PACKAGE (JEDEC MS-001)
0°C to 70°C	SN75LBC184D	SN75LBC184P
-40°C to 85°C	SN65LBC184D	SN65LBC184P

† Add R suffix for taped and reel.

**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ (see Note 1)	.....	-0.5 V to 7 V
Continuous voltage range at any bus terminal	.....	-15 V to 15 V
Data input/output voltage	.....	-0.3 V to 7 V
Receiver output current, $I_O$	.....	$\pm 20$ mA
Electrostatic discharge: Contact discharge (IEC61000-4-2) A, B, GND (see Note 2)	.....	30 kV
Air discharge (IEC61000-4-2) A, B, GND (see Note 2)	.....	15 kV
Human body model (see Note 3) A, B, GND (see Note 2)	.....	15 kV
	All pins	3 kV
	All terminals (Class 3A) (see Note 2)	8 kV
	All terminals (Class 3B) (see Note 2)	1200 V
Continuous total power dissipation (see Note 4)	.....	Internally Limited

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.  
 2. GND and bus terminal ESD protection is beyond readily available test equipment capabilities for IEC 61000-4-2, EIA/JEDEC test method A114-A and MIL-STD-883C method 3015. Ratings listed are limits of test equipment; device performance exceeds these limits.  
 3. Tested in accordance with JEDEC Standard 22, Test Method A114-A.  
 4. The driver shuts down at a junction temperature of approximately 160°C. To operate below this temperature, see the Dissipation Rating Table.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW

**recommended operating conditions**

		MIN‡	TYP	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), $V_I$ or $V_{IC}$		-7		12	V
High-level input voltage, $V_{IH}$	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, $V_{IL}$	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, $ V_{ID} $				12	V
High-level output current, $I_{OH}$	Driver	-60			mA
	Receiver	-8			mA
Low-level output current, $I_{OL}$	Driver			60	mA
	Receiver			4	
Operating free-air temperature, $T_A$	SN75LBC184	0		70	°C
	SN65LBC184	-40		85	°C

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet.

**DRIVER SECTION**
**electrical characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER	ALTERNATE SYMBOLS	TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
I <sub>CC</sub>	Supply current	NA	DE = $\overline{\overline{RE}}$ = 5 V, No Load		12	25	mA
			DE = 0 V, $\overline{\overline{RE}}$ = 5 V, No Load		175	300	μA
I <sub>IH</sub>	High-level input current (D, DE, $\overline{\overline{RE}}$ )	NA	V <sub>I</sub> = 2.4 V		50	μA	
I <sub>IL</sub>	Low-level input current (D, DE, $\overline{\overline{RE}}$ )	NA	V <sub>I</sub> = 0.4 V		-50	μA	
I <sub>OS</sub>	Short-circuit output current (see Note 5)	NA	V <sub>O</sub> = -7 V		-250	-120	mA
			V <sub>O</sub> = V <sub>CC</sub>		250		
			V <sub>O</sub> = 12 V		250		
I <sub>OZ</sub>	High-impedance output current	NA			See Receiver I <sub>I</sub>	mA	
V <sub>O</sub>	Output voltage	V <sub>Oa</sub> , V <sub>Ob</sub>	I <sub>O</sub> = 0		0	V <sub>CC</sub>	V
V <sub>OC(PP)</sub>	Peak-to-peak change in common-mode output voltage during state transitions	NA	See Figures 5 and 6		0.8		V
V <sub>OC</sub>	Common-mode output voltage	V <sub>Osl</sub>	See Figure 4		1	3	V
ΔV <sub>OC(SS)</sub>	Magnitude of change, common-mode steady-state output voltage	V <sub>Oss</sub> - $\overline{V_{Oss}}$	See Figure 5		0.1		V
V <sub>ODI</sub>	Magnitude of differential output voltage  V <sub>A</sub> - V <sub>B</sub>	V <sub>O</sub>	I <sub>O</sub> = 0		1.5	6	V
			R <sub>L</sub> = 54 Ω, See Figure 4		1.5		V
Δ V <sub>ODI</sub>	Change in differential voltage magnitude between logic states	V <sub>t1</sub>   - $\overline{ V_{t1} }$	R <sub>L</sub> = 54 Ω			0.1	V

 † All typical values are measured with T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5 V.

NOTE 5: This parameter is measured with only one output being driven at a time.

**switching characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>d(DH)</sub>	R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF, See Figure 5			1.3	μs
t <sub>d(DL)</sub>				1.3	μs
t <sub>PLH</sub>		0.5	1.3	μs	
t <sub>PHL</sub>		0.5	1.3	μs	
t <sub>sk(p)</sub>		75	150	ns	
t <sub>r</sub>		0.25	1.2	μs	
t <sub>f</sub>		0.25	1.2	μs	
t <sub>PZH</sub>	R <sub>L</sub> = 110 Ω, See Figure 2			3.5	μs
t <sub>PZL</sub>	R <sub>L</sub> = 110 Ω, See Figure 3			3.5	μs
t <sub>PHZ</sub>	R <sub>L</sub> = 110 Ω, See Figure 2			2	μs
t <sub>PLZ</sub>	R <sub>L</sub> = 110 Ω, See Figure 3			2	μs

**RECEIVER SECTION**
**electrical characteristics over recommended operating conditions (unless otherwise noted)**

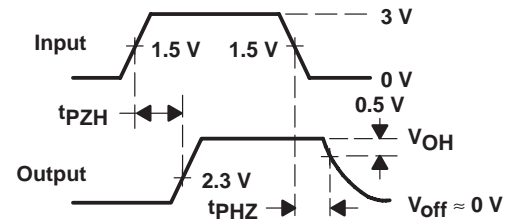
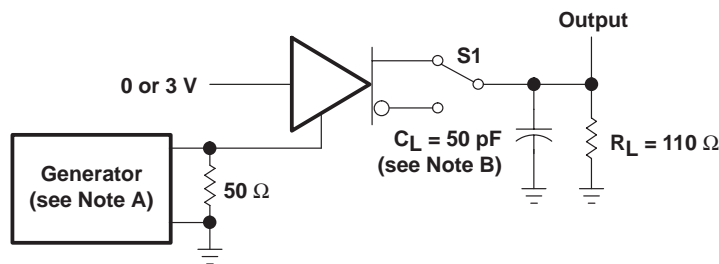
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I <sub>CC</sub>	Supply current (total package)	DE = $\overline{RE}$ = 0 V,	No Load			3.9	mA
		$\overline{RE}$ = 5 V, No Load	DE = 0 V,			300	μA
I <sub>I</sub>	Input current	Other input = 0 V	V <sub>I</sub> = 12 V			250	μA
			V <sub>I</sub> = 12 V, V <sub>CC</sub> = 0			250	
			V <sub>I</sub> = -7 V			-200	
			V <sub>I</sub> = -7 V, V <sub>CC</sub> = 0			-200	
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = 0.4 V to 2.4 V				±100	μA
V <sub>hys</sub>	Input hysteresis voltage				70		mV
V <sub>IT+</sub>	Positive-going input threshold voltage					200	mV
V <sub>IT-</sub>	Negative-going input threshold voltage					-200	mV
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -8 mA	Figure 7			2.8	V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA	Figure 7			0.4	V

 † All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

**switching characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>pLH</sub>	Propagation delay time, low-to-high-level output	C <sub>L</sub> = 50 pF,	See Figure 7			150	ns
t <sub>pHL</sub>	Propagation delay time, high-to-low-level output					150	ns
t <sub>sk(p)</sub>	Pulse skew ( t <sub>pHL</sub> - t <sub>pLH</sub>  )					50	ns
t <sub>r</sub>	Rise time, single ended	See Figure 7			20		ns
t <sub>f</sub>	Fall time, single ended				20		ns
t <sub>pZH</sub>	Output enable time to high level	See Figure 8				100	ns
t <sub>pZL</sub>	Output enable time to low level					100	ns
t <sub>PHZ</sub>	Output disable time from high level					100	ns
t <sub>PLZ</sub>	Output disable time from low level					100	ns

**PARAMETER MEASUREMENT INFORMATION**

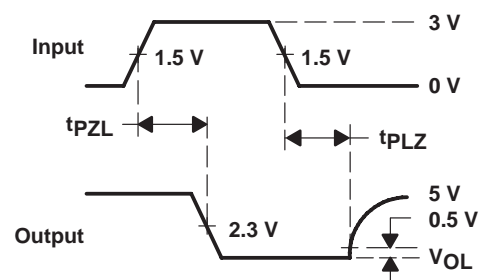
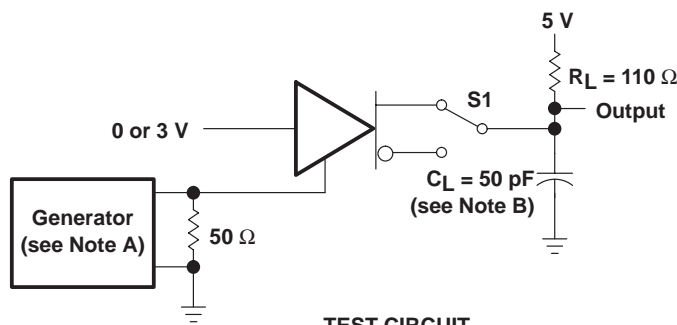


**TEST CIRCUIT**

**VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

**Figure 2. Driver  $t_{pZH}$  and  $t_{pHZ}$  Test Circuit and Voltage Waveforms**

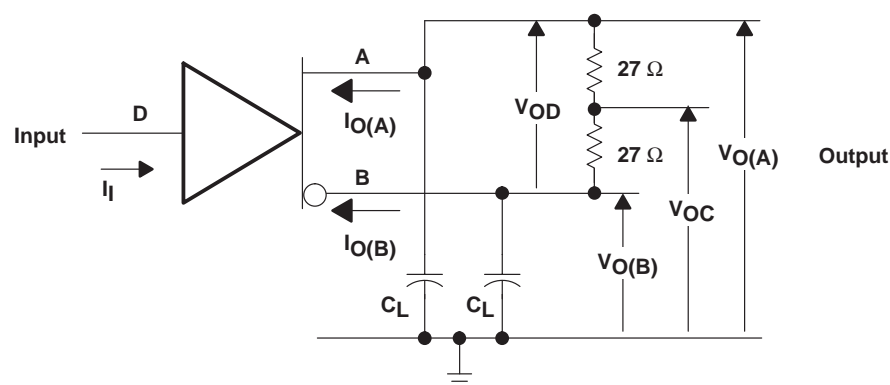


**TEST CIRCUIT**

**VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

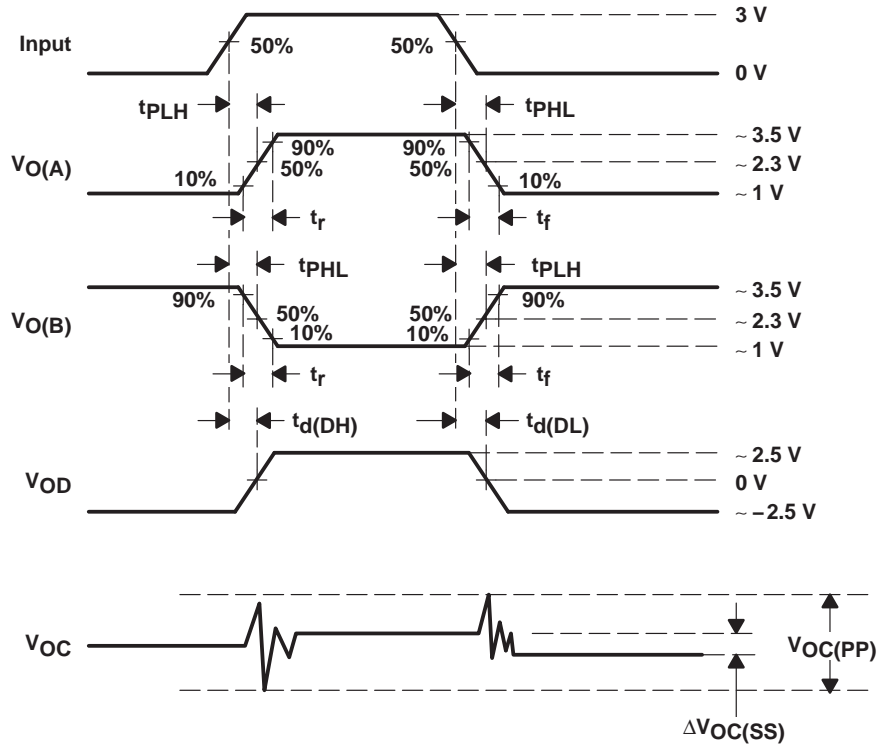
**Figure 3. Driver  $t_{pZL}$  and  $t_{pLZ}$  Test Circuit and Voltage Waveforms**



NOTES: A. Resistance values are in ohms and are 1% tolerance.  
B.  $C_L$  includes probe and jig capacitance.

**Figure 4. Driver Test Circuit, Voltage, and Current Definitions**

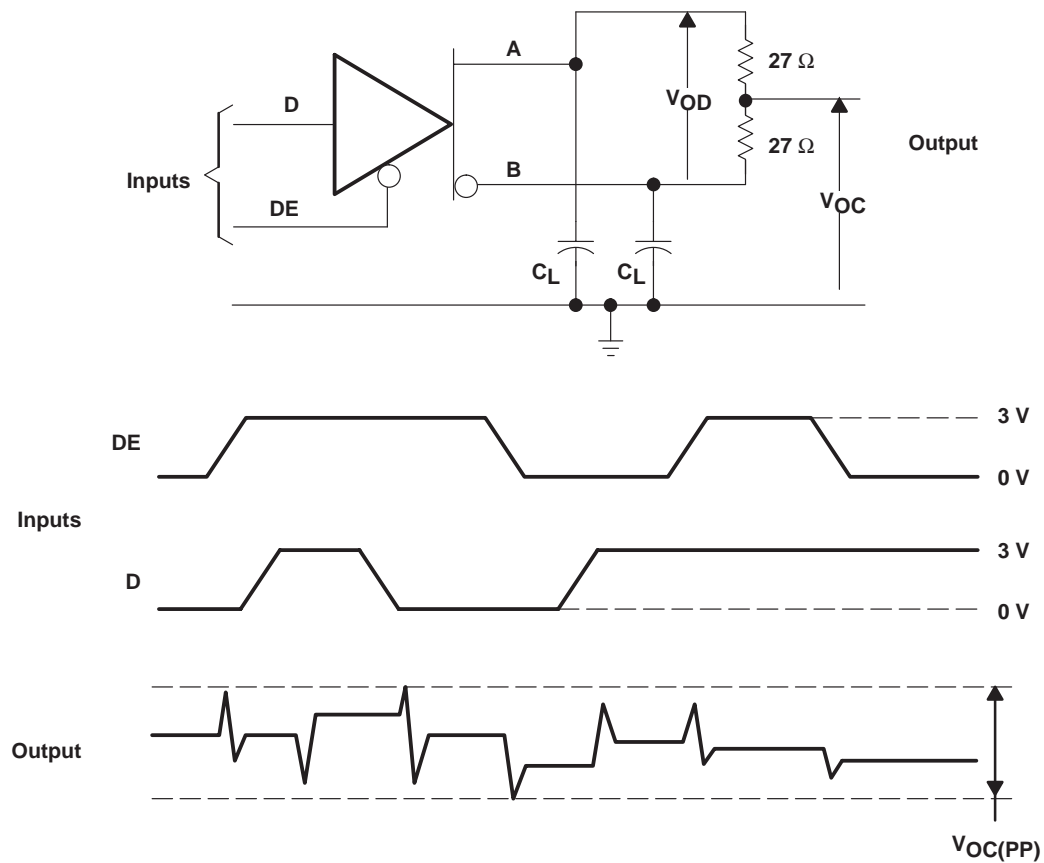
**PARAMETER MEASUREMENT INFORMATION**



**Figure 5. Driver Timing, Voltage and Current Waveforms**

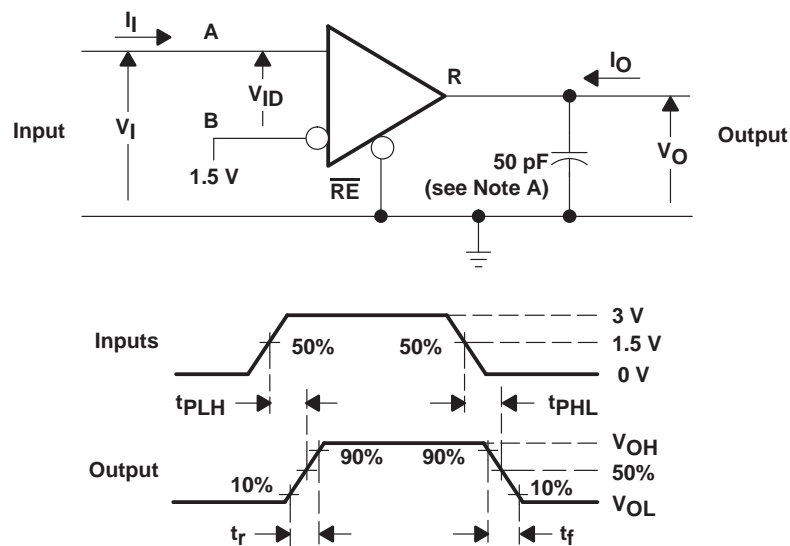


**PARAMETER MEASUREMENT INFORMATION**



NOTES: A. Resistance values are in ohms and are 1% tolerance.  
B.  $C_L$  includes probe and jig capacitance ( $\pm 10\%$ ).

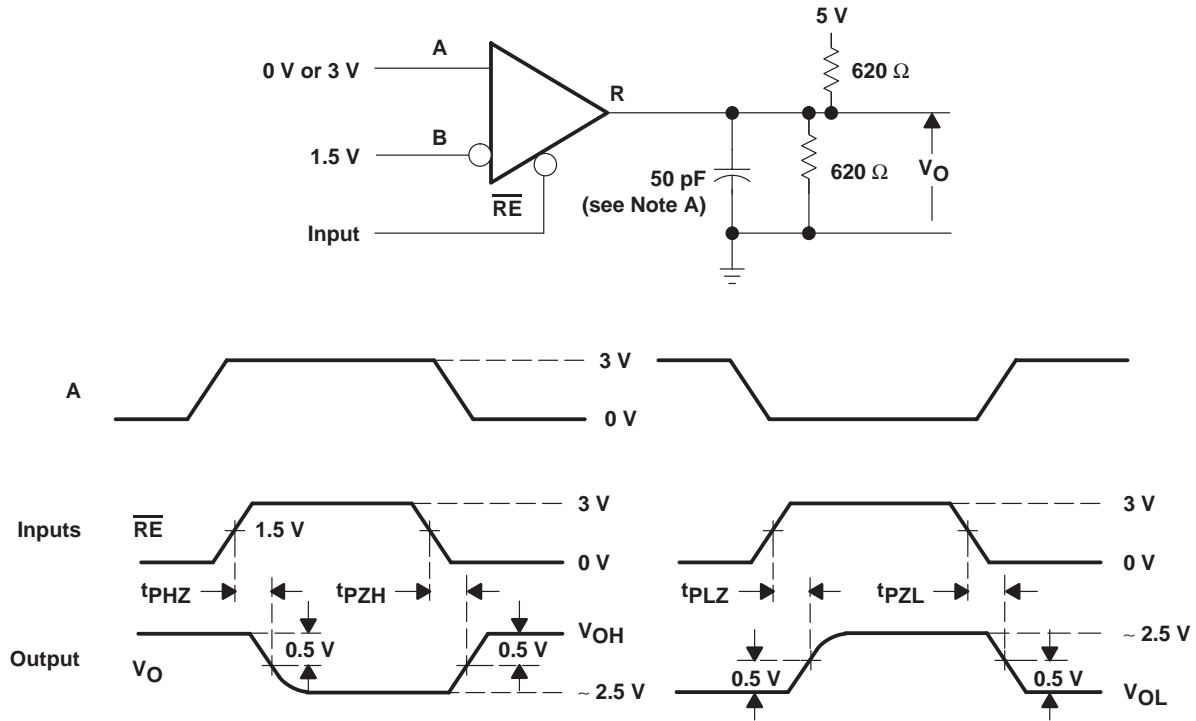
**Figure 6. Driver  $V_{OC(PP)}$  Test Circuit and Waveforms**



NOTE A: This value includes probe and jig capacitance ( $\pm 10\%$ ).

**Figure 7. Receiver  $t_{PLH}$  and  $t_{PHL}$  Test Circuit and Voltage Waveforms**

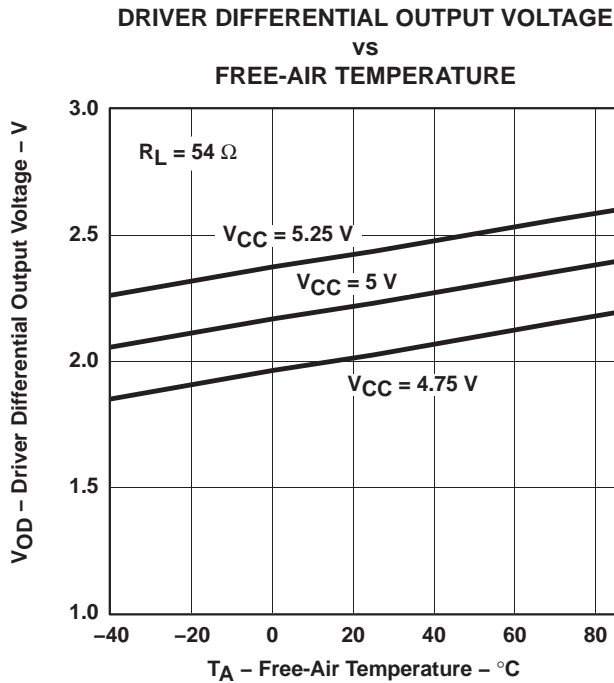
**PARAMETER MEASUREMENT INFORMATION**



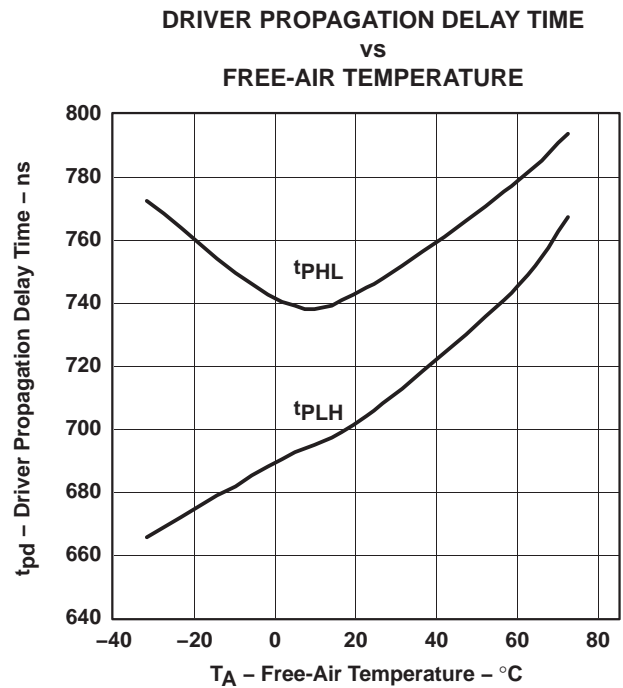
NOTE A: This value includes probe and jig capacitance ( $\pm 10\%$ ).

**Figure 8. Receiver  $t_{PZL}$ ,  $t_{PLZ}$ ,  $t_{PZH}$ , and  $t_{PHZ}$  Test Circuit and Voltage Waveforms**

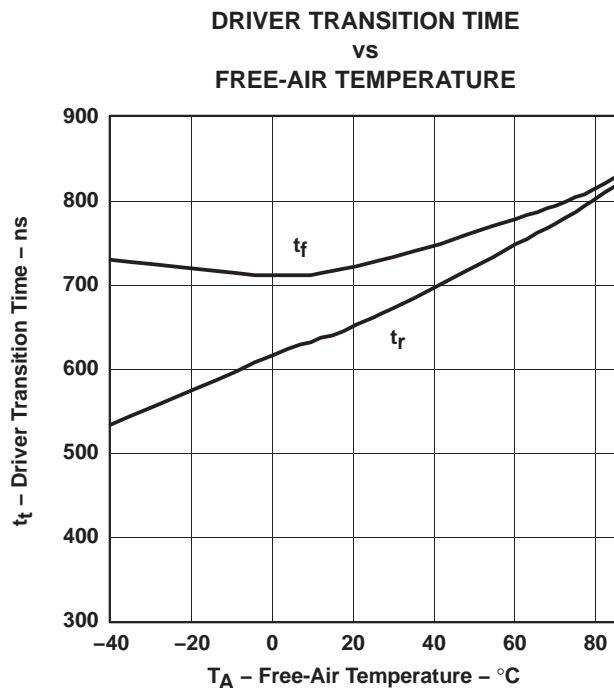
**TYPICAL CHARACTERISTICS**



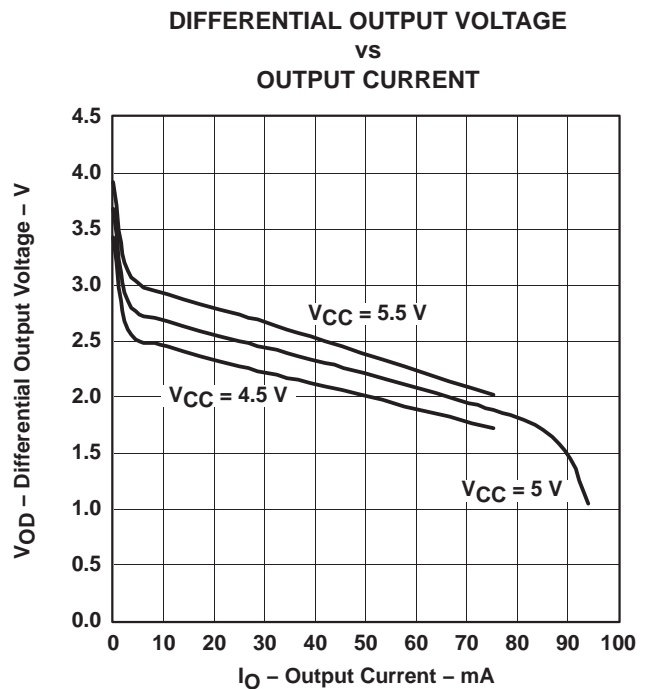
**Figure 9**



**Figure 10**

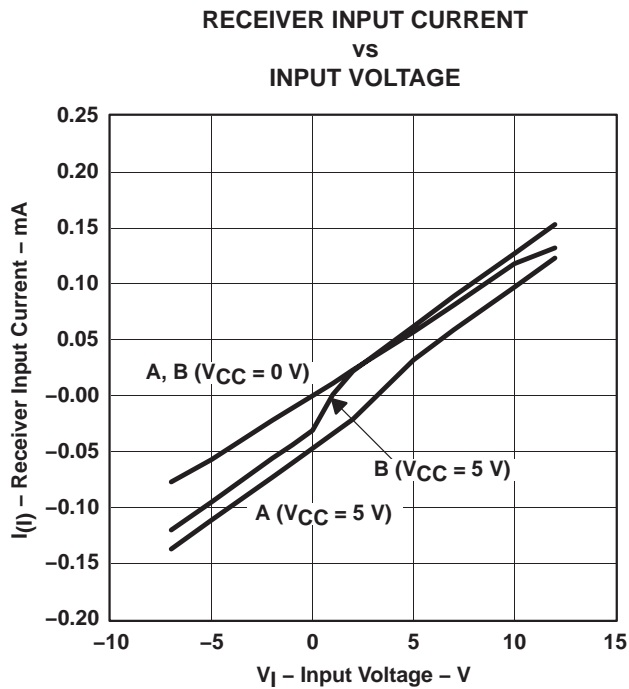


**Figure 11**



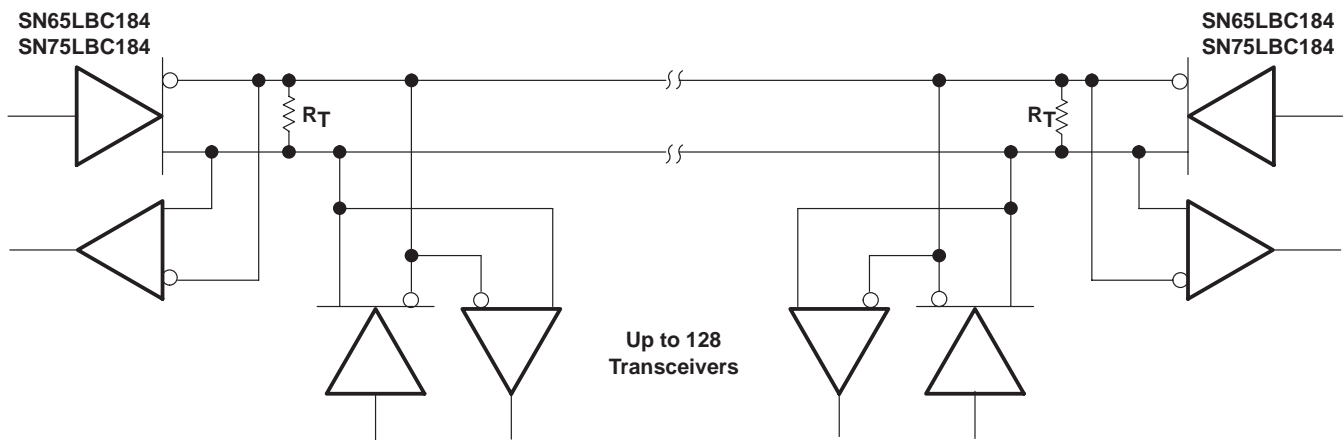
**Figure 12**

**TYPICAL CHARACTERISTICS**



**Figure 13**

**APPLICATION INFORMATION**



NOTE A: The line should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

**Figure 14. Typical Application Circuit**

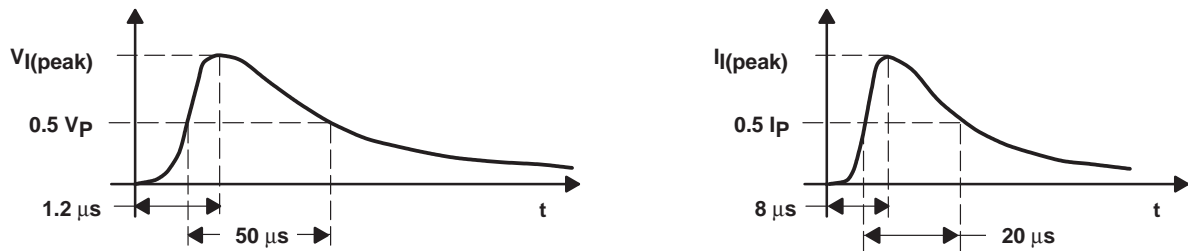
**APPLICATION INFORMATION**

**'LBC184 test description**

The 'LBC184 is tested against the IEC 61000-4-5 recommended transient identified as the combination wave. The combination wave provides a 1.2-/50- $\mu$ s open-circuit voltage waveform and a 8-/20- $\mu$ s short-circuit current waveform shown in Figure 15. The testing is performed with a combination/hybrid pulse generator with an effective output impedance of 2  $\Omega$ . The setup for the overvoltage stress is shown in Figure 16 with all testing performed with power applied to the 'LBC184 circuit.

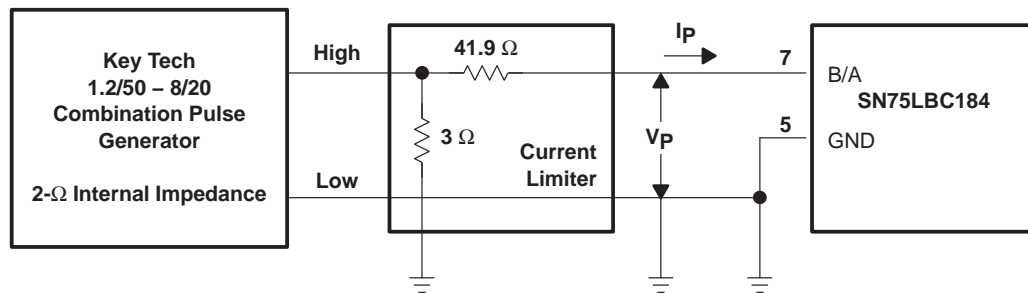
**NOTE**

High voltage transient testing is done on a sampling basis.



**Figure 15. Short-Circuit Current Waveforms**

The 'LBC184 is tested and evaluated for both maximum (single pulse) as well as life test (multiple pulse) capabilities. The 'LBC184 is evaluated against transients of both positive and negative polarity and all testing is performed with the worst-case transient polarity. Transient pulses are applied to the bus pins (A & B) across ground as shown in Figure 16.



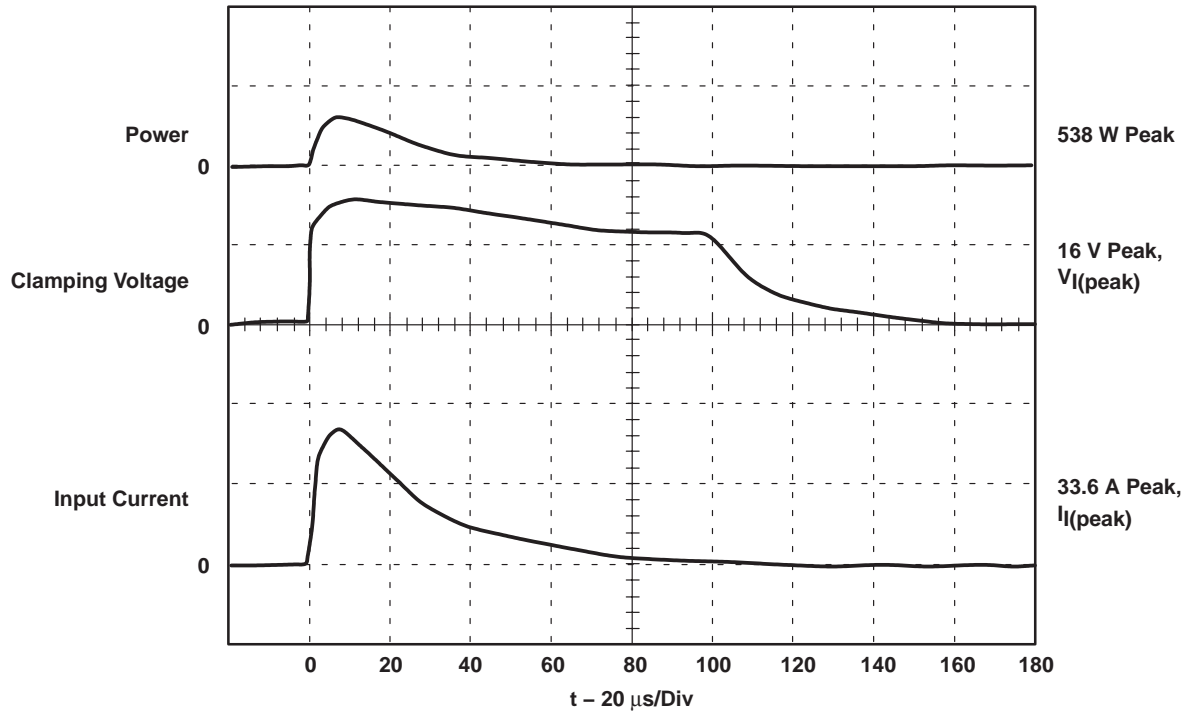
**Figure 16. Overvoltage-Stress Test Circuit**

An example waveform as seen by the 'LBC184 is shown in Figure 17. The bottom trace is current, the middle trace shows the clamping voltage of the device and the top trace is power as calculated from the voltage and current waveforms. This example shows a peak clamping voltage of 16 V, peak current of 33.6 A yielding an absorbed peak power of 538 W.

**NOTE**

A circuit reset may be required to ensure normal data communications following a transient noise pulse of greater than 250 W peak.

**APPLICATION INFORMATION**



**Figure 17. Typical Surge Waveform Measured At Terminals 5 and 7**

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[MAX22502EATC+T](#) [MAX3042BCSE+T](#) [SP3077EEN-L/TR](#) [MAX487ESA+TCBX](#) [MAX1483CUA+T](#) [MAX487CUA+T](#) [CA-IS3082W](#) [CA-](#)  
[IS3088W](#) [SP3074EEN-L/TR](#) [SP3483EN-L/TR](#) [NSI83085](#)