

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Product Summary

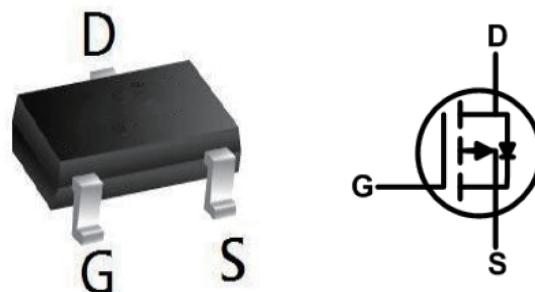
BVDSS	RDSON	ID
-20V	13mΩ	-9.0A

Description

The 20P09L is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and efficiency for most of the small power switching and load switch applications.

The 20P09L meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

SOT23-3L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-to-Source Voltage	-20	V
V _{GS}	Gate-to-Source Voltage	±12	V
I _D	Continuous Drain Current	-9	A
		-4	
I _{DM}	Pulsed Drain Current ⁽¹⁾	-66	A
E _{AS}	Single Pulsed Avalanche Energy ⁽²⁾	28.8	mJ
P _D	Power Dissipation	30	W
R _{θJA}	Thermal Resistance, Junction to Ambient ⁽³⁾	41.6	°C/W
T _J , T _{STG}	Junction & Storage Temperature Range	-55 to 150	°C

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D = -250\mu\text{A}$	-20	-	-	V
I_{DS}^{off}	Zero Gate Voltage Drain Current ($T_J = 25^\circ\text{C}$)	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}$	-	-	-1	μA
I_{DS}^{off}	Zero Gate Voltage Drain Current ($T_J = 100^\circ\text{C}$)	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}$	-	-	-100	μA
I_{GS}	Gate to Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 12\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-0.4	-0.65	-1	V
$R_{DS(on)}$	Static Drain-Source onResistance <small>note2</small>	$V_{GS} = -4.5\text{V}, I_D = -8\text{A}$	-	13	18	$\text{m}\Omega$
		$V_{GS} = -2.5\text{V}, I_D = -6\text{A}$	-	17	23	
g_f	Forward Transconductance ⁴	$V_{DS} = -4.5\text{V}, I_D = -8\text{A}$	-	36	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -10\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$	-	1630	-	pF
C_{oss}	Output Capacitance		-	211	-	pF
C_{rss}	Reverse Transfer Capacitance		-	187	-	pF
R_g	Gate Resistance	$f = 1.0\text{MHz}$	-	10	-	Ω
Q_g	Total Gate Charge	$V_{DS} = -10\text{V}, I_D = -8\text{A}, V_{GS} = -4.5\text{V}$	-	12	-	nC
Q_{gs}	Gate-Source Charge		-	1.8	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	3.2	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = -4.5\text{V}, V_{DD} = -10\text{V}, R_G = 3\Omega, I_D = -8\text{A}$	-	17	-	ns
t_r	Turn-on Rise Time		-	25.5	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	32	-	ns
t_f	Turn-off Fall Time		-	15	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	-40	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -8\text{A}$	-	-	-1.2	V

Note :

- 1.Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$.
- 2.The EAS data shows Max. rating . The test condition is $V_{DD} = -25\text{V}, V_{GS} = -10\text{V}, L = 0.1\text{mH}, I_{AS} = -24\text{A}$
- 3.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
- 4.The data tested by pulsed , pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$.
- 5.This value is guaranteed by design hence it is not included in the production test..

Typical Performance Characteristics

Figure 1: Output Characteristics

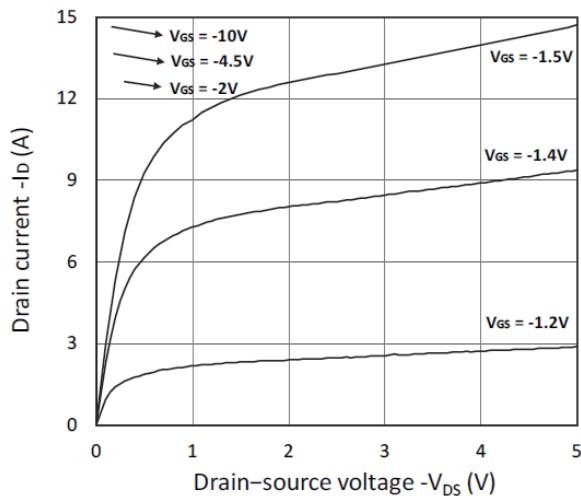


Figure 2: Transfer Characteristics

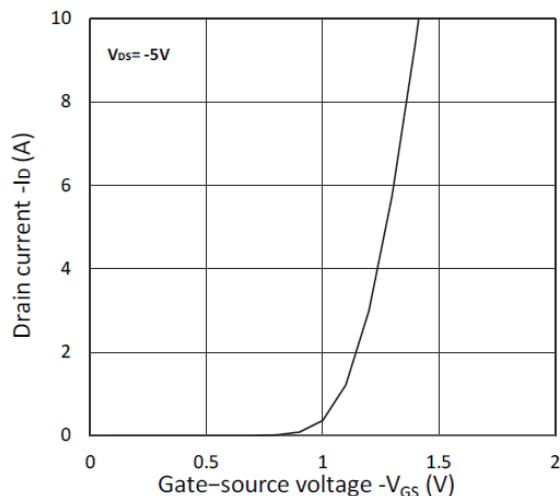


Figure 3: Forward Characteristics of Reverse Current

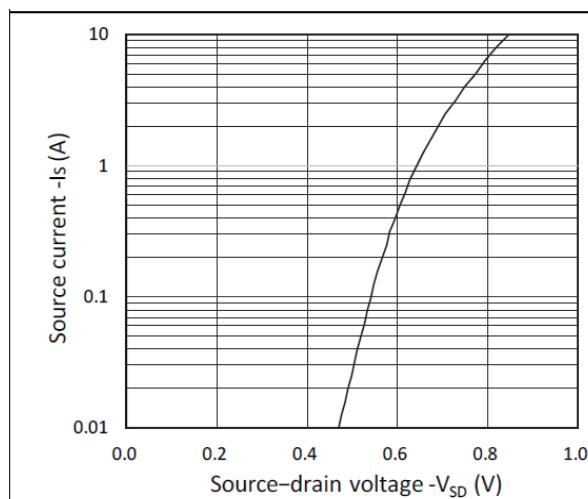


Figure 4: RDS(ON) vs. VGS

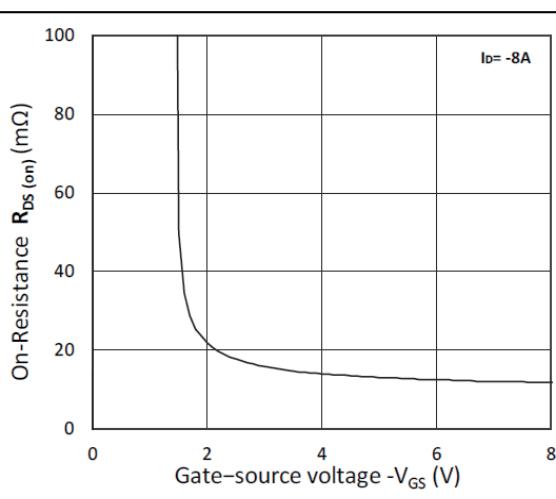


Figure 5: RDS(ON) vs. ID

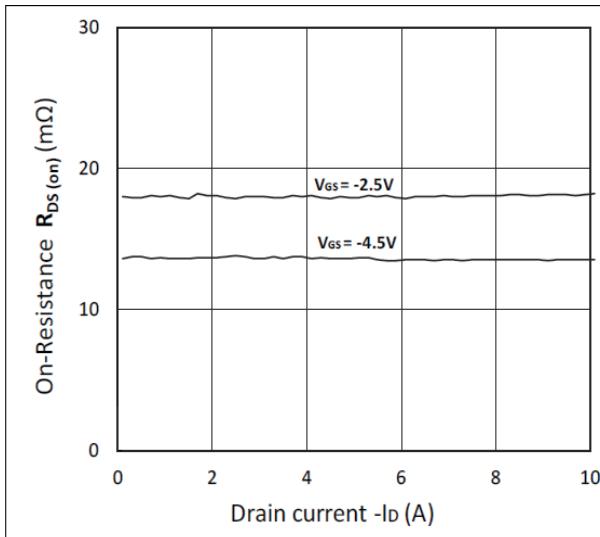
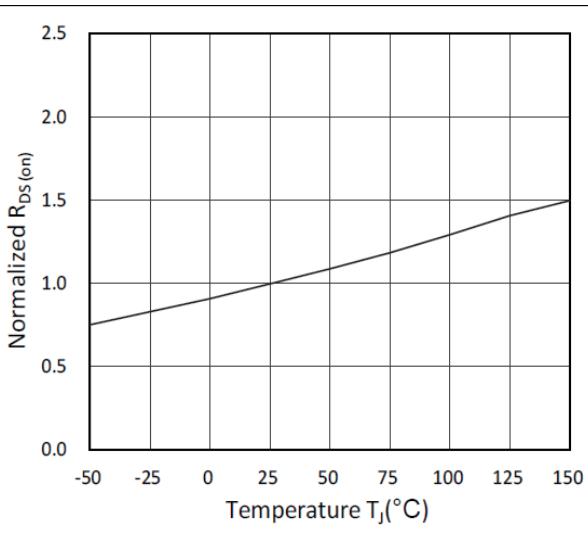


Figure 6: Normalized RDS(on) vs. Temperature



Typical Performance Characteristics

Figure 7: Capacitance Temperature

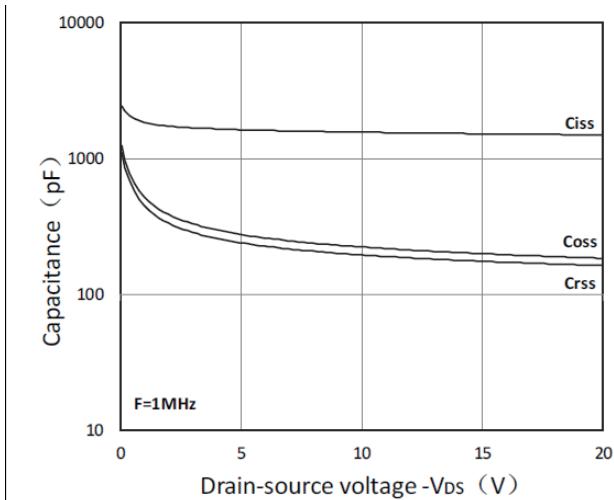


Figure 8: Gate Charge Characteristics

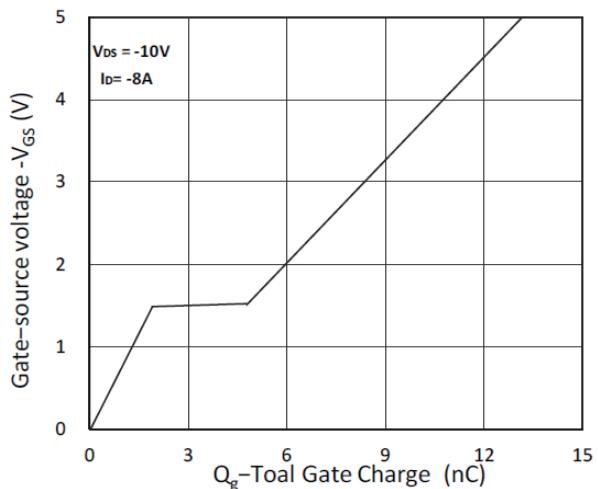


Figure 9: Power Dissipation Thermal Impedance

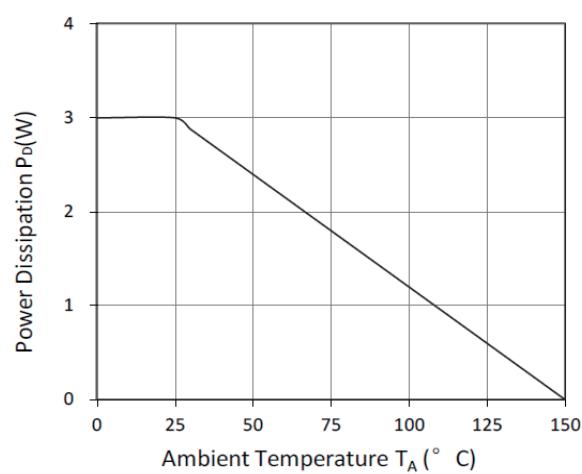


Figure 10: Power Dissipation

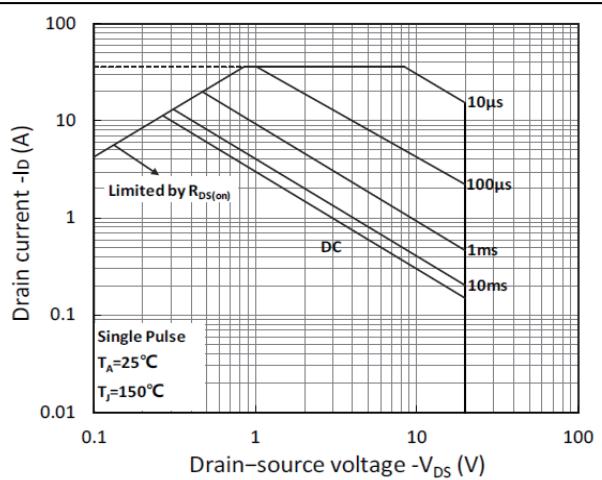
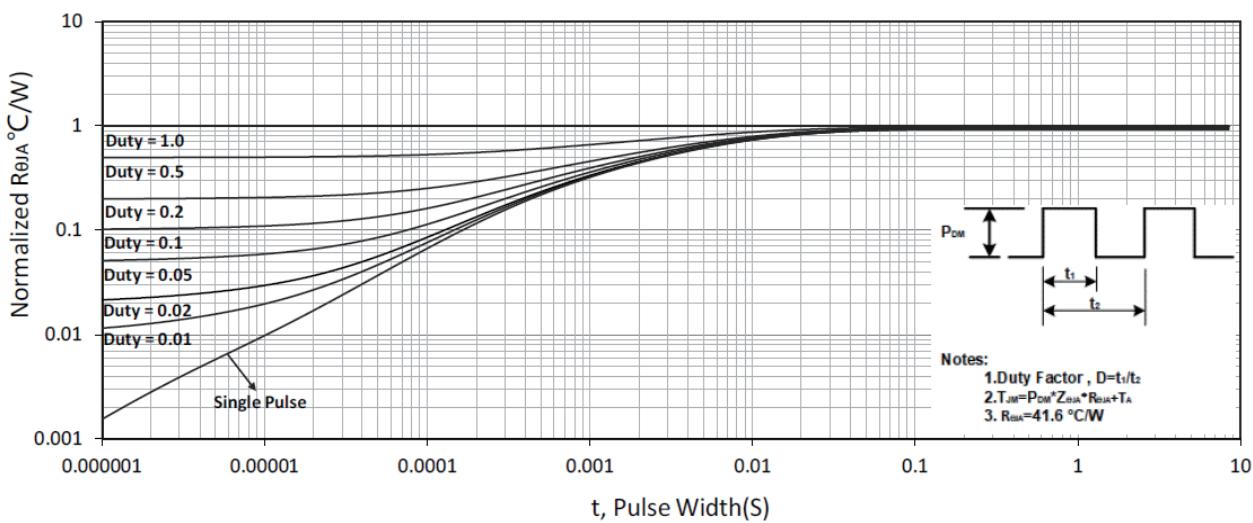
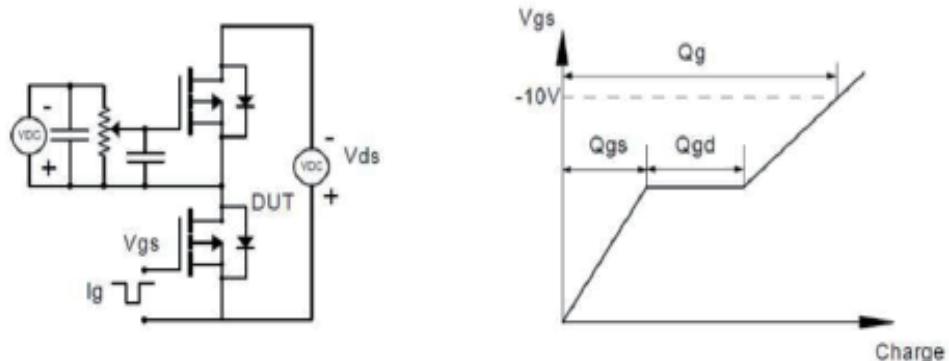


Figure 11: Safe Operating Area

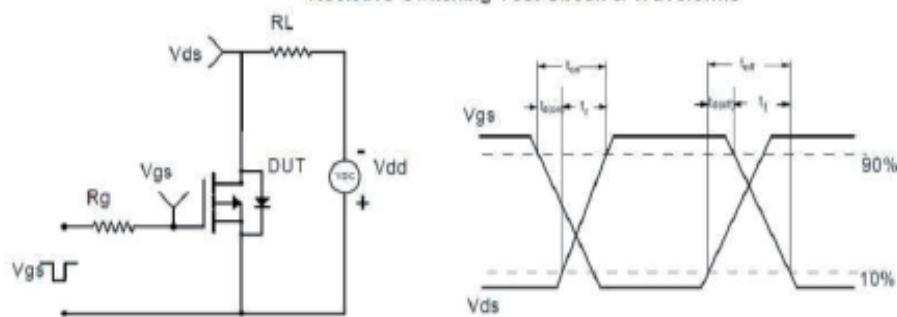


Test Circuit

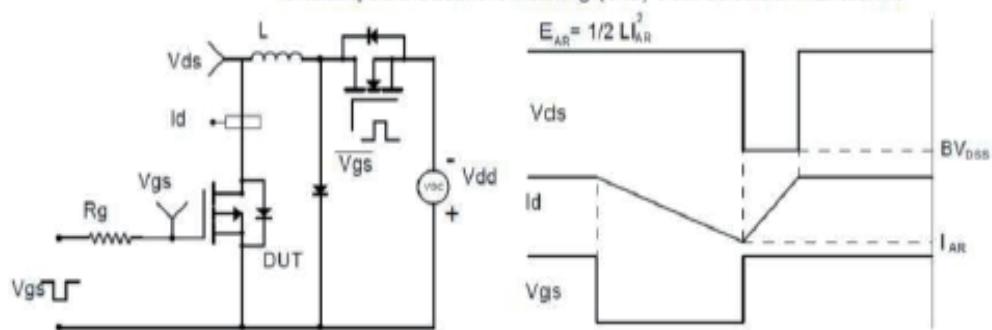
Gate Charge Test Circuit & Waveform



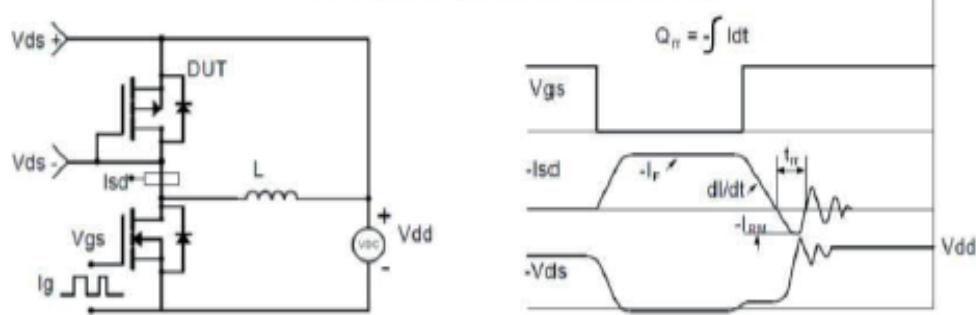
Resistive Switching Test Circuit & Waveforms



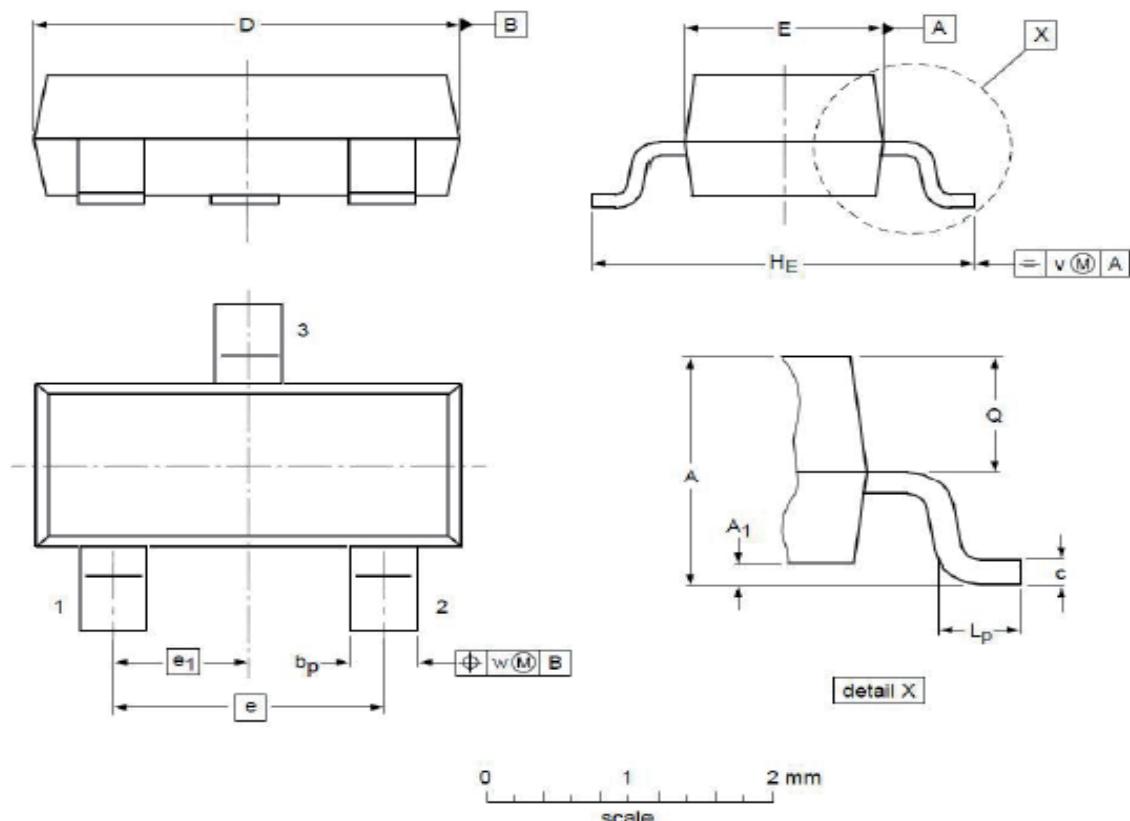
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



SOT-23-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.05	1.25	0.041	0.049
A ₁	0.00	0.10	0.000	0.004
A ₂	1.05	1.15	0.041	0.045
b	0.30	0.50	0.012	0.02
c	0.10	0.20	0.004	0.008
D	2.82	3.02	0.111	0.119
E	1.50	1.70	0.059	0.067
E ₁	2.65	2.95	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

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