

Features

- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Product Summary

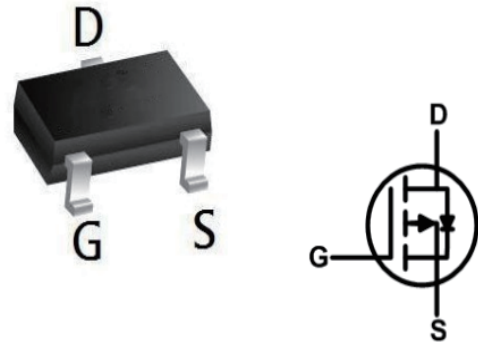
RoHS

BVDSS	RDSON	ID
-30V	48mΩ	-4A

Description

THE 3401 is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and efficiency for most of the small power switching and load switch applications. The 3401 meet the RoHS and Green Product requireme n t with full function reliability approved.

SOT23 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-to-Source Voltage	-30	V
$V_{GS}$	Gate-to-Source Voltage	±12	V
$I_D$	Continuous Drain Current	$T_A = 25^\circ\text{C}$	-4
		$T_A = 100^\circ\text{C}$	-3
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	-16	A
$P_D$	Power Dissipation	$T_A = 25^\circ\text{C}$	1.2
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient <sup>(2)</sup>	108	°C/W
$T_J, T_{STG}$	Junction & Storage Temperature Range	-55 to 150	°C

**Electrical Characteristics ( $T_J = 25^\circ\text{C}$  unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_b = -250\mu\text{A}, V_{GS} = 0\text{V}$	-30	-	-	V
$I_{BSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 12\text{V}$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_b = -250\mu\text{A}$	-0.6	-0.95	-1.3	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance <sup>(3)</sup>	$V_{GS} = -10\text{V}, I_b = -4\text{A}$	-	48	62	$\text{m}\Omega$
		$V_{GS} = -4.5\text{V}, I_b = -3\text{A}$	-	56	73	$\text{m}\Omega$
		$V_{GS} = -2.5\text{V}, I_b = -3\text{A}$	-	75	98	$\text{m}\Omega$
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = -15\text{V}, f = 1\text{MHz}$	-	553	-	pF
$C_{oss}$	Output Capacitance		-	57	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	35	-	pF
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ to } -4.5\text{V}, V_{DS} = -15\text{V}, I_b = -3\text{A}$	-	6.5	-	nC
$Q_{gs}$	Gate Source Charge		-	1.4	-	nC
$Q_{gd}$	Gate Drain ("Miller") Charge		-	1.7	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = -4.5\text{V}, V_{DD} = -15\text{V}, I_b = -3\text{A}, R_{GEN} = 3\Omega$	-	10	-	ns
$t_r$	Turn-On Rise Time		-	86	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	150	-	ns
$t_f$	Turn-Off Fall Time		-	357	-	ns
<b>Drain-Source Diode Characteristics and Max Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	-4	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-16	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -4\text{A}$	-	-	-1.2	V
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F = -3\text{A}, di/dt = 80\text{A}/\mu\text{s}$	-	36	-	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge		-	5	-	nC

**Note :**

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2.  $R_{\theta JA}$  is measured with the device mounted on a 1inch<sup>2</sup> pad of 2oz copper FR4 PCB
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 0.5\%$ .

P-Channel Typical Performance Characteristics

Figure 1: Typical Output Characteristics

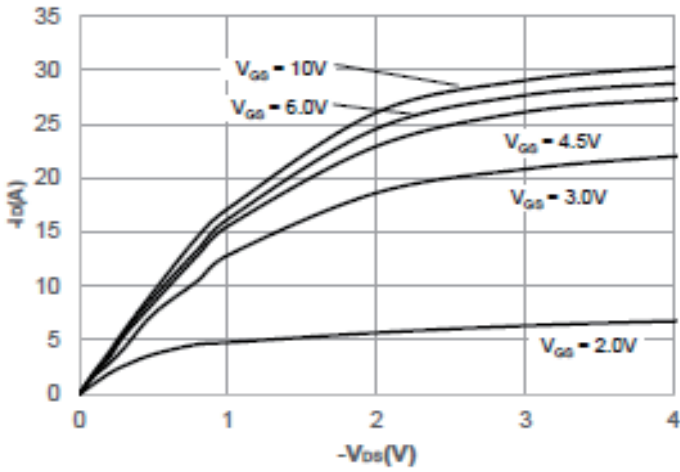


Figure 2: Transfer Characteristics

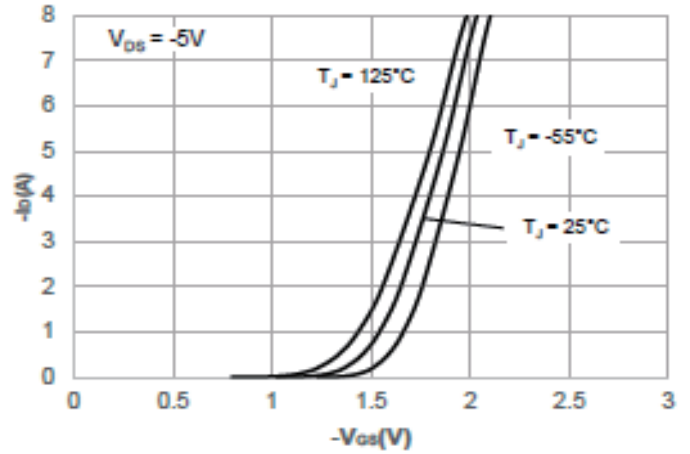


Figure 3: On-resistance vs. Drain Current

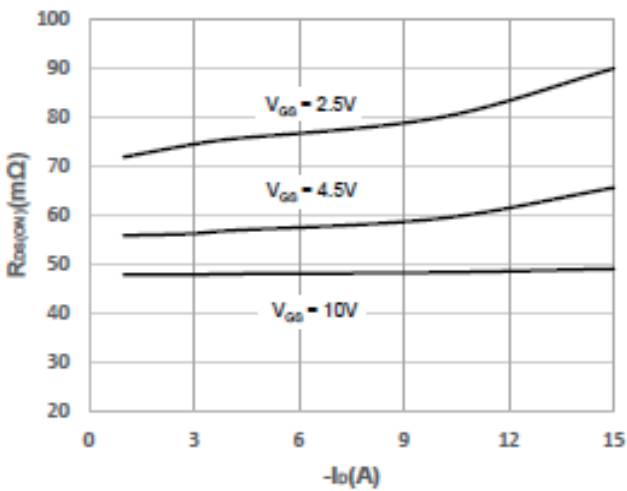


Figure 4: Body Diode Characteristics

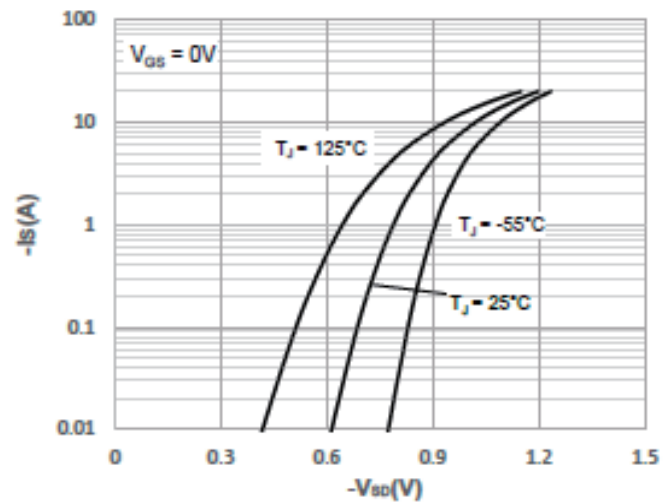


Figure 5: Gate Charge Characteristics

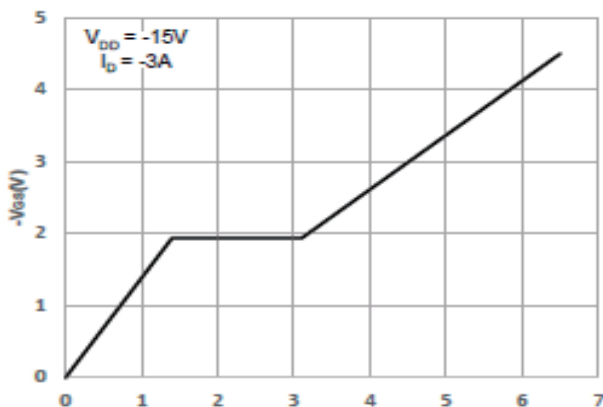
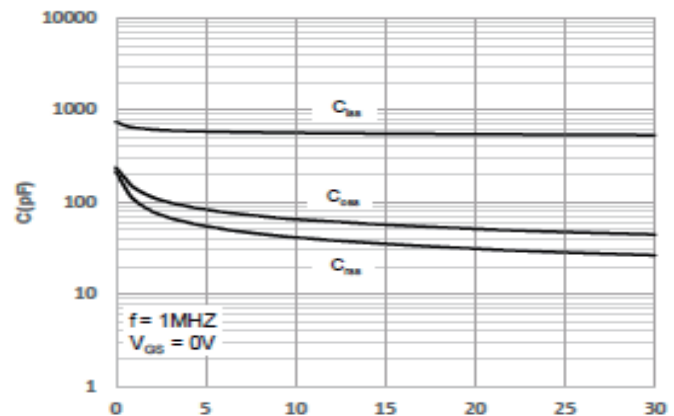


Figure 6: Capacitance Characteristics



P-Channel Typical Performance Characteristics

Figure7: Normalized Breakdown voltage vs. Junction Temperature

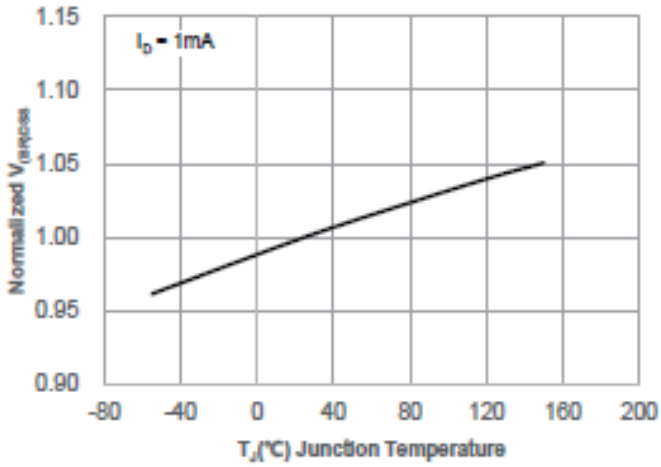


Figure 8: Normalized on Resistance vs. Junction Temperature

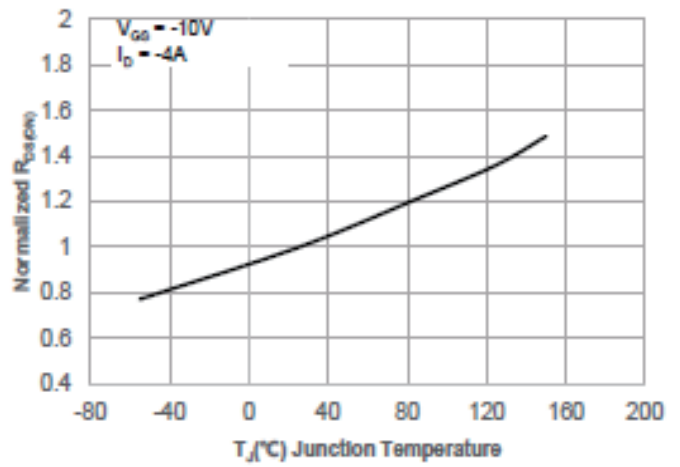


Figure9: Maximum Safe Operating Area

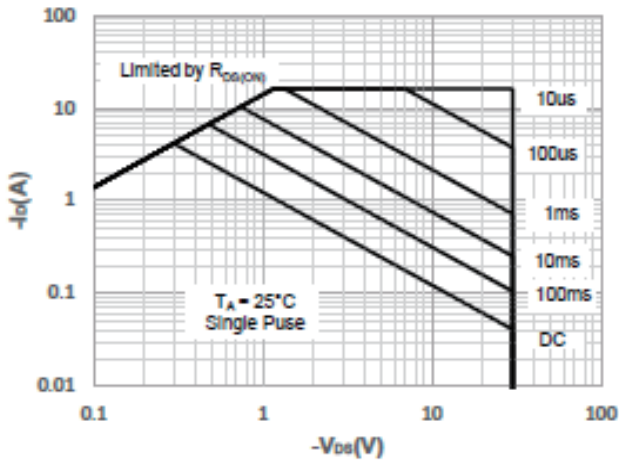


Figure10: Maximum Continuous Drain Current vs. Ambient Temperature

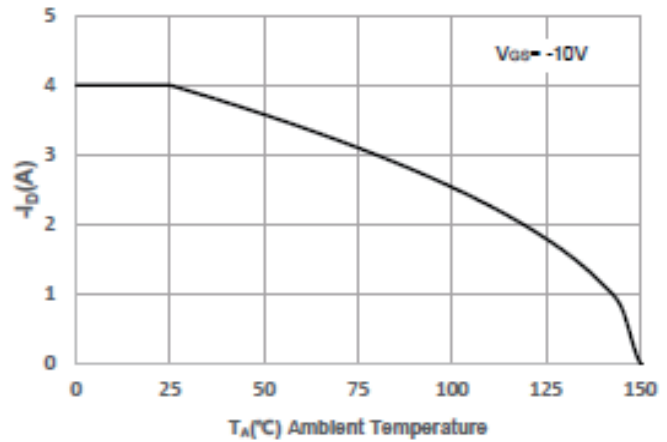


Figure11: Normalized Maximum Transient Thermal Impedance

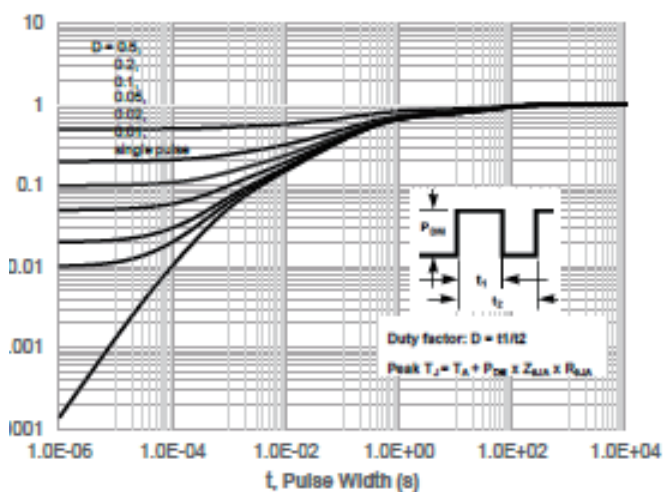
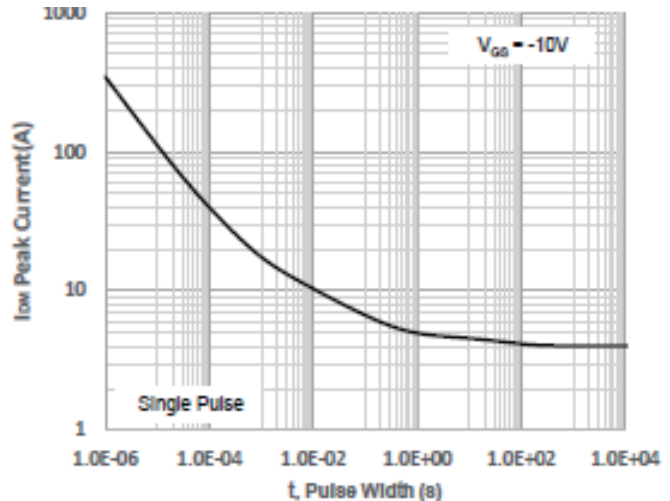


Figure 11: Peak Current Capacity



Test Circuit

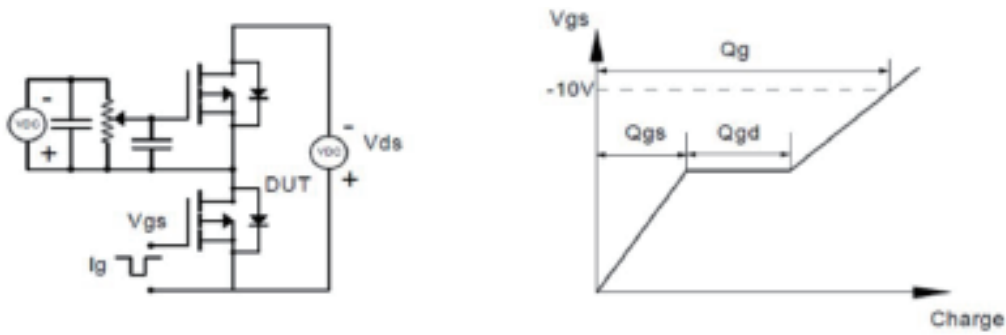


Figure 1: Gate Charge Test Circuit & Waveform

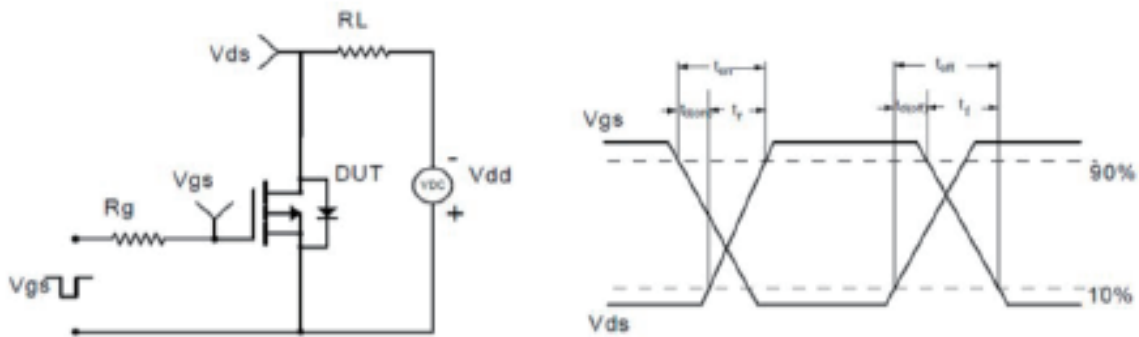


Figure 2: Resistive Switching Test Circuit & Waveform

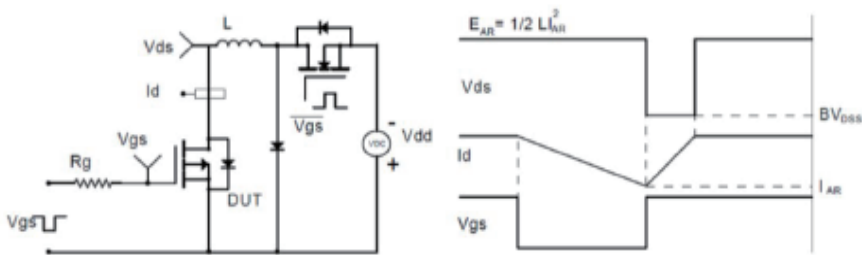


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

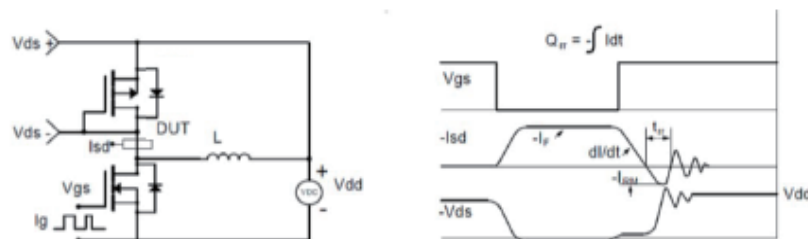


Figure 4: Diode Recovery Test Circuit & Waveform



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