

- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology
- ★ 100% EAS Guaranteed

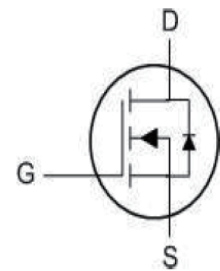
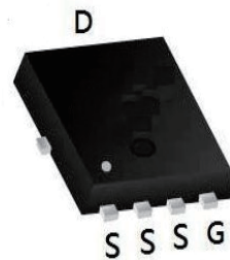
**Product Summary**

BVDSS	RDS(on)	ID
30V	3.8mΩ	80A

**Description**

The 80N03F is the high cell density trenched N-ch MOSFETs, which provide excellent RDS(on) and gate charge for most of the synchronous buck converter applications.

The 80N03F meet the RoHS and Green Product, requirement 100% EAS guaranteed with full function reliability approved.

**PRPAK5\*6 Pin Configuration**

**Absolute Maximum Ratings**

Symbol	Parameter	Limit	Unit
V <sub>DS</sub>	Drain-Source Voltage	30	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous	80	A
I <sub>D</sub> (100°C)	Drain Current-Continuous(T <sub>C</sub> =100°C)	46	A
I <sub>DM</sub>	Pulsed Drain Current <sup>(Note 1)</sup>	200	A
P <sub>D</sub>	Maximum Power Dissipation	65	W
	Derating factor	0.52	W/°C
EAS	Single pulse avalanche energy <sup>(Note 5)</sup>	150	mJ
T <sub>J</sub> ,T <sub>STG</sub>	Operating Junction and Storage	-55 To 150	°C

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Case(Note <sup>2</sup> )	-	0.56	°C/W

**Electrical Characteristics ( $T_J = 25^\circ\text{C}$  unless otherwise specified)**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_b=250\mu A$	30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=30V, V_{GS}=0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> (Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_b=250\mu A$	1	1.6	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=20A$	-	3.8	5.0	m $\Omega$
		$V_{GS}=4.5V, I_D=20A$	-	6.9	11.0	
$g_{FS}$	Forward Transconductance	$V_{DS}=5V, I_b=20A$	20	-	-	S
<b>Dynamic Characteristics</b> (Note 4)						
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V,$ $F=1.0MHz$	-	1400	-	PF
$C_{oss}$	Output Capacitance		-	205	-	PF
$C_{rss}$	Reverse Transfer Capacitance		-	177	-	PF
<b>Switching Characteristics</b> (Note 4)						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15V, I_b=20A$ $V_{GS}=10V, R_{GEN}=6.0\Omega$	-	9	-	nS
$t_r$	Turn-on Rise Time		-	8	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	28	-	nS
$t_f$	Turn-Off Fall Time		-	5	-	nS
$Q_g$	Total Gate Charge		-	32.3	-	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=15V, I_b=20A, V_{GS}=10V$	-	4.9	-	nC
$Q_{gd}$	Gate-Drain Charge		-	6.9	-	nC
<b>Drain-Source Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage (Note 3)	$V_{GS}=0V, I_s=20A$	-	0.85	1.2	V
$I_s$	Diode Forward Current (Note 2)		-	-	65	A
$t_{rr}$	Reverse Recovery Time	$T_J = 25^\circ\text{C}, I_F = 20A$	-	-	27	nS
$Q_{rr}$	Reverse Recovery Charge	$di/dt = 100A/\mu s$ (Note 3)	-	-	20	nC
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Note :**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^\circ\text{C}, V_{DD}=15V, V_G=10V, L=0.5mH, R_g=25\Omega$ .

Typical Electrical and Thermal Characteristics (Curves)

Figure 1: Output Characteristics

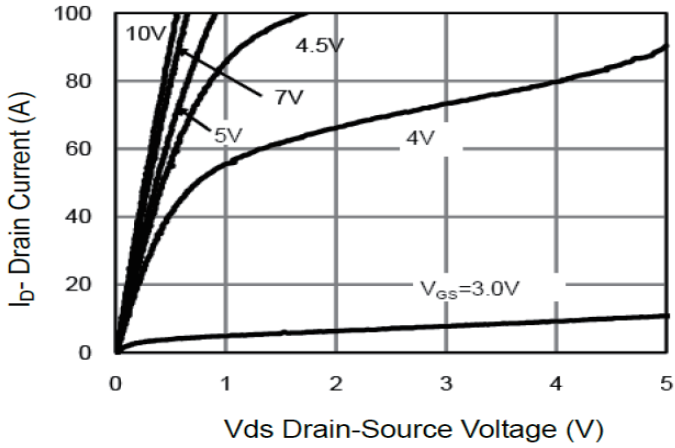


Figure 4:  $R_{DS(on)}$ -Junction Temperature

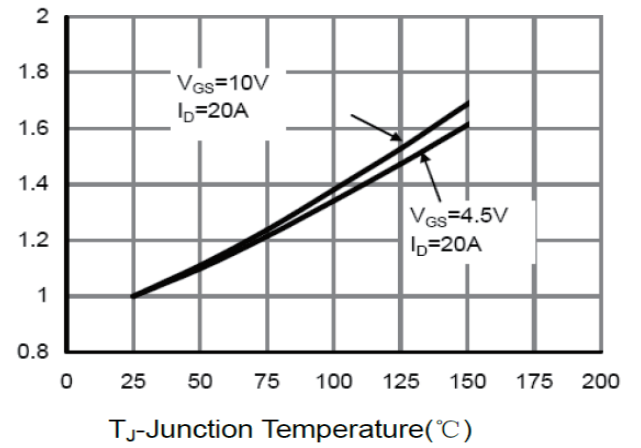


Figure 2: Transfer Characteristics

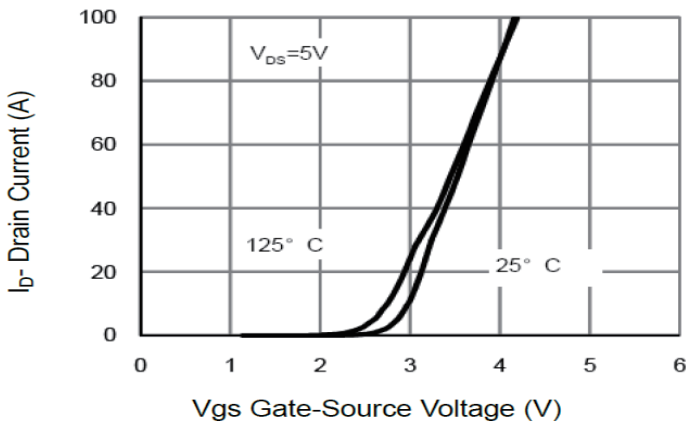


Figure 5: Gate Charge

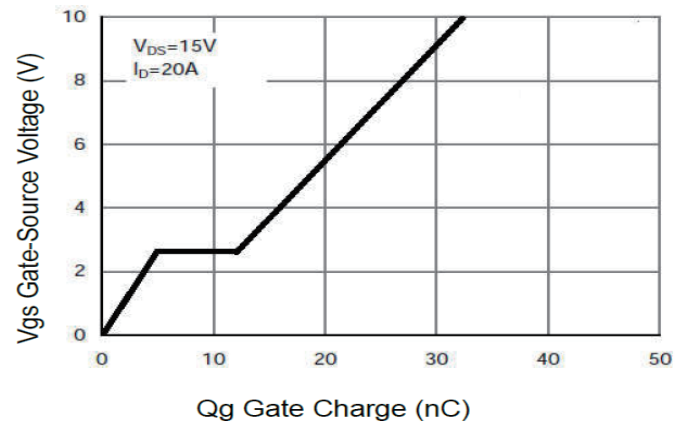


Figure 3:  $R_{DS(on)}$ - Drain Current

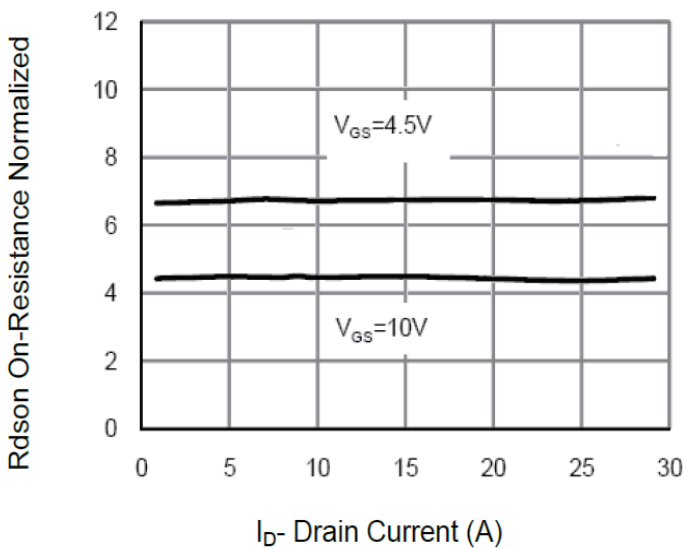
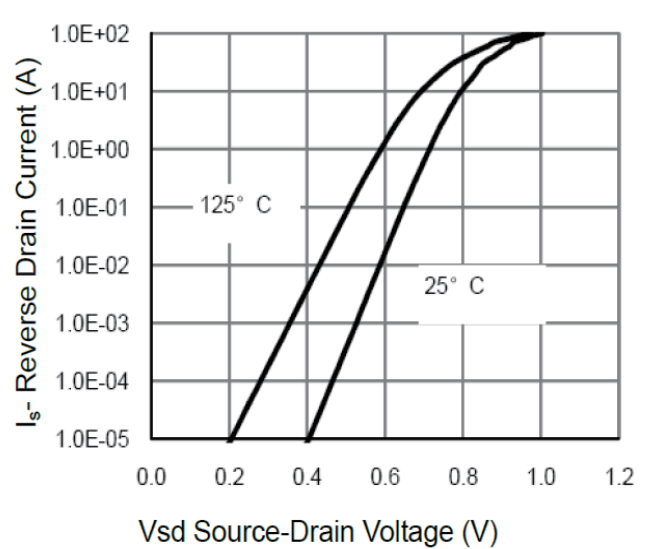


Figure 6: Source- Drain Diode Forward



Typical Performance Characteristics

Figure 7: Capacitance vs Vds

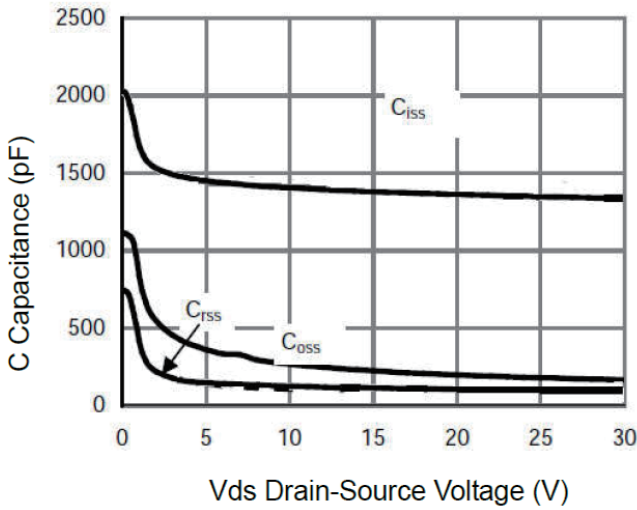


Figure 9: BVDS vs Junction Temperature

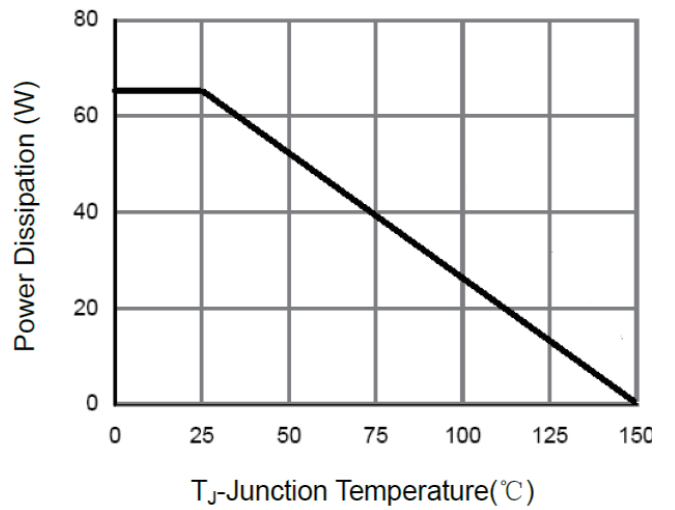


Figure 8: Safe Operation Area

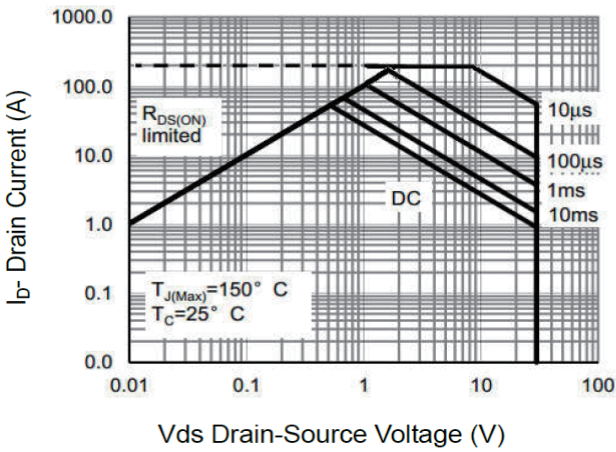


Figure 10: VGS(th) vs Junction Temperature

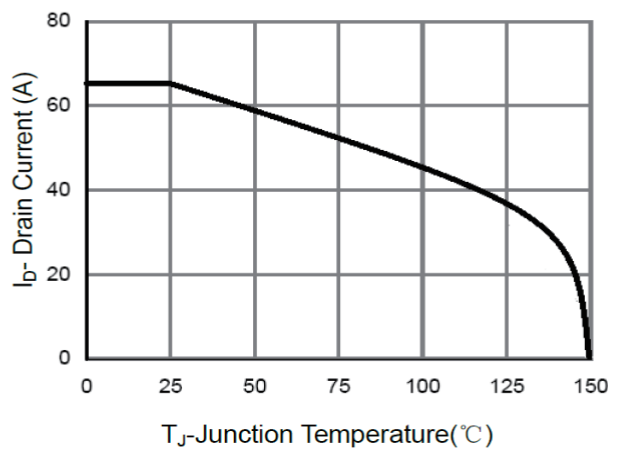
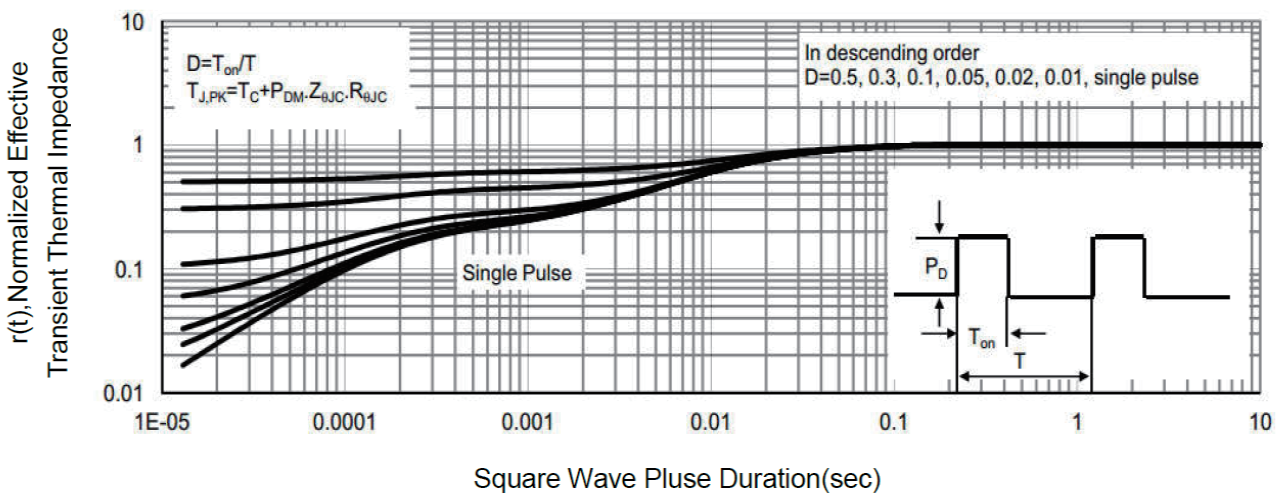


Figure 11: Normalized Maximum Transient Thermal Impedance



Test Circuit

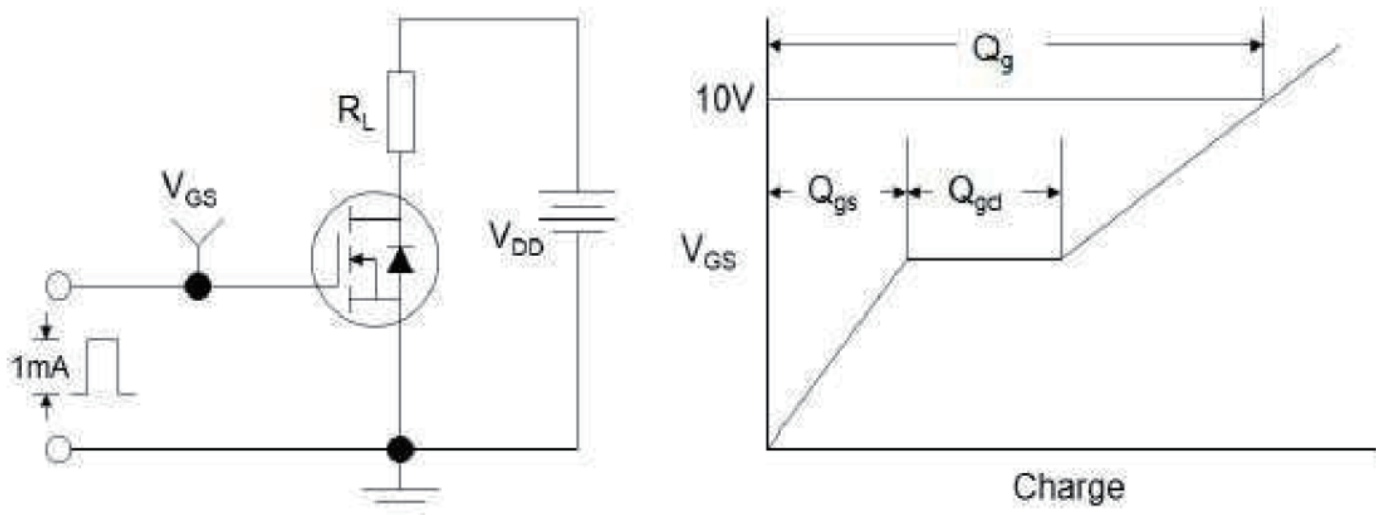


Figure 1: Gate Charge Test Circuit & Waveform

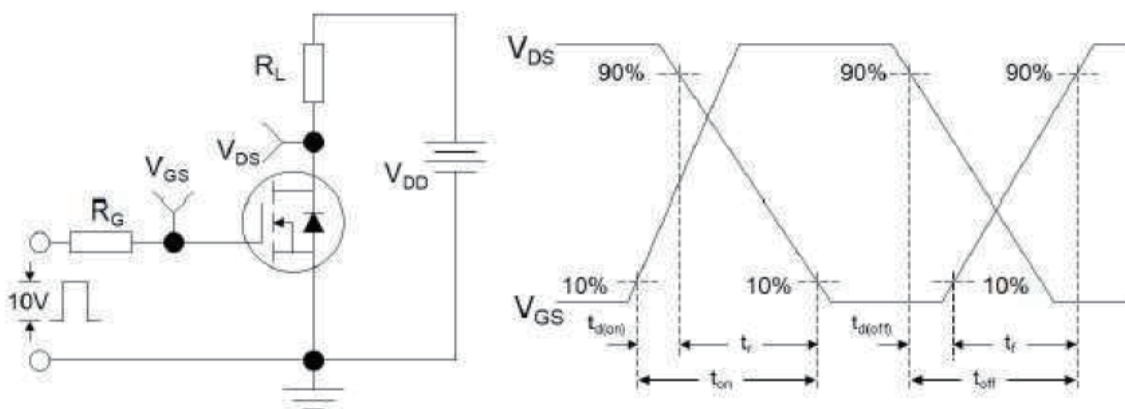


Figure 2: Resistive Switching Test Circuit & Waveforms

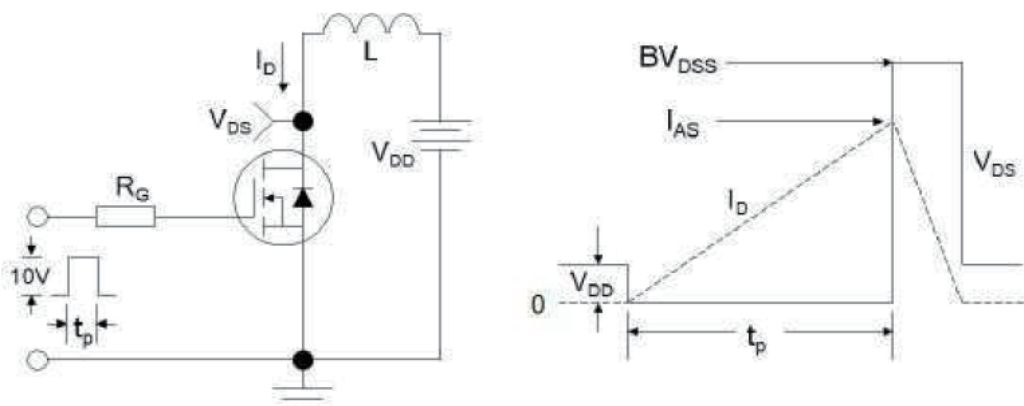
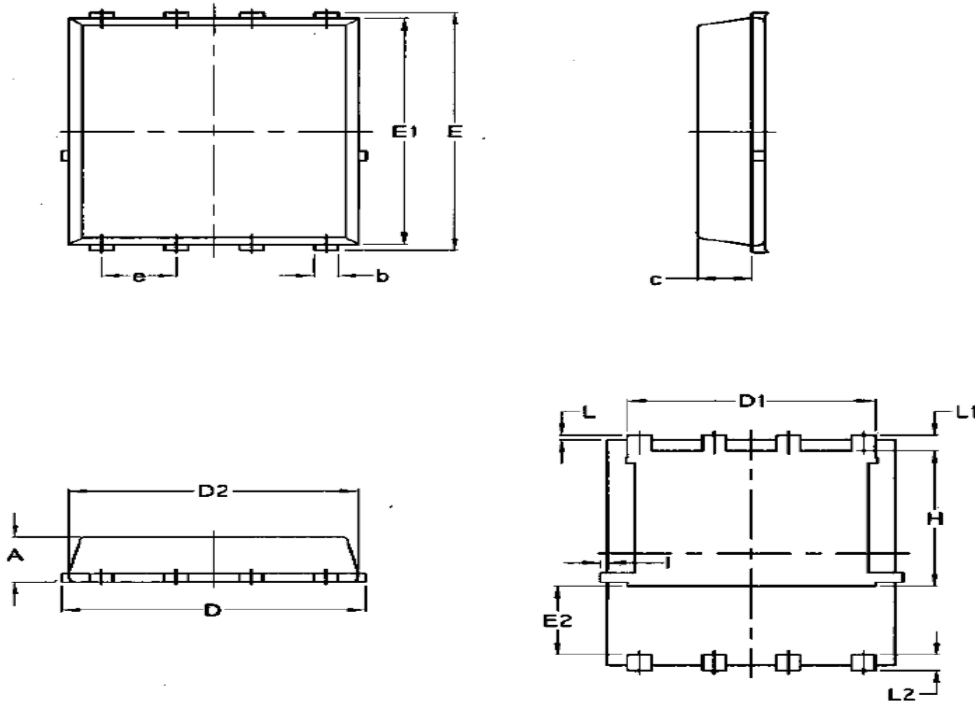


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data-DFN5\*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.097	0.0324	0.082
D	4.8	5.4	0.189	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.8	5	0.189	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.6	/	0.063	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.002	0.0098
L1	0.38	0.5	0.015	0.0197
L2	0.38	0.5	0.015	0.0197
H	3.3	3.5	0.1299	0.1378
I	/	0.18	/	0.007

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