

Features

- ★ Split Gate Trench MOSFET technology
- ★ Excellent package for heat dissipation
- ★ High density cell design for low RDS(ON)

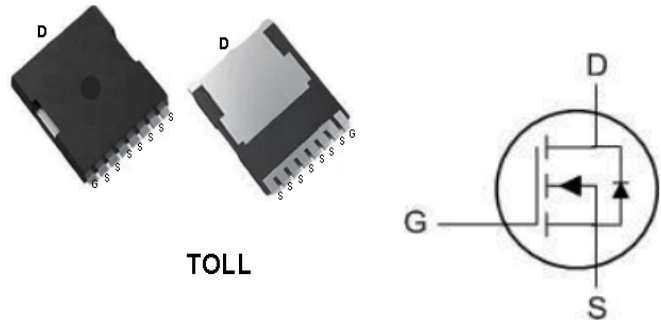
Product Summary

BVDSS	RDS(ON)	ID
40V	1.0mΩ	300A

Applications

- ★ DC-DC Converters
- ★ Power management functions
- ★ Power management functions

TOLL Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
I_b	Drain Current (Silicon limited)	300	A
$I_{D@Tc=25^{\circ}C}$	Continuous Drain Current ₁	200	A
$I_{D@Tc=100^{\circ}C}$	Continuous Drain Current ₁	82	A
I_{DM}	Pulsed Drain Current ₂	690	A
EAS	Single Pulse Avalanche Energy ³	500	mJ
P_D	Total Power Dissipation ⁴	220	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	35	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.0	°C/W

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
	TOLL-8L				20000	

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
Static Parameter						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_b = 250\mu A$	40	48	---	V
I_{BSS}	Zero Gate Voltage Drain Current	$V_{DS} = 40V, V_{GS} = 0V$	---	---	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	---	---	± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_b = 250\mu A$	1.2	1.8	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10V, I_b = 20A$	---	1.0	1.4	m Ω
		$V_{GS} = 4.5V, I_b = 20A$	---	1.6	2.3	
R_g	Gate Resistance	$V_{GS} = 0V, V_{DS} \text{ Open}, f = 1MHz$	---	2.7	---	Ω
I_S	Maximum Body-Diode Continuous Current		---	---	300	A
Dynamic Parameters						
C_{iss}	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V, f = 300KHz$	---	8300	---	pF
C_{oss}	Output Capacitance		---	1510	---	
C_{rss}	Reverse Transfer Capacitance		---	130	---	
Switching Parameters						
Q_g	Total Gate Charge	$V_{GS} = 10V, V_{DS} = 32V, I_b = 20A$	---	127	---	nC
Q_{gs}	Gate-Source Charge		---	35	---	
Q_{gd}	Gate-Drain Charge		---	26	---	
Q_{rr}	Reverse Recovery Charge	$I_f = 25A, di/dt = 100A/\mu s$	---	163	---	ns
t_{rr}	Reverse Recovery Time		---	100	---	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 10V, V_{DD} = 20V, I_b = 25A$ $R_{GEN} = 2\Omega$	---	22.5	---	ns
t_r	Turn-on Rise Time		---	6.7	---	
$t_{d(off)}$	Turn-off Delay Time		---	80.3	---	
t_f	Turn-off fall Time		---	26.9	---	

Notes:

1. A. The maximum current rating is package limited.
2. Repetitive rating; pulse width limited by max. junction temperature.
3. $V_{DD} = 32V, R_G = 25\Omega, L = 0.5mH$, starting $T_J = 25^\circ\text{C}$.
4. PD is based on max. junction temperature, using junction-case thermal resistance.
5. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a = 25^\circ\text{C}$.

Typical Electrical and Thermal Characteristics (Curves)

Figure 1: Output Characteristics

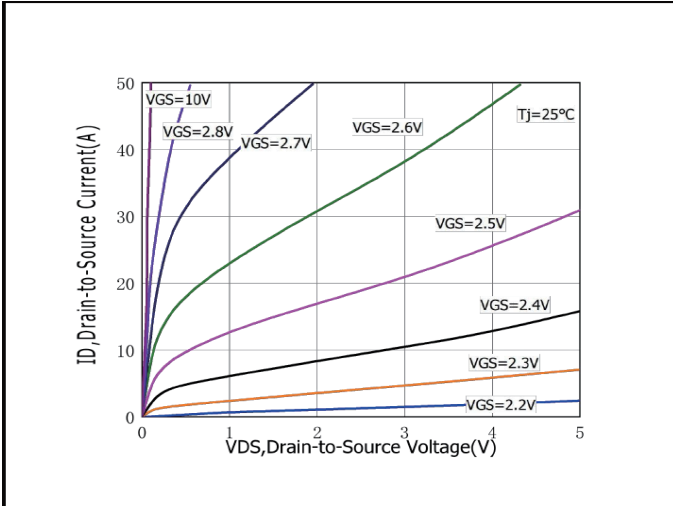


Figure 2: Typical Gate Charge vs Gate-to-Source Voltage

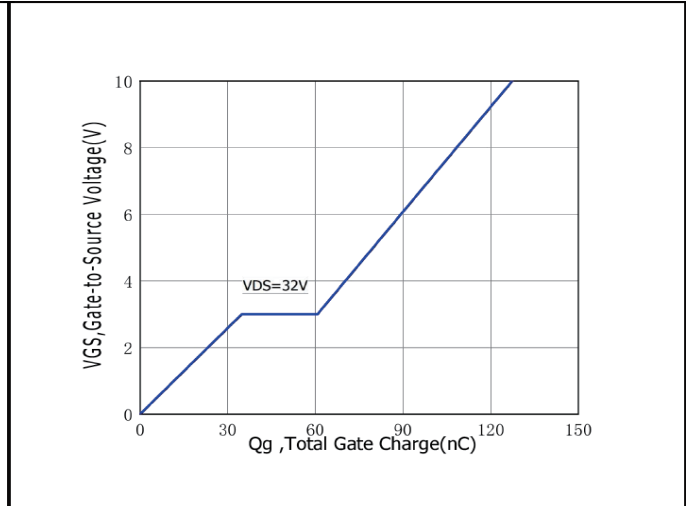


Figure 3: Typical Body Diode Transfer Characteristic

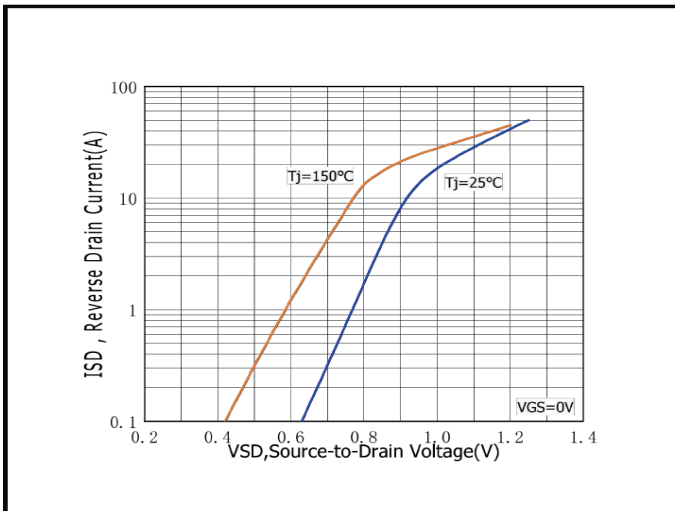


Figure 4: Typical Capacitance vs Drain-to-Source Voltage

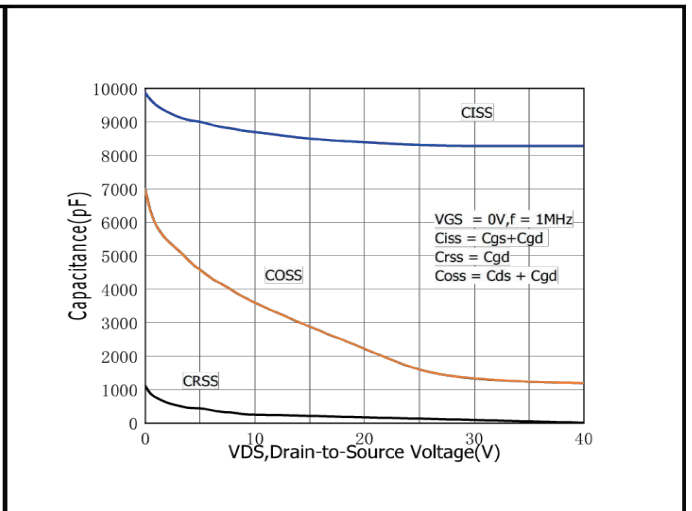


Figure 5: Typical Breakdown Voltage vs Junction Temperature

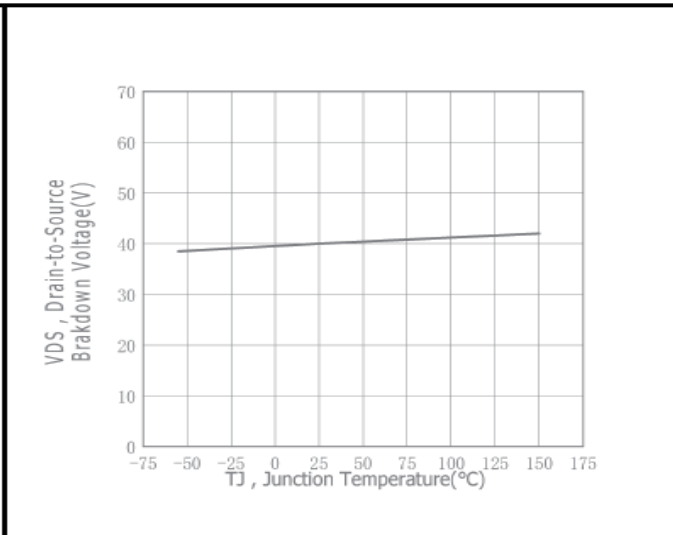
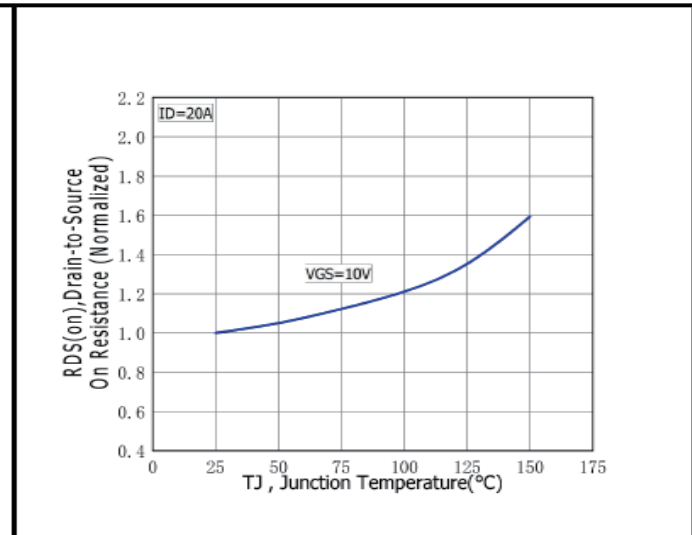


Figure 6: Typical Drain-to-Source On Resistance vs Junction Temperature



Typical Performance Characteristics

Figure 7: Maximum Forward Bias Safe Operating Area

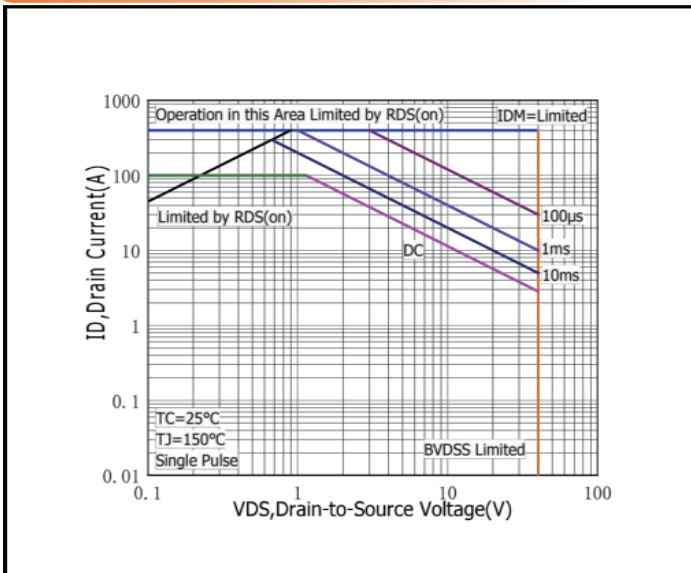


Figure 8: Typical Drain to Source ON Resistance vs Drain Current

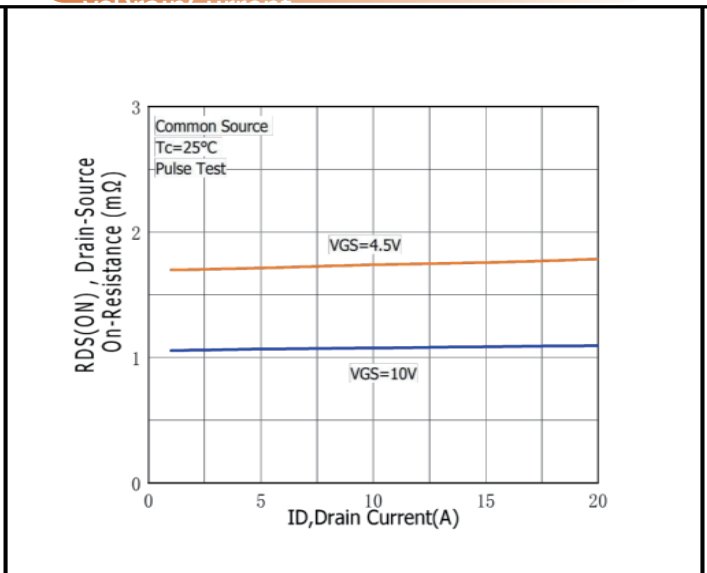


Figure 9: Maximum EAS vs Channel Temperature

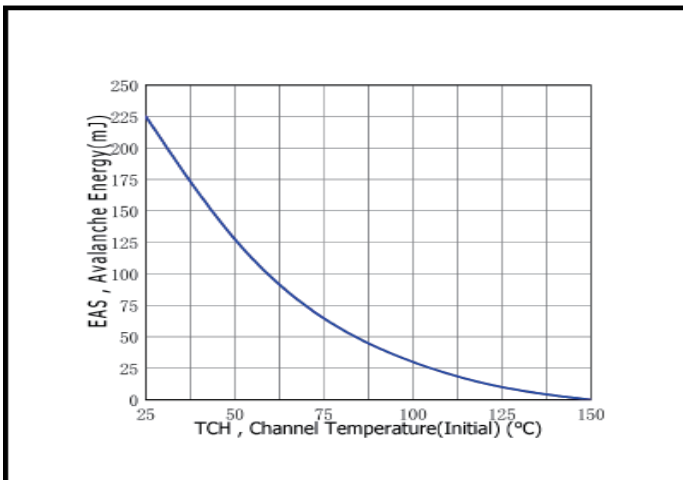


Figure 10: Typical Threshold Voltage vs Case Temperature

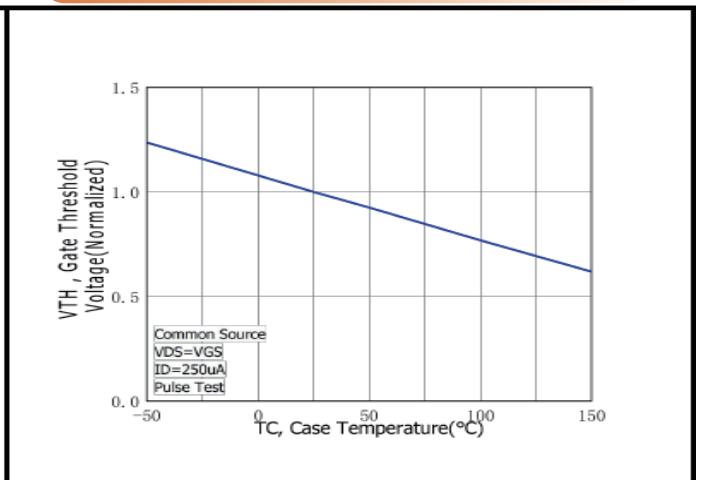


Figure 11: Typical Transfer Characteristics

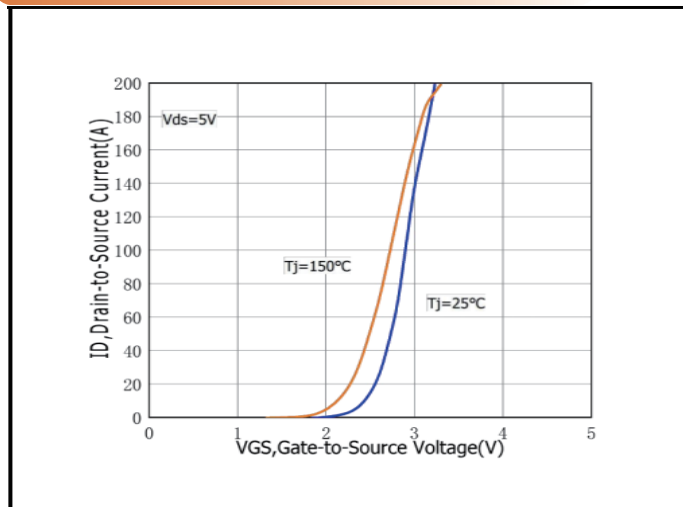
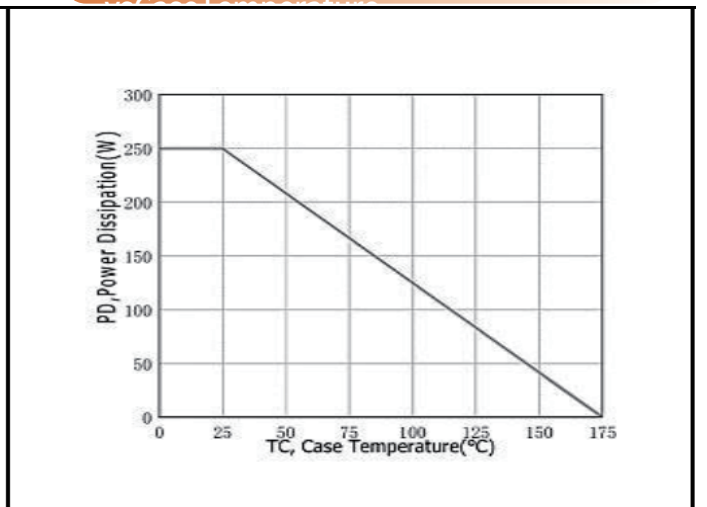


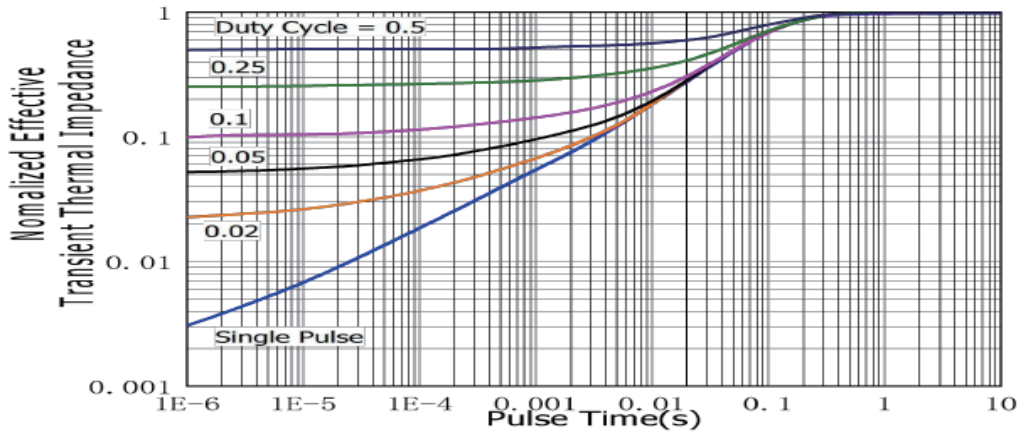
Figure 12: Maximum Power Dissipation vs Case Temperature





Typical Performance Characteristics

Figure 13: Maximum Effective Thermal Impedance



Test circuits and waveforms

Figure A: Gate Charge Test Circuit & Waveforms

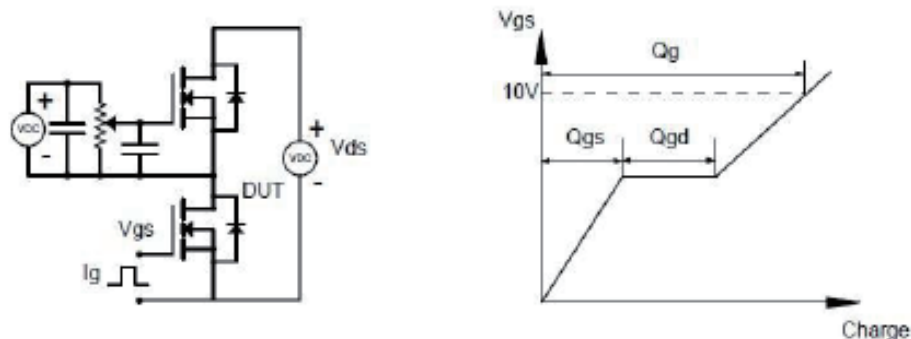


Figure B: Resistive Switching Test Circuit & Waveforms

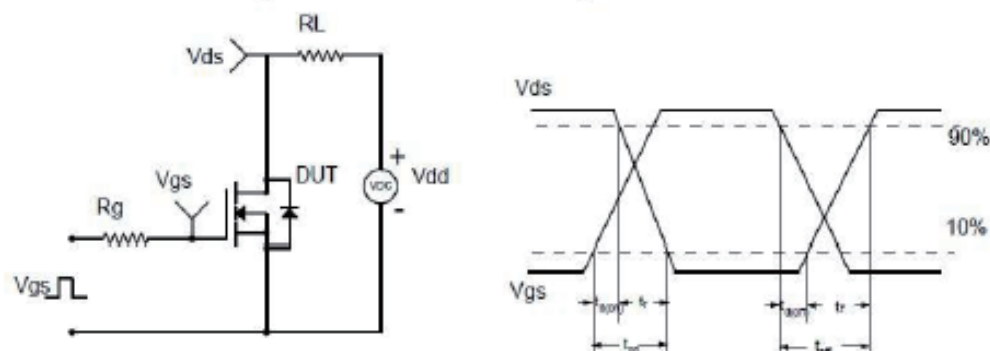


Figure C: Unclamped Inductive Switching (UIS) Test

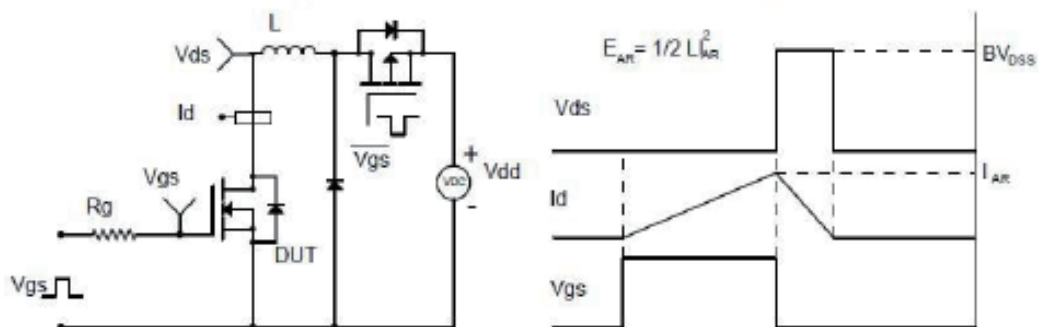
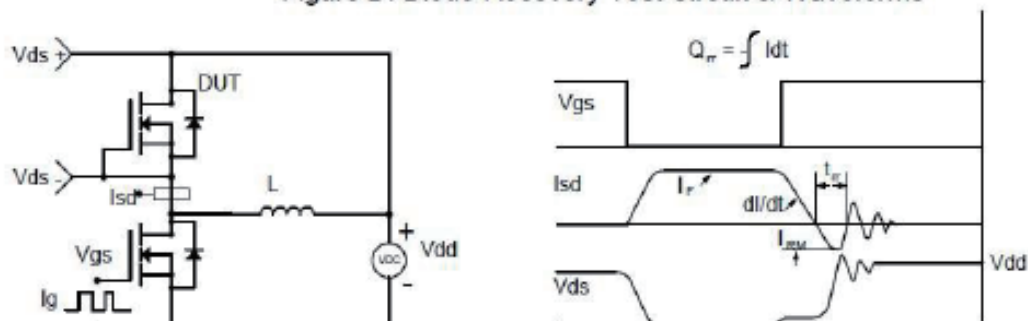
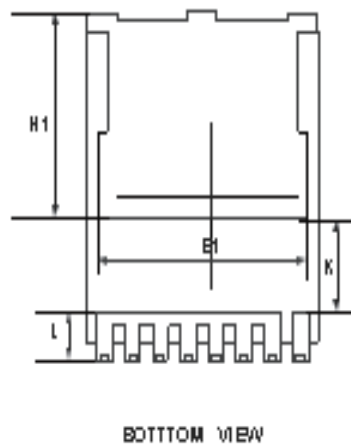
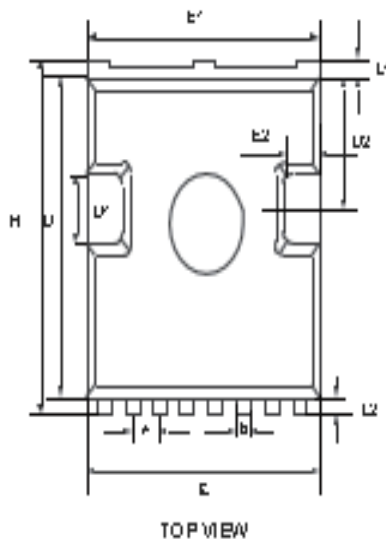


Figure D: Diode Recovery Test Circuit & Waveforms



Mechanical Dimensions for TOLL-8L



COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	2.20	2.40
b	0.60	0.90
b1	9.70	9.90
c	0.40	0.60
D	10.20	10.60
D1	3.10	3.50
D2	4.45	4.75
E	9.70	10.10
E1	7.80 BSC	
E2	0.50	0.70
e	1.200 BSC	
H	11.45	11.90
H1	6.75 BSC	
K	3.10 REF	
L	1.70	2.10
L1	0.60	0.80
L2	0.50	0.70
θ	10° REF	

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