

Features

- ★ Split Gate Trench MOSFET technology
- ★ Excellent package for heat dissipation
- ★ High density cell design for low RDS(ON)

Product Summary

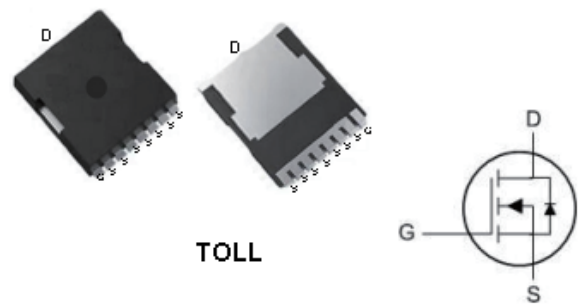
RoHS

BVDSS	RDSON	ID
80V	1.05mΩ	400A

Description

- ★ DC-DC Converters
- ★ Power management functions
- ★ Synchronous-rectification applications

TOLL Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Max.	Unit	
V <sub>DSS</sub>	Drain-Source Voltage	80	V	
V <sub>GSS</sub>	Gate-Source Voltage	±20	V	
I <sub>D</sub>	Continuous Drain Current	T <sub>C</sub> = 25°C	400	A
		T <sub>C</sub> = 100°C	253	A
I <sub>DM</sub>	Pulsed Drain Current <sup>note1</sup>	1600	A	
E <sub>AS</sub>	Single Pulsed Avalanche Energy <sup>note2</sup>	1280	mJ	
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25°C	468.8	W
R <sub>θJA</sub>	Thermal Resistance from Junction-to-Ambient <sup>3</sup>	39	°C/W	
R <sub>θJC</sub>	Thermal Resistance, Junction to Case	2.5	°C/W	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +175	°C	

**Electrical Characteristics ( $T_J = 25^\circ\text{C}$  unless otherwise specified)**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
<b>Static Characteristics</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	80	-	-	V
$I_{GSS}$	Gate-body Leakage current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$T_J = 25^\circ\text{C}$	-	-	1	$\mu A$
		$T_J = 100^\circ\text{C}$	-	-	100	
$V_{GS(th)}$	Gate-Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	V
$R_{DS(on)}$	Drain-Source on-Resistance <sup>4</sup>	$V_{GS} = 10V, I_D = 20A$	-	1.05	1.35	m $\Omega$
$g_{fs}$	Forward Transconductance <sup>4</sup>	$V_{DS} = 10V, I_D = 20A$	-	62	-	S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 40V, V_{GS} = 0V,$ $f = 1\text{MHz}$	-	13085	-	pF
$C_{oss}$	Output Capacitance		-	2615	-	
$C_{rss}$	Reverse Transfer Capacitance		-	120	-	
$R_g$	Gate Resistance	$f = 1\text{MHz}$	-	3.1	-	$\Omega$
<b>Switching Characteristics</b>						
$Q_g$	Total Gate Charge	$V_{GS} = 10V, V_{DS} = 40V,$ $I_D = 20A$	-	243.6	-	nC
$Q_{gs}$	Gate-Source Charge		-	64.2	-	
$Q_{gd}$	Gate-Drain Charge		-	58.8	-	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 10V, V_{DD} = 40V,$ $R_G = 3\Omega, I_D = 20A$	-	44.8	-	ns
$t_r$	Rise Time		-	86.8	-	
$t_{d(off)}$	Turn-off Delay Time		-	164	-	
$t_f$	Fall Time		-	94	-	
$t_{rr}$	Body Diode Reverse Recovery Time		$I_F = 20A,$	-	128	
$Q_{rr}$	Body Diode Reverse Recovery Charge	$dI/dt = 100A/\mu s$	-	140.8	-	nC
<b>Drain-Source Body Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage <sup>4</sup>	$I_S = 20A, V_{GS} = 0V$	-	-	1.2	V
$I_S$	Continuous Source Current	$T_C = 25^\circ\text{C}$	-	-	400	A

**Notes:**

- 1.Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)} = 175^\circ\text{C}$ .
- 2.The EAS data shows Max. rating . The test condition is  $V_{DD} = 25V, V_{GS} = 10V, L = 0.4\text{mH}, I_{AS} = 80A$ .
- 3.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
- 4.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$ .
- 5.This value is guaranteed by design hence it is not included in the production test.

Typical Electrical and Thermal Characteristics (Curves)

Figure 1: Output Characteristics

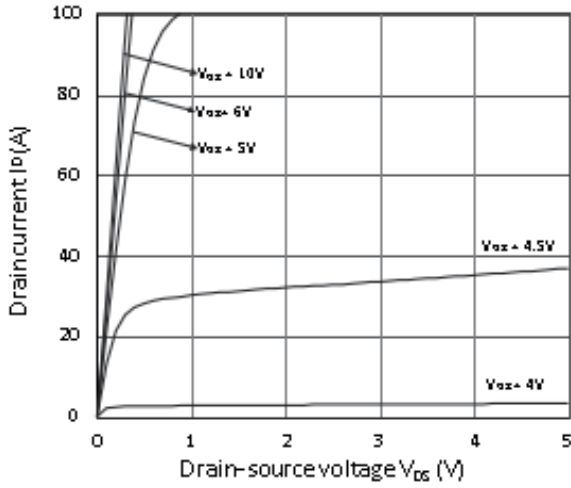


Figure 2: Typ. Transfer Characteristics

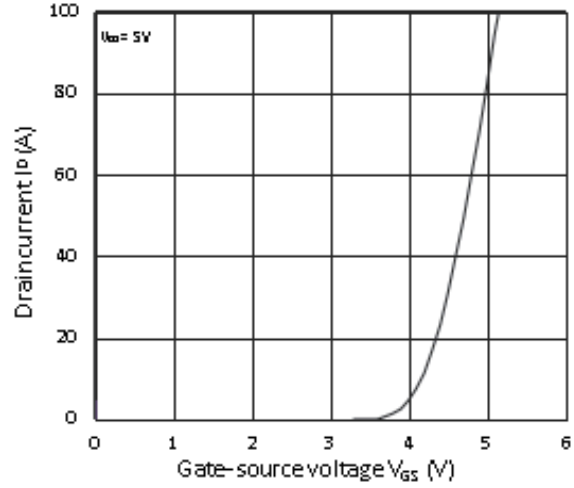


Figure 3: Forward Characteristics of Reverse

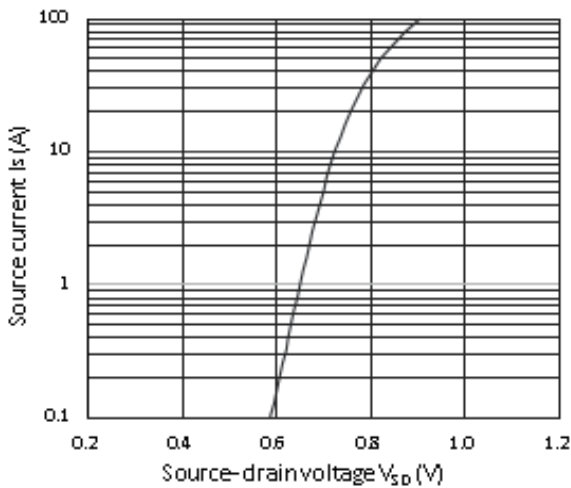


Figure 4: RDS(ON) vs. VGS

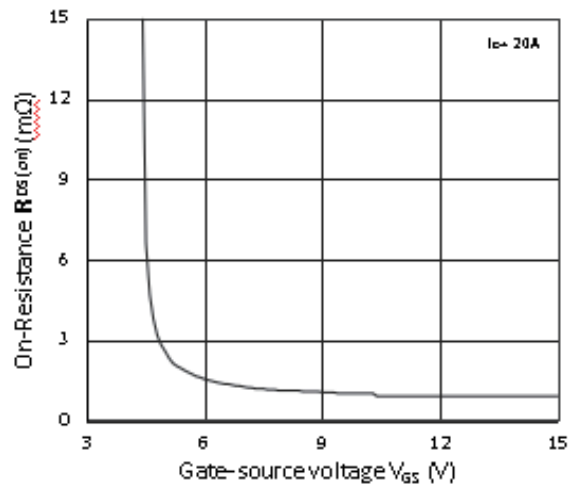


Figure 5: RDS(ON) vs. ID

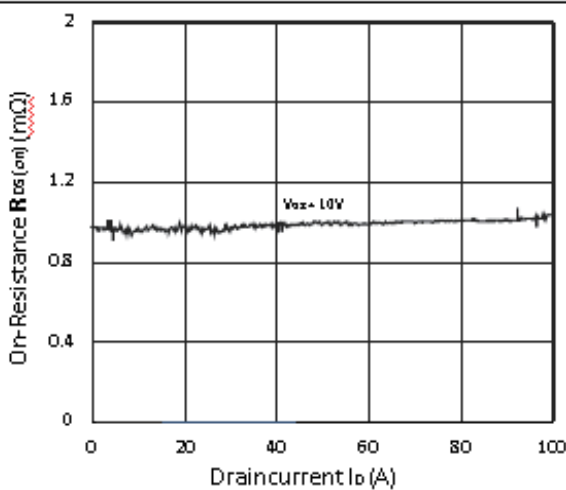
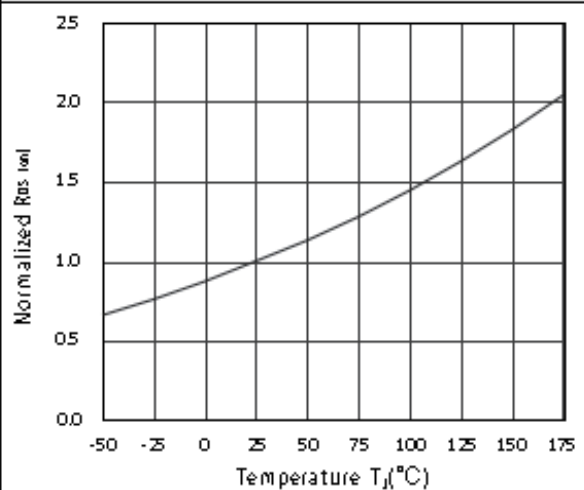


Figure 6: Normalized RDS(on) vs. Temperature



Typical Performance Characteristics

Figure 7: Capacitance Characteristics

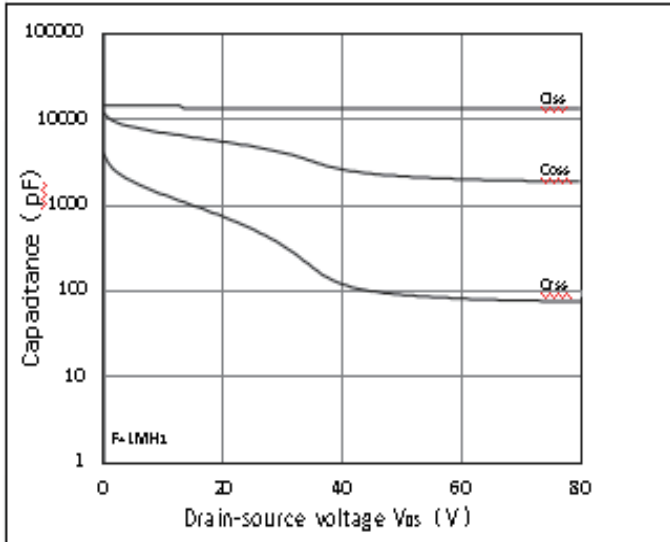


Figure 8: Gate Charge Characteristics

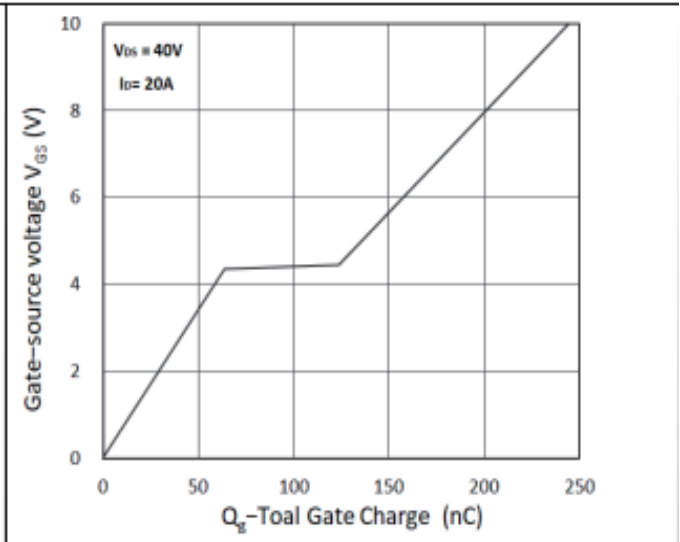


Figure 9: Power Dissipation

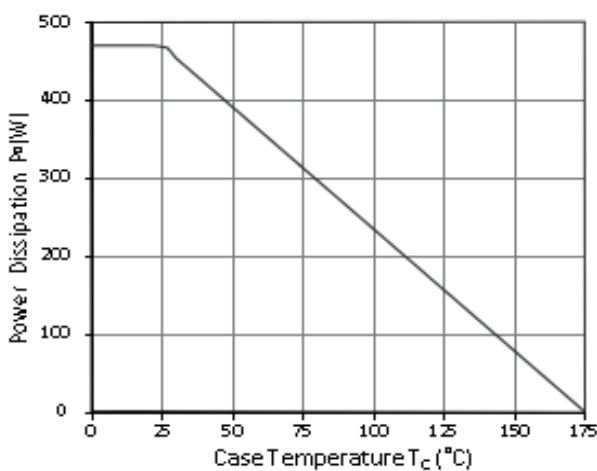


Figure 10: Safe Operating Area

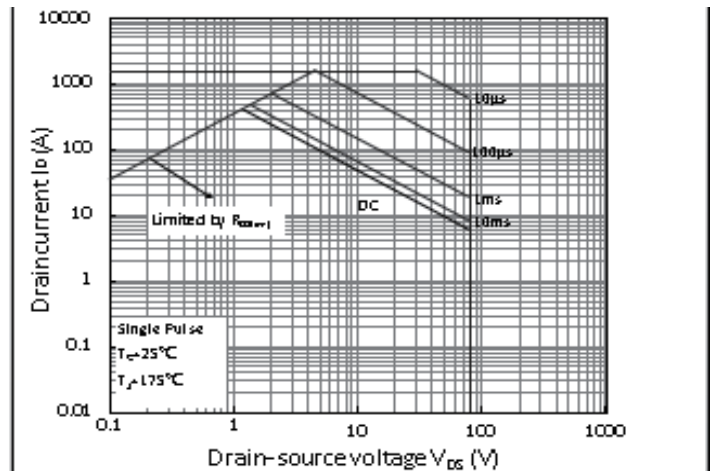
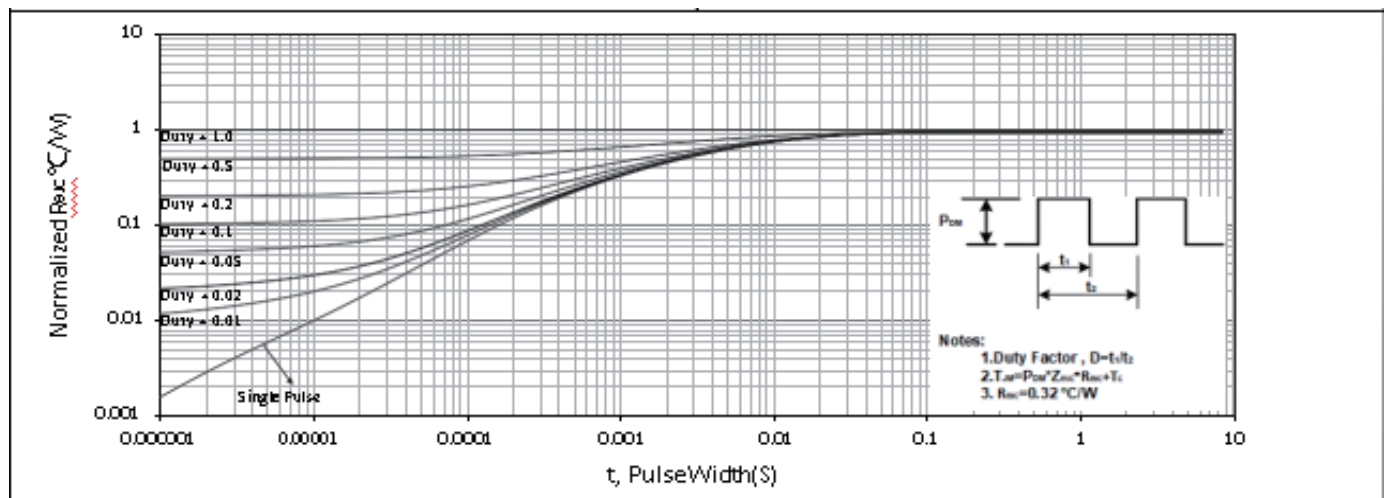


Figure 11: Normalized Maximum Transient Thermal Impedance



## Test Circuit and Waveform

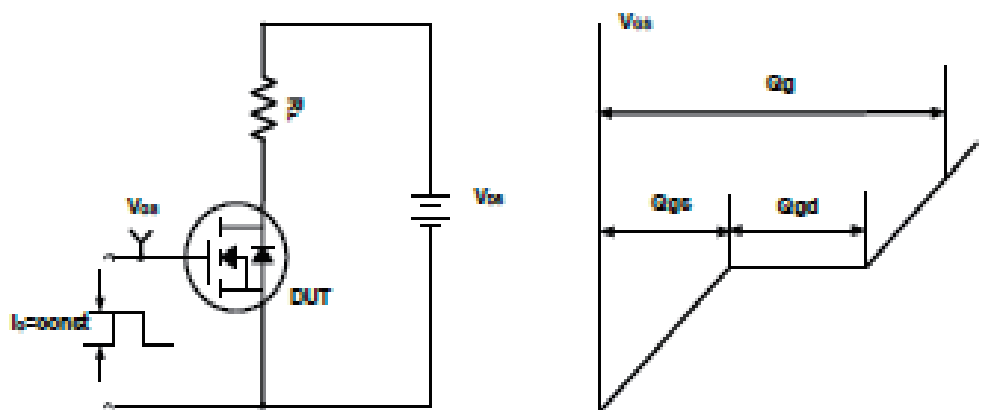


Figure A. Gate Charge Test Circuit & Waveforms

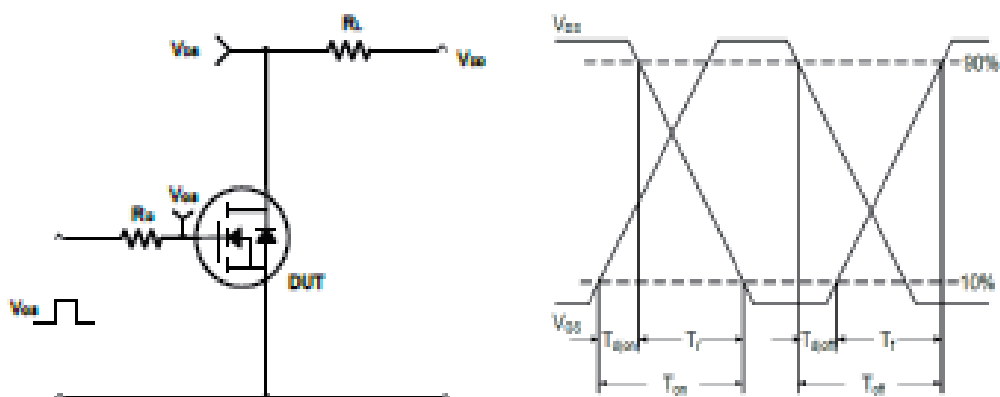


Figure B. Switching Test Circuit & Waveforms

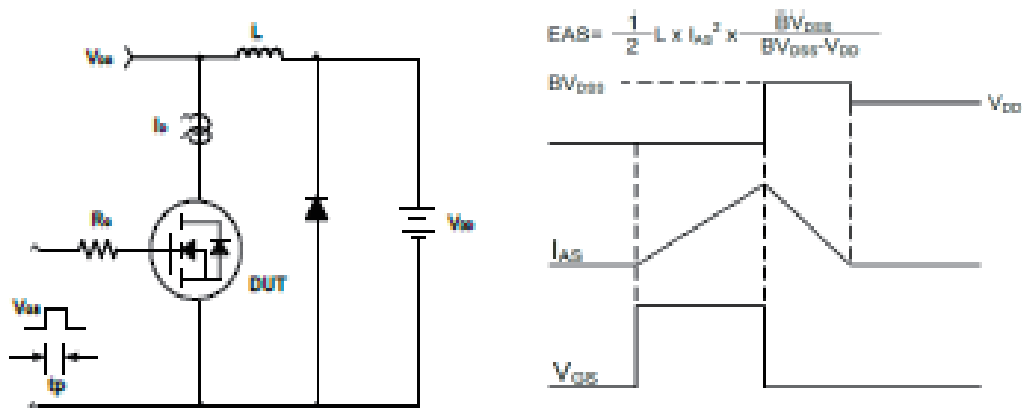
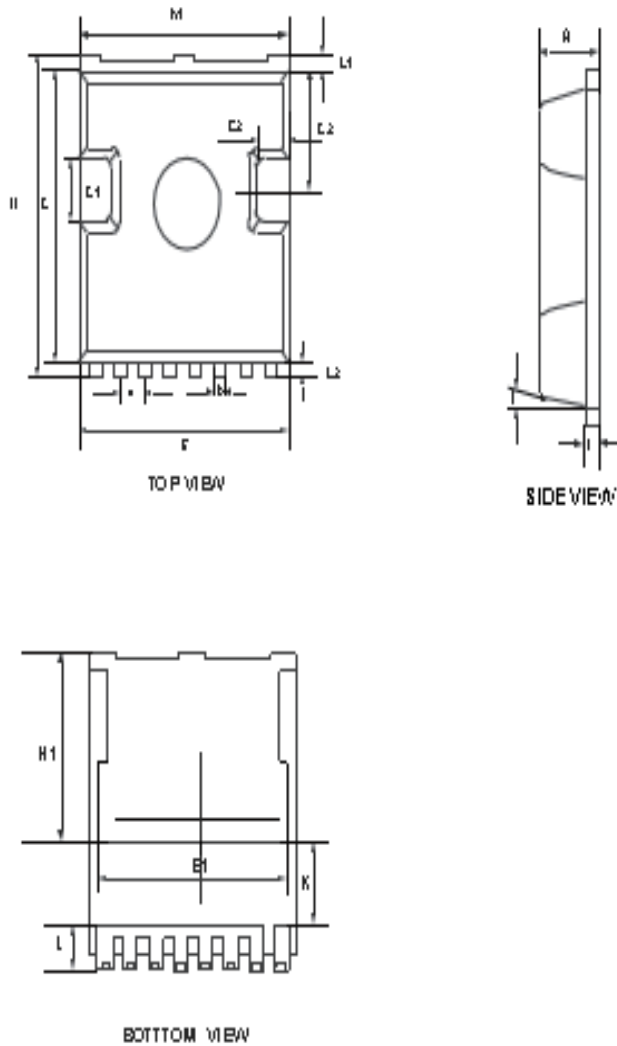


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Mechanical Dimensions for TOLL-8L



COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	2.20	2.40
b	0.60	0.90
b1	9.70	9.90
c	0.40	0.60
D	10.20	10.60
D1	3.10	3.50
D2	4.45	4.75
E	9.70	10.10
E1	7.80BSC	
E2	0.50	0.70
e	1.200 BSC	
H	11.45	11.90
H1	6.75 BSC	
K	3.10 REF	
L	1.70	2.10
L1	0.60	0.80
L2	0.50	0.70
$\theta$	10° REF	

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