

- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Advanced Trench MOS Technology
- ★ 100% EAS Guaranteed
- ★ Excellent CdV/dt effect decline

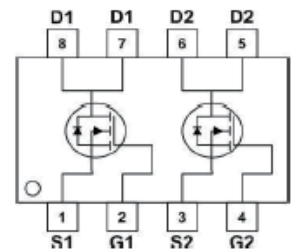
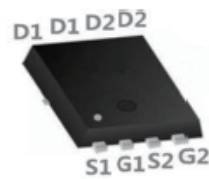
Product Summary

BVDSS	RDSON	ID
40V	7.2mΩ	40A

Description

The S4896D is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The S4896D meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

PDFN3* 3 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	±20	V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	40	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	20	A
I_{DM}	Pulsed Drain Current 2	180	A
EAS	Single Pulse Avalanche Energy 3	26.1	mJ
I_{AS}	Avalanche Current	15	A
$P_D@T_C=25^{\circ}C$	Total Power Dissipation 4	43.6	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) 1	---	62	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case 1	---	2.8	°C/W

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=12A$	---	7.2	9.5	m Ω
		$V_{GS}=4.5V, I_D=10A$	---	10	15	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.35	---	3	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=32V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=32V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.7	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=20V, V_{GS}=4.5V, I_D=12A$	---	5.8	---	nC
Q_{gs}	Gate-Source Charge		---	3	---	
Q_{gd}	Gate-Drain Charge		---	1.2	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega, I_D=1A$	---	14.3	---	ns
T_r	Rise Time		---	5.6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	20	---	
T_f	Fall Time		---	11	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	690	---	pF
C_{oss}	Output Capacitance		---	193	---	
C_{rss}	Reverse Transfer Capacitance		---	38	---	

Thermal Data

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	40	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=31A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Performance Characteristics

Figure1: Output Characteristics

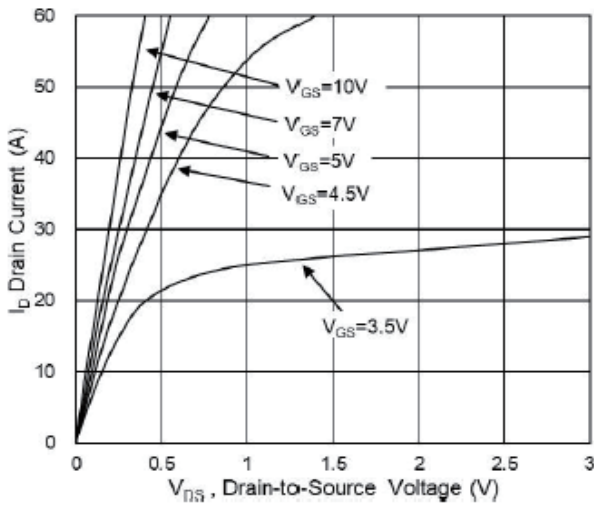


Figure 2: On-Resistance vs G-S Voltage

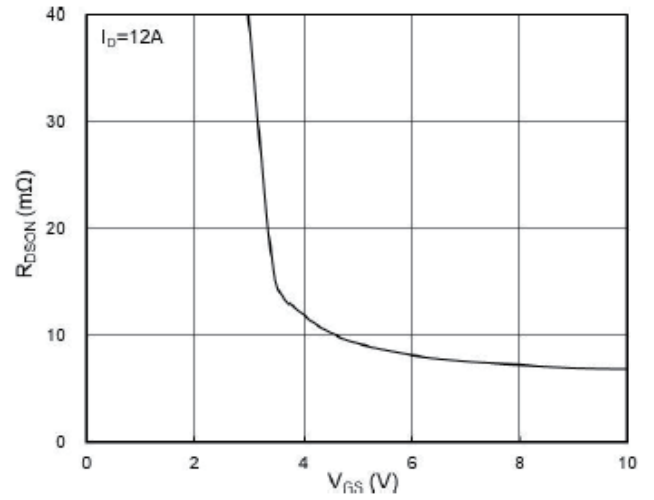


Figure 3: Source Drain Forward Character

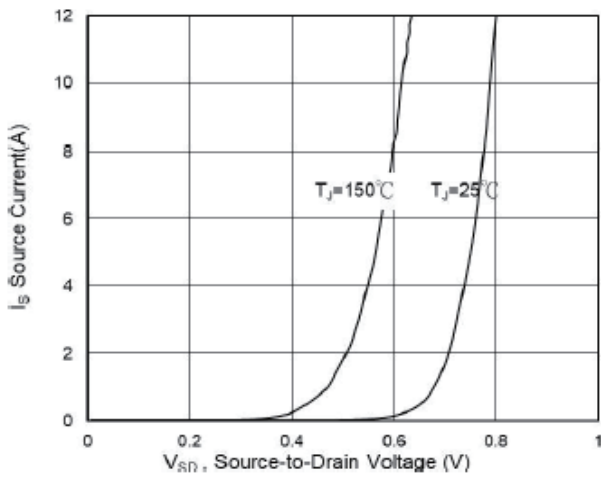


Figure 4: Gate-Charge Characteristics

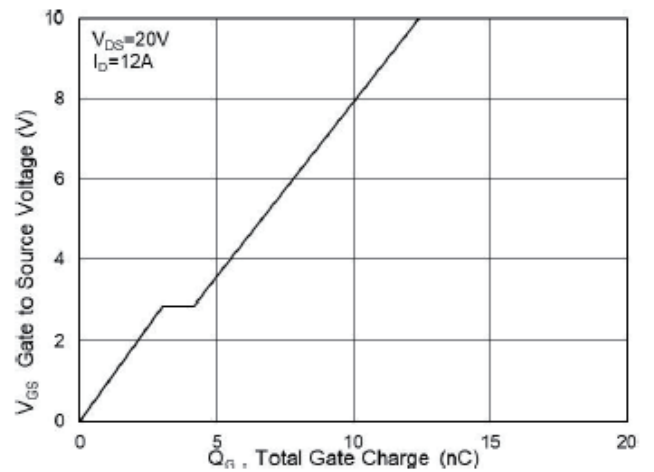


Figure 5: Normalized VGS(th) vs TJ

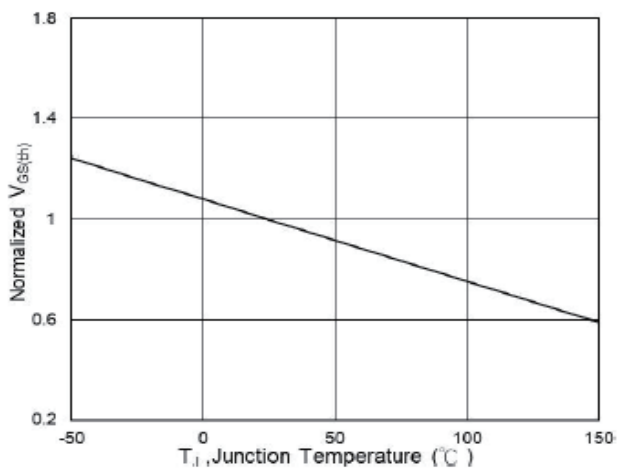
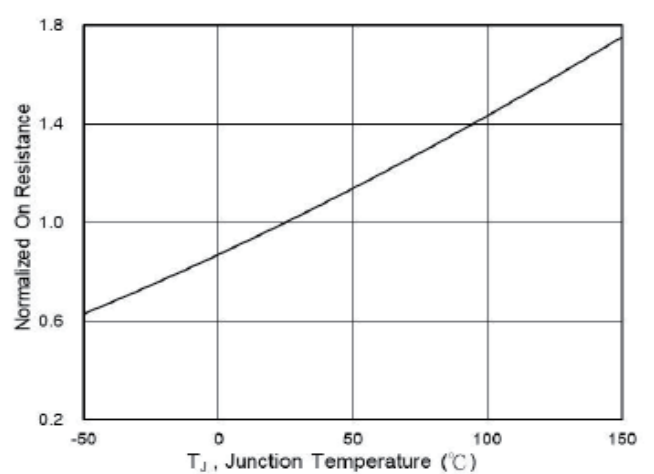


Figure 6: Normalized RDS(on) vs TJ



Typical Performance Characteristics

Figure 7: Capacitance

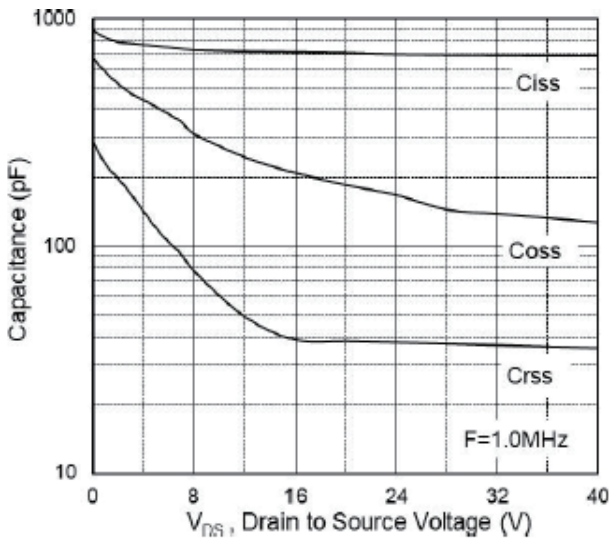


Figure 8: Safe Operating Area

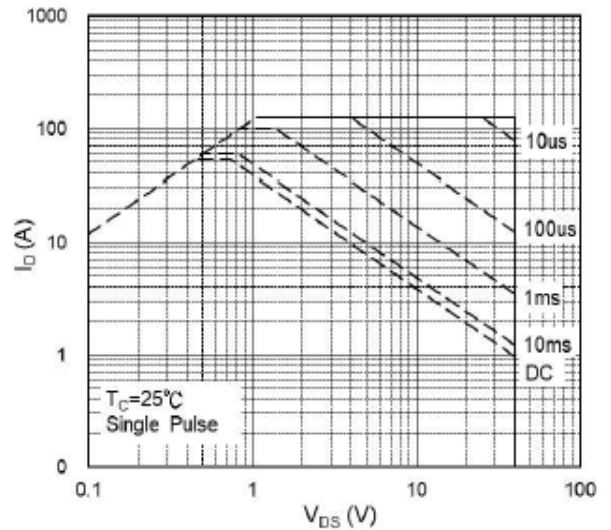


Figure 9: Normalized Maximum Transient Thermal Impedance

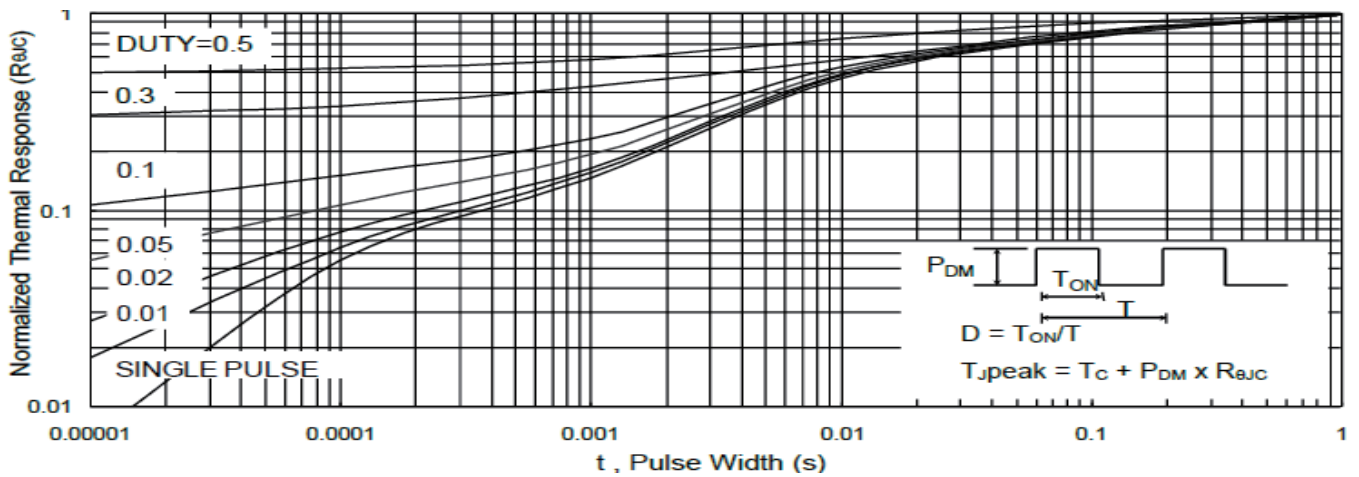


Figure.10: Switching Time Waveform

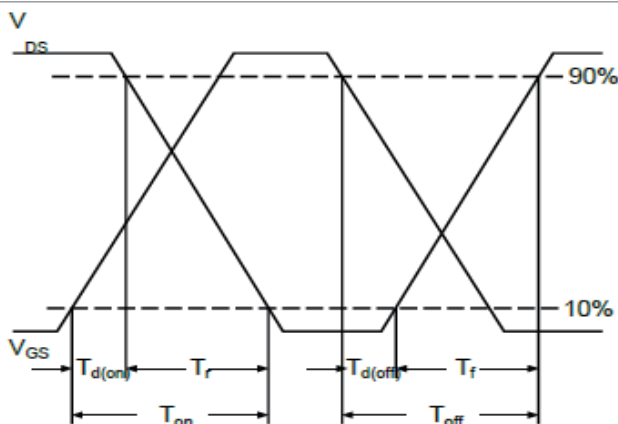
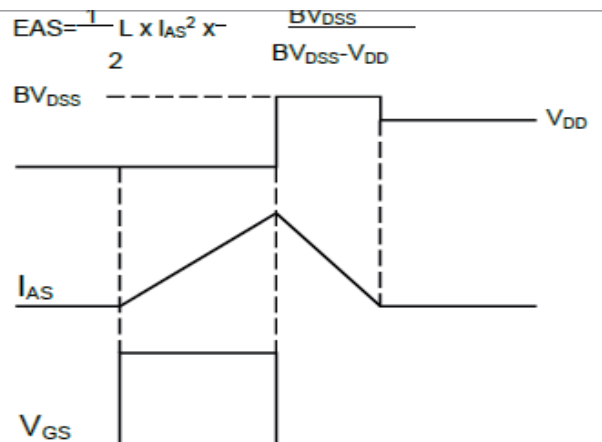
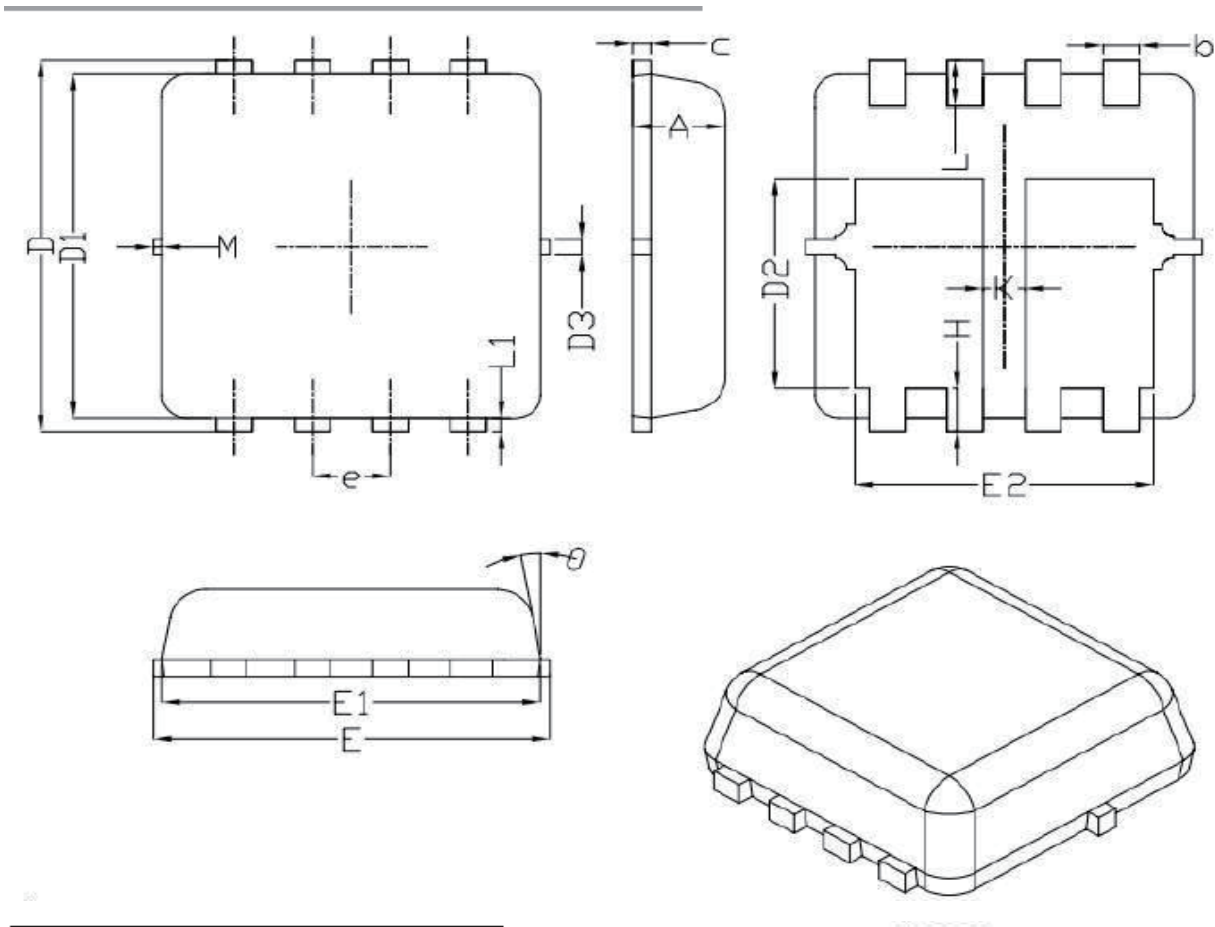


Figure.11: Unclamped Inductive Switching



Dual PDFN3X3 Package Outline Data



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Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
theta	--	10°	12°
M	*	*	0.15
* Not Specified			

Notes:

1. Refer to JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion.

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