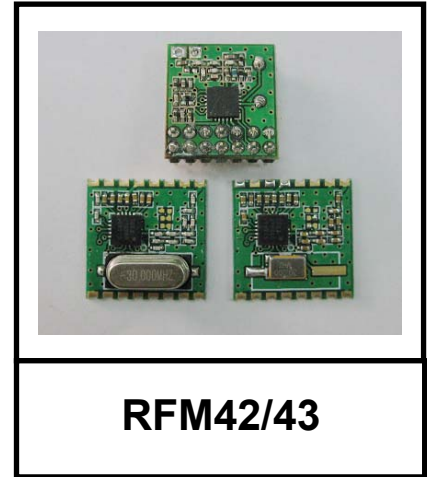


**RFM42/43 ISM TRANSMITTER Module**

V1.1

**Features**

- Frequency Range = 240–930 MHz
- Output Power Range
  - ◆ +8 to +17 dBm (RFM42)
  - ◆ –8 to +13 dBm (RFM43)
- Low Power Consumption
  - ◆ (RFM42)
    - 60 mA @ +17 dBm
    - 27 mA @ +11 dBm
  - ◆ (RFM43)
    - 28 mA @ +13 dBm
    - 16 mA @ +1 dBm
- Data Rate = 1 to 128 kbps
- Power Supply = 1.8 to 3.6 V
- Ultra low power shutdown mode
- Wake Up Timer
- Integrated 32 kHz RC or 32 kHz XTAL
- Integrated voltage regulators
- Configurable packet structure
- TX 64 byte FIFO
- Low battery detector
- Temperature sensor and 8-bit ADC
- –40 to +85 °C temperature range
- Integrated voltage regulators
- Frequency hopping capability
- FSK, GFSK, and OOK modulation
- Power-on-reset (POR)

**Applications**

- Remote control
- Home security & alarm
- Telemetry
- Personal data logging
- Toy control
- Wireless PC peripherals
- Remote keyless entry
- Remote meter reading
- Home automation
- Industrial control
- Sensor networks
- Health monitors

**Description**

The RFM42/43 is low cost ISM transmitter module and offers advanced radio features including continuous frequency coverage from 240–930 MHz with adjustable power output levels of –8 to +13 dBm on the RFM43 and +8 to +17 dBm on the RFM42. Power adjustments are made in 3 dB steps. The RFM42's Industry leading +17 dBm output power ensures extended range and improved link performance.

Additional system features such as an automatic wake-up timer, low battery detector, 64 byte TX FIFO, and automatic packet handling reduce overall current consumption and allow the use of lower-cost system MCUs. An integrated temperature sensor, general purpose ADC, power-on-reset (POR), and GPIOs further reduce overall system cost and size.

The direct digital transmit modulation and automatic PA power ramping ensure precise transmit modulation and reduced spectral spreading ensuring compliance with FCC and ETSI regulations.

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## 1. Electrical Specifications

Table 1. DC Characteristics

| Parameter   | Symbol           | Conditions   | Min | Typ | Max | Units   |
|---|------------------|--|-----|-----|-----|---------|
| Supply Voltage Range  | $V_{dd}$         |  | 1.8 | 3.0 | 3.6 | V       |
| Power Saving Modes  | $I_{Shutdown}$   | RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF <sup>2</sup>                                  | —   | 10  | TBD | nA      |
|   | $I_{Standby}$    | Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator, and RC Oscillator OFF <sup>1</sup> | —   | 400 | —   | nA      |
|   | $I_{Sleep}$      | RC Oscillator and Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator OFF <sup>1</sup>  | —   | 800 | —   | nA      |
|   | $I_{Sensor-LBD}$ | Main Digital Regulator and Low Battery Detector ON, Crystal Oscillator and all other blocks OFF <sup>2</sup>             | —   | 1   | —   | $\mu$ A |
|   | $I_{Sensor-TS}$  | Main Digital Regulator and Temperature Sensor ON, Crystal Oscillator and all other blocks OFF <sup>2</sup>               | —   | 1   | —   | $\mu$ A |
|   | $I_{Ready}$      | Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF. Crystal Oscillator buffer disabled <sup>1</sup>  | —   | 600 | —   | $\mu$ A |
| TUNE Mode Current   | $I_{Tune}$       | Synthesizer and regulators enabled   | —   | 9.5 | —   | mA      |
| TX Mode Current for RFM42   | $I_{TX_{+17}}$   | txpow[2:0] = 011 (+17 dBm), VDD = 3.3 V  | —   | 60  | —   | mA      |
|   | $I_{TX_{+11}}$   | txpow[2:0] = 000 (+11 dBm), VDD = 3.3 V  | —   | 27  | —   | mA      |
| TX Mode Current for RFM43   | $I_{TX_{+13}}$   | txpow[2:0] = 111 (+13 dBm), VDD = 3.3 V  | —   | 28  | —   | mA      |
|   | $I_{TX_{+1}}$    | txpow[2:0] = 100 (+1 dBm), VDD = 3.3 V   | —   | 16  | —   | mA      |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. All specification guaranteed by production test unless otherwise noted.</li> <li>2. Guaranteed by qualification.</li> </ol> |                  |  |     |     |     |         |

**Table 2. Synthesizer AC Electrical Characteristics<sup>2</sup>**

| Parameter                                     | Symbol                | Conditions  | Min | Typ    | Max | Units              |
|---|-----------------------|---|-----|--------|-----|--------------------|
| Synthesizer Frequency Range                   | F <sub>SYNTH-LB</sub> | Low Band  | 240 | —      | 480 | MHz                |
|   | F <sub>SYNTH-HB</sub> | High Band   | 480 | —      | 930 | MHz                |
| Synthesizer Frequency Resolution <sup>2</sup> | F <sub>RES-LB</sub>   | Low Band  | —   | 156.25 | —   | Hz                 |
|   | F <sub>RES-HB</sub>   | High Band   | —   | 312.5  | —   | Hz                 |
| Reference Frequency                           | f <sub>REF</sub>      | f <sub>crystal</sub> /3   | —   | 10     | —   | MHz                |
| Reference Frequency Input Level <sup>2</sup>  | f <sub>REF_LV</sub>   | When using reference frequency instead of crystal. Measured peak-to-peak (VPP)                | 0.7 | —      | 1.6 | V                  |
| Synthesizer Settling Time <sup>2</sup>        | t <sub>LOCK</sub>     | Measured from leaving Ready mode with XOSC running to any frequency including VCO Calibration | —   | 200    | —   | μs                 |
| Residual FM <sup>2</sup>                      | ΔF <sub>RMS</sub>     | Integrated over ± 250 kHz bandwidth (500 Hz lower bound of integration)                       | —   | 2      | 4   | kHz <sub>RMS</sub> |
| Phase Noise <sup>2</sup>                      | L <sub>φ</sub> (fM)   | ΔF = 10 kHz   | —   | -80    | —   | dBc/Hz             |
|   |                       | ΔF = 100 kHz  | —   | -90    | —   | dBc/Hz             |
|   |                       | ΔF = 1 MHz  | —   | -115   | —   | dBc/Hz             |
|   |                       | ΔF = 10 MHz   | —   | -130   | —   | dBc/Hz             |

**Notes:**

1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

**Table 3. Transmitter AC Electrical Characteristics**<sup>1</sup>

| Parameter   | Symbol                | Conditions   | Min    | Typ   | Max  | Units |
|---|-----------------------|--|--------|-------|------|-------|
| TX Frequency Range <sup>1</sup>                           | F <sub>SYNTH-LB</sub> | Low Band   | 240    | —     | 480  | MHz   |
|   | F <sub>SYNTH-HB</sub> | High Band  | 480    | —     | 930  |       |
| FSK Modulation Data Rate <sup>2</sup>                     | DR <sub>FSK</sub>     |  | 1      | —     | 128  | kbps  |
| OOK Modulation Data Rate <sup>2</sup>                     | DR <sub>OOK</sub>     |  | 1.2    | —     | 40   | kbps  |
| Modulation Deviation <sup>1</sup>                         | Δf                    | Production tests maximum limit of 320 kHz  | ±0.625 |       | ±320 | kHz   |
| Modulation Deviation Resolution                           | Δf <sub>RES</sub>     |  | —      | 0.625 | —    | kHz   |
| Output Power Range <sup>1</sup> (RFM43)                   | P <sub>TX</sub>       | Power control by txpow[2:0] Register<br>Production test at txpow[2:0] = 11 Tested at 915 MHz | -8     | —     | +13  | dBm   |
| Max Output Power(RFM43)                                   | P <sub>TX_max</sub>   | Tested at 315-915 MHz  | +11    | +13   | —    | dBm   |
| Output Power Range <sup>1</sup> (RFM42)                   | P <sub>TX</sub>       | Power control by txpow[2:0] Register<br>Production test at txpow[2:0] = 11 Tested at 915 MHz | +8     | —     | +17  | dBm   |
| Max Output Power(RFM42)                                   | P <sub>TX_max</sub>   | Tested at 315-915 MHz  | +15    | +17   | —    | dBm   |
| TX RF Output Steps <sup>2</sup>                           | P <sub>RF_OUT</sub>   | controlled by txpow[2:0] Register  | —      | 3     | —    | dB    |
| TX RF Output Level Variation vs. Voltage <sup>2</sup>     | P <sub>RF_V</sub>     | Measured from VDD=3.6 V to VDD=1.8 V   | —      | 2     | —    | dB    |
| TX RF Output Level <sup>2</sup> Variation vs. Temperature | P <sub>RF_TEMP</sub>  | -40 to +85 °C  | —      | 2     | —    | dB    |
| TX RF Output Level Variation vs. Frequency <sup>2</sup>   | P <sub>RF_FREQ</sub>  | Measured across any one frequency band   | —      | 1     | —    | dB    |
| Transmit Modulation Filtering <sup>2</sup>                | B*T                   | Gaussian Filtering Bandwith Time Product   | —      | 0.5   | —    |       |
| Spurious Emissions <sup>2</sup>                           | P <sub>OB-TX1</sub>   | P <sub>OUT</sub> =11dBm, Frequencies <1 GHz  | —      | —     | -54  | dBm   |
|   | P <sub>OB-TX2</sub>   | 1-12.75 GHz, excluding harmonics   | —      | —     | -54  | dBm   |

**Notes:**

1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

**Table 4. Auxiliary Block Specifications<sup>1</sup>**

| Parameter  | Symbol               | Conditions  | Min     | Typ  | Max | Units |
|--|----------------------|---|---------|------|-----|-------|
| Temperature Sensor Accuracy <sup>2</sup>                                   | TS <sub>A</sub>      | When calibrated using temp sensor offset register                                 | —       | 0.5  | —   | °C    |
| Temperature Sensor Sensitivity <sup>2</sup>                                | TS <sub>S</sub>      |   | —       | 5    | —   | mV/°C |
| Low Battery Detector Resolution <sup>2</sup>                               | LBD <sub>RES</sub>   |   | —       | 50   | —   | mV    |
| Low Battery Detector Conversion Time <sup>2</sup>                          | LBD <sub>CT</sub>    |   | —       | 250  | —   | μs    |
| Microcontroller Clock Output Frequency                                     | MC                   | Configurable to 30 MHz, 15 MHz, 10 MHz, 4 MHz, 3 MHz, 2 MHz, 1 MHz, or 32.768 kHz | 32.768K | —    | 30M | Hz    |
| General Purpose ADC Accuracy <sup>2</sup>                                  | ADC <sub>ENB</sub>   |   | —       | 8    | —   | bit   |
| General Purpose ADC Resolution <sup>2</sup>                                | ADC <sub>RES</sub>   |   | —       | 4    | —   | mV    |
| Temp Sensor & General Purpose ADC Conversion Time <sup>2</sup>             | ADC <sub>CT</sub>    |   | —       | 305  | —   | μsec  |
| 30 MHz XTAL Start-Up time  | t <sub>30M</sub>     |   | —       | 1    | —   | ms    |
| 30 MHz XTAL Cap Resolution <sup>2</sup>                                    | 30M <sub>RES</sub>   |   | —       | 97   | —   | fF    |
| 32 kHz XTAL Start-Up Time <sup>2</sup>                                     | t <sub>32K</sub>     |   | —       | 6    | —   | sec   |
| 32 kHz XTAL Accuracy <sup>2</sup>  | 32K <sub>RES</sub>   |   | —       | 100  | —   | ppm   |
| 32 kHz RC OSC Accuracy <sup>2</sup>  | 32KRC <sub>RES</sub> |   | —       | 2500 | —   | ppm   |
| POR Reset Time   | t <sub>POR</sub>     |   | —       | 16   | —   | ms    |
| Software Reset Time <sup>2</sup>   | t <sub>soft</sub>    |   | —       | 100  | —   | μs    |
| <b>Notes:</b>  |                      |   |         |      |     |       |
| 1. All specification guaranteed by production test unless otherwise noted. |                      |   |         |      |     |       |
| 2. Guaranteed by qualification.  |                      |   |         |      |     |       |

**Table 5. Digital IO Specifications (SDO, SDI, SCLK, nSEL, and nIRQ)**

| Parameter                       | Symbol | Conditions                       | Min       | Typ | Max | Units |
|---------------------------------|--------|----------------------------------|-----------|-----|-----|-------|
| Rise Time                       | TRISE  | 0.1 x VDD to 0.9 x VDD, CL= 5 pF | —         | —   | 8   | ns    |
| Fall Time                       | TFALL  | 0.9 x VDD to 0.1 x VDD, CL= 5 pF | —         | —   | 8   | ns    |
| Input Capacitance               | CIN    |                                  | —         | —   | 1   | pF    |
| Logic High Level Input Voltage  | VIH    |                                  | VDD – 0.6 | —   | —   | V     |
| Logic Low Level Input Voltage   | VIL    |                                  |           | —   | 0.6 | V     |
| Input Current                   | IIN    | 0<VIN< VDD                       | -100      | —   | 100 | nA    |
| Logic High Level Output Voltage | VOH    | IOH<1 mA source, VDD=1.8 V       | VDD – 0.6 | —   | —   | V     |
| Logic Low Level Output Voltage  | VOL    | IOL<1 mA sink, VDD=1.8 V         | —         | —   | 0.6 | V     |

Note: All specification guaranteed by production test unless otherwise noted.

**Table 6. GPIO Specifications (GPIO\_0, GPIO\_1, and GPIO\_2)**

| Parameter                            | Symbol  | Conditions                                     | Min       | Typ | Max | Units |
|--------------------------------------|---------|--|-----------|-----|-----|-------|
| Rise Time                            | TRISE   | 0.1 x VDD to 0.9 x VDD, CL= 10 pF, DRV<1:0>=HH | —         | —   | 8   | ns    |
| Fall Time                            | TFALL   | 0.9 x VDD to 0.1 x VDD, CL= 10 pF, DRV<1:0>=HH | —         | —   | 8   | ns    |
| Input Capacitance                    | CIN     |  | —         | —   | 1   | pF    |
| Logic High Level Input Voltage       | VIH     |  | VDD – 0.6 | —   | —   | V     |
| Logic Low Level Input Voltage        | VIL     |  | —         | —   | 0.6 | V     |
| Input Current                        | IIN     | 0<VIN< VDD                                     | -100      | —   | 100 | nA    |
| Input Current If Pullup is Activated | IINP    |  | VIL=0 V   | 5   | —   | 25    |
| Maximum Output Current               | IOmaxLL | DRV<1:0>=LL                                    | 0.1       | 0.5 | 0.8 | mA    |
|                                      | IOmaxLH | DRV<1:0>=LH                                    | 0.9       | 2.3 | 3.5 | mA    |
|                                      | IOmaxHL | DRV<1:0>=HL                                    | 1.5       | 3.1 | 4.8 | mA    |
|                                      | IOmaxHH | DRV<1:0>=HH                                    | 1.8       | 3.6 | 5.4 | mA    |
| Logic High Level Output Voltage      | VOH     | IOH< IOmax source, VDD=1.8 V                   | VDD – 0.6 | —   | —   | V     |
| Logic Low Level Output Voltage       | VOL     | IOL< IOmax sink, VDD=1.8 V                     | —         | —   | 0.6 | V     |

Note: All specification guaranteed by production test unless otherwise noted.



**Table 7. Absolute Maximum Ratings**

| Parameter  | Value           | Unit |
|--|-----------------|------|
| VDD to GND   | -0.3, +3.6      | V    |
| VDD to GND on TX Output Pin                        | -0.3, +8.0      | V    |
| Voltage on Digital Control Inputs                  | -0.3, VDD + 0.3 | V    |
| Voltage on Analog Inputs                           | -0.3, VDD + 0.3 | V    |
| Operating Ambient Temperature Range T <sub>A</sub> | -40 to +85      | °C   |
| Thermal Impedance $\theta_{JA}$                    | 30              | °C/W |
| Junction Temperature T <sub>J</sub>                | +125            | °C   |
| Storage Temperature Range T <sub>STG</sub>         | -55 to +125     | °C   |

**Note:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Caution: ESD sensitive device.

Power Amplifier may be damaged if switched on without proper load or termination connected.

## 2. Functional Description

The RFM42/43 is low cost ISM wireless transmitter module with continuous frequency tuning over the complete 240–930 MHz band. The wide operating voltage range of 1.8–3.6 V and low current consumption makes the RFM42/43 an ideal solution for battery powered applications.

A high precision local oscillator (LO) is used for transmit mode. The LO is generated by an integrated VCO and  $\Delta\Sigma$  Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates, output frequency, frequency deviation, and Gaussian filtering at any frequency between 240–930 MHz. The transmit FSK data is modulated directly into the  $\Delta\Sigma$  data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The RFM42's PA output power can be configured between +8 and +17 dBm in 3 dB steps, while the RFM43's PA output power can be configured between –8 and +13 dBm in 3 dB steps. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading.

The RFM42/43 is designed to work with a microcontroller to create a very low cost system. Voltage regulators are integrated on-chip which allow for a wide range of operating supply voltage conditions from +1.8 to +3.6 V. A standard 4-pin SPI bus is used to communicate with the microcontroller. Three configurable general purpose I/Os are available for use to tailor towards the needs of the system. A more complete list of the available GPIO functions is shown in "7. Auxiliary Functions" but just to name a few, microcontroller clock output, POR, and specific interrupts.

### 2.1. Operating Modes

The RFM42/43 provides several modes of operation which can be used to optimize the power consumption of the device application.

Table 8 summarizes the modes of operation of the RFM42/43. In general, any given mode of operation may be classified as an Active mode or a Power Saving mode. The table indicates which block(s) are enabled (active) in each corresponding mode. With the exception the Shutdown mode, all can be dynamically selected by sending the appropriate commands over the SPI in order to optimize the average current consumption. An "X" in any cell means that, in the given mode of operation, that block can be independently programmed to be either ON or OFF, without noticeably affecting the current consumption. The SPI circuit block includes the SPI interface and the register space. The 32 kHz OSC circuit block includes the 32.768 kHz RC oscillator or 32.768 kHz crystal oscillator, and wake-up timer. AUX (Auxiliary Blocks) includes the temperature sensor, general purpose ADC, and low-battery detector.

**Table 8. Operating Modes**

| Mode Name | Circuit Blocks                     |     |            |     |             |     |     | I <sub>VDD</sub> |
|-----------|------------------------------------|-----|------------|-----|-------------|-----|-----|------------------|
|           | Digital LDO                        | SPI | 32 kHz OSC | AUX | 30 MHz XTAL | PLL | PA  |                  |
| Shutdown  | OFF<br>(Register contents lost)    | OFF | OFF        | OFF | OFF         | OFF | OFF | 10 nA            |
| Standby   | ON<br>(Register contents retained) | ON  | OFF        | OFF | OFF         | OFF | OFF | 400 nA           |
| Sleep     |                                    | ON  | ON         | X   | OFF         | OFF | OFF | 800 nA           |
| Sensor    |                                    | ON  | X          | ON  | OFF         | OFF | OFF | 1 $\mu$ A        |
| Ready     |                                    | ON  | X          | X   | ON          | OFF | OFF | 600 $\mu$ A      |
| Tuning    |                                    | ON  | X          | X   | ON          | ON  | OFF | 9.5 mA           |
| Transmit  |                                    | ON  | X          | X   | ON          | ON  | ON  | 28 mA*           |

**\*Note: 28 mA at +3 dBm RFM43**

## 3. Controller Interface

### 3.1. Serial Peripheral Interface (SPI)

The RFM42/43 communicates with the host MCU over a 3 wire SPI interface: SCLK, SDI, and nSEL. The host MCU can also read data from internal registers on the SDO output pin. A SPI transaction is a 16-bit sequence which consists of a Read-Write ( $\overline{R/W}$ ) select bit, followed by a 7-bit address field (ADDR), and an 8-bit data field (DATA), as demonstrated in Figure 1. The 7-bit address field supports reading from or writing to one of the 128, 8-bit control registers. The  $\overline{R/W}$  select bit determines whether the SPI transaction is a write or read transaction. If  $\overline{R/W} = 1$ , it signifies a WRITE transaction, while  $\overline{R/W} = 0$  signifies a READ transaction. The contents (ADDR or DATA) are latched into the RFM42/43 every eight clock cycles. The timing parameters for the SPI interface are shown in Table 9. The SCLK rate is flexible with a maximum rate of 10 MHz.

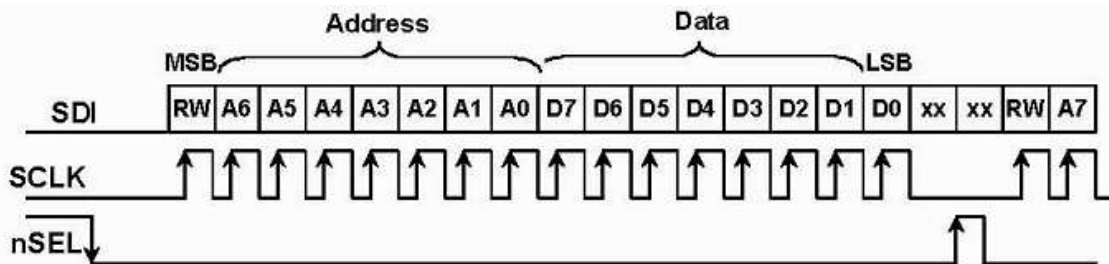
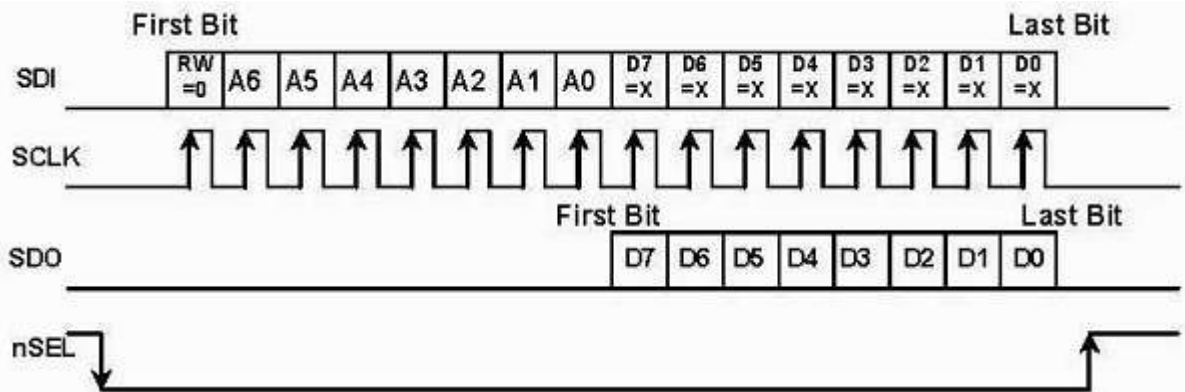


Figure 1. SPI Timing

Table 9. Serial Interface Timing Parameters

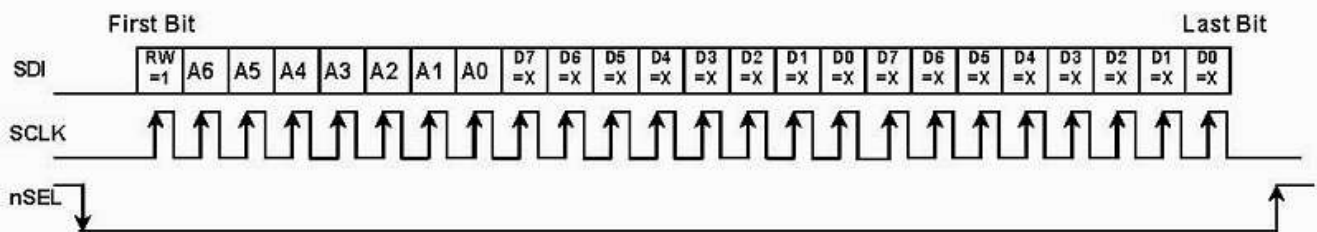
| Symbol   | Parameter              | Min (nsec) | Diagram |
|----------|------------------------|------------|---------|
| $t_{CH}$ | Clock high time        | 40         |         |
| $t_{CL}$ | Clock low time         | 40         |         |
| $t_{DS}$ | Data setup time        | 20         |         |
| $t_{DH}$ | Data hold time         | 20         |         |
| $t_{DD}$ | Output data delay time | 20         |         |
| $t_{EN}$ | Output enable time     | 20         |         |
| $t_{DE}$ | Output disable time    | 50         |         |
| $t_{SS}$ | Select setup time      | 20         |         |
| $t_{SH}$ | Select hold time       | 50         |         |
| $t_{SW}$ | Select high period     | 80         |         |

To read back data from the RFM42/43, the  $\overline{R/W}$  bit must be set to 0 followed by the 7-bit address of the register from which to read. The 8 bit DATA field following the 7-bit ADDR field is ignored when  $\overline{R/W} = 0$ . The next eight negative edge transitions of the SCLK signal will clock out the contents of the selected register. The data read from the selected register will be available on the SDO output pin. The READ function is shown in Figure 2. After the READ function is completed the SDO pin will remain at either a logic 1 or logic 0 state depending on the last data bit clocked out (D0). When nSEL goes high the SDO output pin will be pulled high by internal pullup.

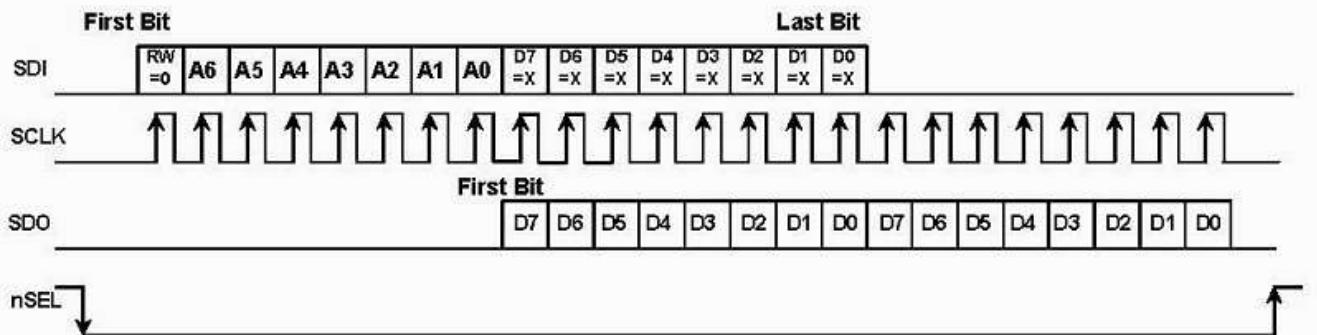


**Figure 2. SPI Timing—READ Mode**

The SPI interface contains a burst read/write mode which will allow for reading/writing sequential registers without having to re-send the SPI address. When the nSEL bit is held low while continuing to send SCLK pulses, the SPI interface will automatically increment the ADDR and read from/write to the next address. An SPI burst write transaction is demonstrated in Figure 3 and burst read in Figure 2. As long as nSEL is held low, input data will be latched into the RFM42/43 every eight SCLK cycles. A burst read transaction is also demonstrated in Figure 4.



**Figure 3. SPI Timing—Burst Write Mode**

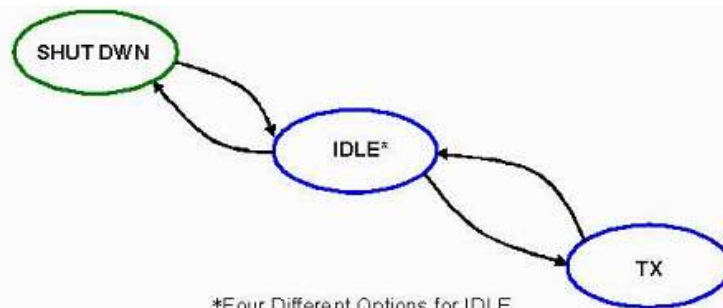


**Figure 4. SPI Timing—Burst Read Mode**

## 3.2. Operating Mode Control

There are three primary states in the RFM42/43 radio state machine: SHUTDOWN, IDLE, and TX (see Figure 5). The SHUTDOWN state completely shuts down the radio to minimize current consumption. There are five different configurations/options for the IDLE state which can be selected to optimize the module to the applications needs. "Register 07h. Operating Mode and Function Control 1" controls which operating mode/state is selected. The TX state may be reached automatically from any of the IDLE states by setting the txon bit in "Register 07h. Operating Mode and Function Control 1". Table 10 shows each of the operating modes with the time required to reach TX mode as well as the current consumption of each mode.

The output of the LPLDO is internally connected in parallel to the output of the main digital regulator (and is available externally at the VR\_DIG pin); this common digital supply voltage is connected to all digital circuit blocks, including the digital modem, crystal oscillator, and SPI and register space. The LPLDO has extremely low quiescent current consumption but limited current supply capability; it is used only in the IDLE-STANDBY and IDLE-SLEEP modes.



\*Four Different Options for IDLE

**Figure 5. State Machine Diagram**

**Table 10. Operating Modes**

| State/Mode      | xtal | pll | wt | LBD or TS | Response Time to TX | Current in State /Mode [µA]   |
|-----------------|------|-----|----|-----------|---------------------|---|
| Shut Down State | X    | X   | X  | X         | 16.21 ms            | 10 nA   |
| Idle States:    |      |     |    |           |                     |   |
| Standby Mode    | 0    | 0   | 0  | 0         | 1.21 ms             | 400 nA  |
| Sleep Mode      | 0    | 0   | 1  | 0         |                     | 800 nA  |
| Sensor Mode     | 0    | 0   | X  | 1         | 1 µA                |   |
| Ready Mode      | 1    | 0   | X  | X         | 210 µs              | 600 µA  |
| Tune Mode       | 1    | 1   | X  | X         | 200 µs              | 9.5 mA  |
| TX State        | 1    | 1   | X  | X         | 200 µs              | <b>RFM42:</b><br>80 mA @ +20 dBm,<br>27 mA @ +11 dBm<br><b>RFM43:</b><br>28 mA @ +13 dBm,<br>16 mA @ +1 dBm |



### 3.2.1. Shutdown State

The shutdown state is the lowest current consumption state of the device with nominally less than 10 nA of current consumption. The shutdown state may be entered by driving the SDN pin high. The SDN pin should be held low in all states except the SHUTDOWN state. In the SHUTDOWN state, the contents of the registers are lost and there is no SPI access.

When the module is connected to the power supply, a POR will be initiated after the falling edge of SDN.

### 3.2.2. Idle State

There are four different modes in the IDLE state which may be selected by "Register 07h. Operating Mode and Function Control 1". All modes have a tradeoff between current consumption and response time to TX mode. This tradeoff is shown in Table 10. After the POR event, SWRESET, or exiting from the SHUTDOWN state the module will default to the IDLE-READY mode. After a POR event the interrupt registers must be read to properly enter the SLEEP, SENSOR, or STANDBY mode and to control the 32 kHz clock correctly.

#### 3.2.2.1. STANDBY Mode

STANDBY mode has the lowest current consumption possible with only the LPLDO enabled to maintain the register values. In this mode the registers can be accessed in both read and write mode. The standby mode can be entered by writing 0h to "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Additionally, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

#### 3.2.2.2. SLEEP Mode

In SLEEP mode the LPLDO is enabled along with the Wake-Up-Timer, which can be used to accurately wake-up the radio at specified intervals. See "7.6. Wake-Up Timer" for more information on the Wake-Up-Timer. Sleep mode is entered by setting enwt = 1 (40h) in "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Also, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

#### 3.2.2.3. SENSOR Mode

In SENSOR Mode either the Low Battery Detector, Temperature Sensor, or both may be enabled in addition to the LPLDO and Wake-Up-Timer. The Low Battery Detector can be enabled by setting enlbd = 1 and the temperature sensor can be enabled by setting ents = 1 in "Register 07h. Operating Mode and Function Control 1". See "7.4. Temperature Sensor" and "7.5. Low Battery Detector" for more information on these features. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption.

#### 3.2.2.4. READY Mode

READY Mode is designed to give a fast transition time to TX mode with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to the TX mode by eliminating the crystal start-up time. Ready mode is entered by setting xton = 1 in "Register 07h. Operating Mode and Function Control 1". To achieve the lowest current consumption state the crystal oscillator buffer should be disabled. This is done by setting "Register 62h. Crystal Oscillator/Power-on-Reset Control" to a value of 02h. To exit ready mode, bufovr (bit 1) of this register must be set back to 0.

#### 3.2.2.5. TUNE Mode

In TUNE Mode the PLL remains enabled in addition to the other blocks enabled in the IDLE modes. This will give the fastest response to TX mode as the PLL will remain locked but it results in the highest current consumption. This mode of operation is designed for Frequency Hopping Systems (FHS). Tune mode is entered by setting pllcn = 1 in "Register 07h. Operating Mode and Function Control 1". It is not necessary to set xton to 1 for this mode, the internal state machine automatically enables the crystal oscillator.

### 3.2.3. TX State

The TX state may be entered from any of the IDLE modes when the txon bit is set to 1 in "Register 07h. Operating Mode and Function Control 1". A built-in sequencer takes care of all the actions required to transition between states from enabling the crystal oscillator to ramping up the PA to prevent unwanted spectral splatter. The following sequence of events will occur automatically when going from STANDBY mode to TX mode by setting the txon bit.

1. Enable the Main Digital LDO and the Analog LDOs.
2. Start up crystal oscillator and wait until ready (controlled by timer).
3. Enable PLL.
4. Calibrate VCO (this action is skipped when the vcocal bit is "0", default value is "1").
5. Wait until PLL settles to required transmit frequency (controlled by timer).
6. Activate Power Amplifier and wait until power ramping is completed (controlled by timer).
7. Transmit Packet.

The first few steps may be eliminated depending on which IDLE mode the module is configured to prior to setting the txon bit. By default, the VCO and PLL are calibrated every time the PLL is enabled. If the ambient temperature is constant and the same frequency band is being used these functions may be skipped by setting the appropriate bits in "Register 55h. Calibration Control".

### 3.2.4. Device Status

| Add | R/W | Function/Description | D7     | D6     | D5       | D4       | D3 | D2 | D1     | D0     | POR Def. |
|-----|-----|----------------------|--------|--------|----------|----------|----|----|--------|--------|----------|
| 02  | R   | Device Status        | ffovfl | ffunfl | Reserved | Reserved |    |    | cps[1] | cps[0] | —        |

The operational status of the module can be read from "Register 02h. Device Status".

### 3.3. Interrupts

The RFM42/43 is capable of generating an interrupt signal when certain events occur. The module notifies the microcontroller that an interrupt event has been detected by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) shown below occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Register(s) (Registers 03h–04h) containing the active Interrupt Status bit; the nIRQ output signal will then be reset until the next change in status is detected. All of the interrupts must be enabled by the corresponding enable bit in the Interrupt Enable Registers (Registers 05h–06h). All enabled interrupt bits will be cleared when the microcontroller reads the interrupt status register. If the interrupt is not enabled when the event occurs inside of the module it will not trigger the nIRQ pin, but the status may still be read correctly at anytime in the Interrupt Status registers.

| Add | R/W | Function/Description | D7       | D6          | D5        | D4       | D3    | D2            | D1        | D0       | POR Def. |
|-----|-----|----------------------|----------|-------------|-----------|----------|-------|---------------|-----------|----------|----------|
| 03  | R   | Interrupt Status 1   | ifferr   | itxffafull  | itxffaem  | Reserved | iext  | ipksent       | Reserved  | Reserved | —        |
| 04  | R   | Interrupt Status 2   | Reserved | Reserved    | Reserved  | Reserved | iwut  | ilbd          | ichiprdy  | ipor     | —        |
| 05  | R/W | Interrupt Enable1    | enferr   | entxffafull | entxffaem | Reserved | enext | enpkse<br>ent | Reserved  | Reserved | 00h      |
| 06  | R/W | Interrupt Enable 2   | Reserved | Reserved    | Reserved  | Reserved | enwut | enlbd         | enchiprdy | enpor    | 01h      |

See “Register 03h. Interrupt/Status 1,” and “Register 04h. Interrupt/Status 2,” for a complete list of interrupts.

### 3.4. Device Code

The device version code is readable from "Register 01h. Version Code (VC)". This is a read only register.

| Add | R/W | Function/Description | D7 | D6 | D5 | D4    | D3    | D2    | D1    | D0    | POR Def. | Notes |
|-----|-----|----------------------|----|----|----|-------|-------|-------|-------|-------|----------|-------|
| 01  | R   | Device Version       | 0  | 0  | 0  | vc[4] | vc[3] | vc[2] | vc[1] | vc[0] | 00h      | DV    |



### 3.5. System Timing

The system timing for TX mode is shown in Figure 6. The timing is shown transitioning from STANDBY mode to TX mode and going automatically through the built-in sequencer of required steps. If a small range of frequencies is being used and the temperature range is fairly constant a calibration may only be needed at the initial power up of the device.

The relevant system timing registers are shown below.

| Add | R/W | Function/Description | D7         | D6                | D5             | D4       | D3    | D2            | D1     | D0      | POR Def. |
|-----|-----|----------------------|------------|-------------------|----------------|----------|-------|---------------|--------|---------|----------|
| 53  | R/W | PLL Tune Time        | pllts[4:0] |                   |                |          |       | pllto[2:0]    |        |         | 45h      |
| 54  | R/W | Reserved 1           | X          | X                 | X              | X        | X     | X             | X      | X       | 00h      |
| 55  | R/W | Calibration Control  |            | xtalstart<br>half | adccal<br>done | enrcfcal | rccal | Vcocal<br>ldp | vcocal | skipvco | 04h      |

The VCO will automatically calibrate at every frequency change or power up. The VCO CAL may also be forced by setting the vcocal bit. The 32.768 kHz RC oscillator is also automatically calibrated but the calibration may also be forced. The enrccal will enable the RC Fine Calibration which will occur every 30 seconds. The rccal bit will force a complete calibration of the RC oscillator which will take approximately 2 ms. The PLL T0 time is to allow for bias settling of the VCO, the default for this should be adequate. The PLL TS time is for the settling time of the PLL, which has a default setting of 200 μs. This setting should be adequate for most applications but may be reduced if small frequency jumps are used. For more information on the PLL register configuration options, see “Register 53h. PLL Tune Time,” and “Register 55h. Calibration Control,”.

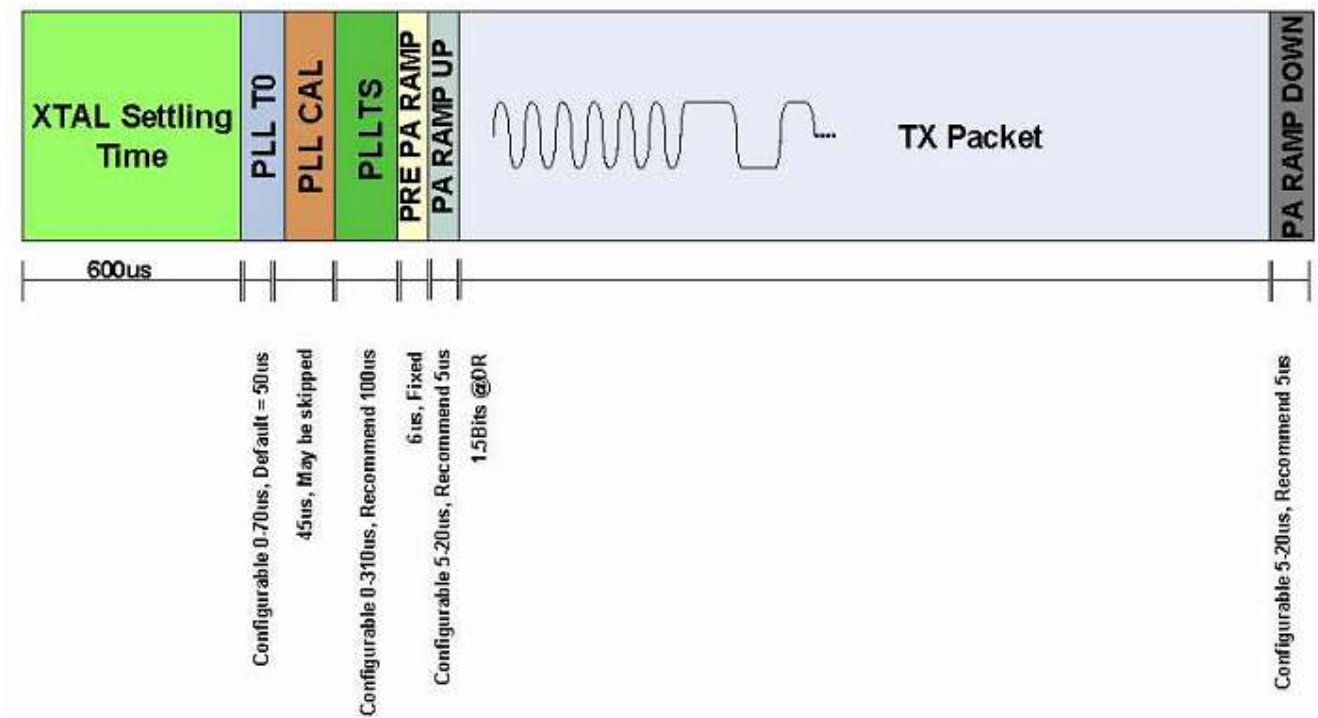


Figure 6. TX Timing

## 3.6. Frequency Control

### 3.6.1. Frequency Programming

In order to transmit an RF signal, the desired channel frequency,  $f_{carrier}$ , must be programmed into the RFM42/43. Note that this frequency is the center frequency of the desired channel and not an LO frequency. The carrier frequency is generated by a Fractional-N Synthesizer, using 10 MHz both as the reference frequency and the clock of the (3<sup>rd</sup> order)  $\Delta\Sigma$  modulator. This modulator uses modulo 64000 accumulators. This design was made to obtain the desired frequency resolution of the synthesizer. The overall division ratio of the feedback loop consist of an integer part (N) and a fractional part (F). In a generic sense, the output frequency of the synthesizer is:

$$f_{out} = 10MHz \times (N + F)$$

The fractional part (F) is determined by three different values, Carrier Frequency ( $fc[15:0]$ ), Frequency Offset ( $fo[8:0]$ ), and Frequency Modulation ( $fd[7:0]$ ). Due to the fine resolution and high loop bandwidth of the synthesizer, FSK modulation is applied inside the loop and is done by varying F according to the incoming data; this is discussed further in "3.6.4. Frequency Deviation". Also, a fixed offset can be added to fine-tune the carrier frequency and counteract crystal tolerance errors. For simplicity assume that only the  $fc[15:0]$  register will determine the fractional component. The equation for selection of the carrier frequency is shown below:

$$f_{carrier} = 10MHz \times (hbsel + 1) \times (N + F)$$

$$f_{TX} = 10MHz * (hbsel + 1) * (fb[4 : 0] + 24 + \frac{fc[15: 0]}{64000})$$

| Add | R/W | Function/Description        | D7     | D6     | D5     | D4     | D3     | D2     | D1    | D0    | POR Def. |
|-----|-----|-----------------------------|--------|--------|--------|--------|--------|--------|-------|-------|----------|
| 73  | R/W | Frequency Offset 1          | fo[7]  | fo[6]  | fo[5]  | fo[4]  | fo[3]  | fo[2]  | fo[1] | fo[0] | 00h      |
| 74  | R/W | Frequency Offset2           |        |        |        |        |        |        | fo[9] | fo[8] | 00h      |
| 75  | R/W | Frequency Band Select       |        | sbsel  | hbsel  | fb[4]  | fb[3]  | fb[2]  | fb[1] | fb[0] | 35h      |
| 76  | R/W | Nominal Carrier Frequency 1 | fc[15] | fc[14] | fc[13] | fc[12] | fc[11] | fc[10] | fc[9] | fc[8] | BBh      |
| 77  | R/W | Nominal Carrier Frequency 0 | fc[7]  | fc[6]  | fc[5]  | fc[4]  | fc[3]  | fc[2]  | fc[1] | fc[0] | 80h      |

The integer part (N) is determined by  $fb[4:0]$ . Additionally, the output frequency can be halved by connecting a  $\div 2$  divider to the output. This divider is not inside the loop and is controlled by the  $hbsel$  bit in "Register 75h.

Frequency Band Select". This effectively partitions the entire 240–930 MHz frequency range into two separate bands: High Band (HB) for  $hbsel = 1$ , and Low Band (LB) for  $hbsel = 0$ . The valid range of  $fb[4:0]$  is from 0 to 23. If a higher value is written into the register, it will default to a value of 23. The integer part has a fixed offset of 24 added to it as shown in the formula above. Table 11 demonstrates the selection of  $fb[4:0]$  for the corresponding frequency band.

After selection of the  $fb$  (N) the fractional component may be solved with the following equation:

$$fc[15:0] = \left( \frac{f_{TX}}{10MHz * (hbsel + 1)} - fb[4:0] - 24 \right) * 64000$$

$fb$  and  $fc$  are the actual numbers stored in the corresponding registers.

**Table 11. Frequency Band Selection**

| fb[4:0] Value | N  | Frequency Band |               |
|---------------|----|----------------|---------------|
|               |    | hbse1=0        | hbse1=1       |
| 0             | 24 | 240–249.9 MHz  | 480–499.9 MHz |
| 1             | 25 | 250–259.9 MHz  | 500–519.9 MHz |
| 2             | 26 | 260–269.9 MHz  | 520–539.9 MHz |
| 3             | 27 | 270–279.9 MHz  | 540–559.9 MHz |
| 4             | 28 | 280–289.9 MHz  | 560–579.9 MHz |
| 5             | 29 | 290–299.9 MHz  | 580–599.9 MHz |
| 6             | 30 | 300–309.9 MHz  | 600–619.9 MHz |
| 7             | 31 | 310–319.9 MHz  | 620–639.9 MHz |
| 8             | 32 | 320–329.9 MHz  | 640–659.9 MHz |
| 9             | 33 | 330–339.9 MHz  | 660–679.9 MHz |
| 10            | 34 | 340–349.9 MHz  | 680–699.9 MHz |
| 11            | 35 | 350–359.9 MHz  | 700–719.9 MHz |
| 12            | 36 | 360–369.9 MHz  | 720–739.9 MHz |
| 13            | 37 | 370–379.9 MHz  | 740–759.9 MHz |
| 14            | 38 | 380–389.9 MHz  | 760–779.9 MHz |
| 15            | 39 | 390–399.9 MHz  | 780–799.9 MHz |
| 16            | 40 | 400–409.9 MHz  | 800–819.9 MHz |
| 17            | 41 | 410–419.9 MHz  | 820–839.9 MHz |
| 18            | 42 | 420–429.9 MHz  | 840–859.9 MHz |
| 19            | 43 | 430–439.9 MHz  | 860–879.9 MHz |
| 20            | 44 | 440–449.9 MHz  | 880–899.9 MHz |
| 21            | 45 | 450–459.9 MHz  | 900–919.9 MHz |
| 22            | 46 | 460–469.9 MHz  | 920–930.0 MHz |
| 23            | 47 | 470–479.9 MHz  | —             |

The module will automatically shift the frequency of the Synthesizer down by 937.5 kHz ( $30 \text{ MHz} \div 32$ ) to achieve the correct Intermediate Frequency (IF).

### 3.6.2. Easy Frequency Programming for FHSS

While Registers 73h–77h may be used to program the carrier frequency of the RFM42/43, it is often easier to think in terms of “channels” or “channel numbers” rather than an absolute frequency value in Hz. Also, there may be some timing-critical applications (such as for Frequency Hopping Systems) in which it is desirable to change frequency by programming a single register. Once the channel step size is set, the frequency may be changed by a single register corresponding to the channel number. A nominal frequency is first set using Registers 73h–77h, as described above. Registers 79h and 7Ah are then used to set a channel step size and channel number, relative to the nominal setting. The Frequency Hopping Step Size (fhs[7:0]) is set in increments of 10 kHz with a maximum channel step size of 2.56 MHz. The Frequency Hopping Channel Select Register then selects channels based on multiples of the step size.

$$F_{carrier} = F_{nom} + fhs[7 : 0] \times (fhch[7 : 0] \times 10kHz)$$

For example: if the nominal frequency is set to 900 MHz using Registers 73h–77h and the channel step size is set to 1 MHz using "Register 7Ah. Frequency Hopping Step Size". For example, if the "Register 79h. Frequency Hopping Channel Select" is set to 5d, the resulting carrier frequency would be 905 MHz. Once the nominal frequency and channel step size are programmed in the registers, it is only necessary to program the fhch[7:0] register in order to change the frequency.

| Add | R/W | Function/Description             | D7      | D6      | D5      | D4      | D3      | D2       | D1       | D0       | POR Def. |
|-----|-----|----------------------------------|---------|---------|---------|---------|---------|----------|----------|----------|----------|
| 79  | R/W | Frequency Hopping Channel Select | fhch[7] | fhch[6] | fhch[5] | fhch[4] | fhch[3] | fhch [2] | fhch [1] | fhch [0] | 00h      |
| 7A  | R/W | Frequency Hopping Step Size      | fhs[7]  | fhs[6]  | fhs[5]  | fhs[4]  | fhs[3]  | fhs[2]   | fhs[1]   | fhs[0]   | 00h      |

### 3.6.3. Automatic Frequency Change

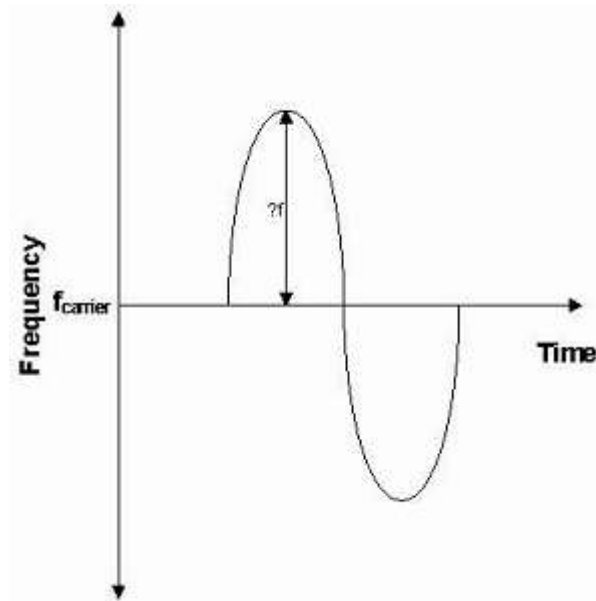
If registers 79h or 7Ah are changed in TX mode, the state machine will automatically transition the module back to tune and change the frequency. This feature is useful to reduce the number of SPI commands required in a Frequency Hopping System. This in turn reduces microcontroller activity, reducing current consumption.

### 3.6.4. Frequency Deviation

The peak frequency deviation is configurable from ±1 to ±320 kHz. The Frequency Deviation (Δf) is controlled by the Frequency Deviation Register (fd), address 71 and 72h, and is independent of the carrier frequency setting. When enabled, regardless of the setting of the hbsel bit (high band or low band), the resolution of the frequency deviation will remain in increments of 625 Hz. When using frequency modulation the carrier frequency will deviate from the nominal center channel carrier frequency by ±Δf:

$$\Delta f = fd [8: 0] \times 625Hz$$

$$fd [8: 0] = \frac{\Delta f}{625Hz} \quad \Delta f = \text{peak deviation}$$



**Figure 7. Frequency Deviation**

The previous equation should be used to calculate the desired frequency deviation. If desired, frequency modulation may also be disabled in order to obtain an unmodulated carrier signal at the channel center frequency; see "4.1. Modulation Type" for further details.

| Add | R/W | Function/Description      | D7       | D6       | D5       | D4       | D3     | D2     | D1        | D0        | POR Def. |
|-----|-----|---------------------------|----------|----------|----------|----------|--------|--------|-----------|-----------|----------|
| 71  | R/W | Modulation Mode Control 2 | trclk[1] | trclk[0] | dtmod[1] | dtmod[0] | eninv  | fd[8]  | modtyp[1] | modtyp[0] | 00h      |
| 72  | R/W | Frequency Deviation       | fd [7]   | fd [6]   | fd [5]   | fd [4]   | fd [3] | fd [2] | fd [1]    | fd [0]    | 43h      |

### 3.6.5. Frequency Offset Adjustment

A frequency offset can be adjusted manually by fo[9:0] in registers 73h and 74h. The frequency offset adjustment is implemented by shifting the Synthesizer Local Oscillator frequency. This register is a signed register so in order to get a negative offset you will need to take the twos complement of the positive offset number. The offset can be calculated by the following:

$$DesiredOffset = 156.25Hz \times (hbssel + 1) \times fo[9 : 0]$$

$$fo[9 : 0] = \frac{DesiredOffset}{156.25Hz \times (hbssel + 1)}$$

The adjustment range in high band is: ±160 kHz, and adjustment range in low band is: ±80 kHz. For example to compute an offset of +50 kHz in high band mode fo[9:0] should be set to 0A0h. For an offset of -50 kHz in high band mode the fo[9:0] register should be set to 360h.

| Add | R/W | Function/Description | D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    | POR Def. | Notes |
|-----|-----|----------------------|-------|-------|-------|-------|-------|-------|-------|-------|----------|-------|
| 73  | R/W | Frequency Offset     | fo[7] | fo[6] | fo[5] | fo[4] | fo[3] | fo[2] | fo[1] | fo[0] | 00h      | 73    |
| 74  | R/W | Frequency Offset     |       |       |       |       |       |       | fo[9] | fo[8] | 43h      |       |

### 3.6.6. TX Data Rate Generator

The data rate is configurable between 1–128 kbps. For data rates below 30 kbps the “txdtrscale” bit in register 70h should be set to 1. When higher data rates are used this bit should be set to 0.

The TX data rate is determined by the following formula:

$$DR\_TX = \frac{txdr[15:0] \times 1MHz}{2^{16+5 \times xdtrscale}}$$

$$txdr[15:0] = \frac{DR\_TX \times 2^{16+5 \times xdtrscale}}{1MHz}$$

The txdr register may be found in the following registers.

| Add | R/W | Function/Description | D7       | D6       | D5       | D4       | D3       | D2       | D1      | D0      | POR Def. |
|-----|-----|----------------------|----------|----------|----------|----------|----------|----------|---------|---------|----------|
| 6E  | R/W | TX Data Rate 1       | txdr[15] | txdr[14] | txdr[13] | txdr[12] | txdr[11] | txdr[10] | txdr[9] | txdr[8] | 0Ah      |
| 6F  | R/W | TX Data Rate 0       | txdr[7]  | txdr[6]  | txdr[5]  | txdr[4]  | txdr[3]  | txdr[2]  | txdr[1] | txdr[0] | Ah       |

## 4. Modulation Options

### 4.1. Modulation Type

The RFM42/43 supports three different modulation options: Gaussian Frequency Shift Keying (GFSK), Frequency Shift Keying (FSK), and On-Off Keying (OOK). GFSK is the recommended modulation type as it provides the best performance and cleanest modulation spectrum. Figure 8 demonstrates the difference between FSK and GFSK for a Data Rate of 64 kbps. The time domain plots demonstrate the effects of the Gaussian filtering. The frequency domain plots demonstrate the spectral benefit of GFSK over FSK. The type of modulation is selected with the modtyp[1:0] bits in "Register 71h. Modulation Mode Control 2". Note that it is also possible to obtain an unmodulated carrier signal by setting modtyp[1:0] = 00.

| modtyp[1:0] | Modulation Source                                  |
|-------------|--|
| 00          | Unmodulated Carrier                                |
| 01          | OOK  |
| 10          | FSK  |
| 11          | GFSK (enable TX Data CLK when direct mode is used) |

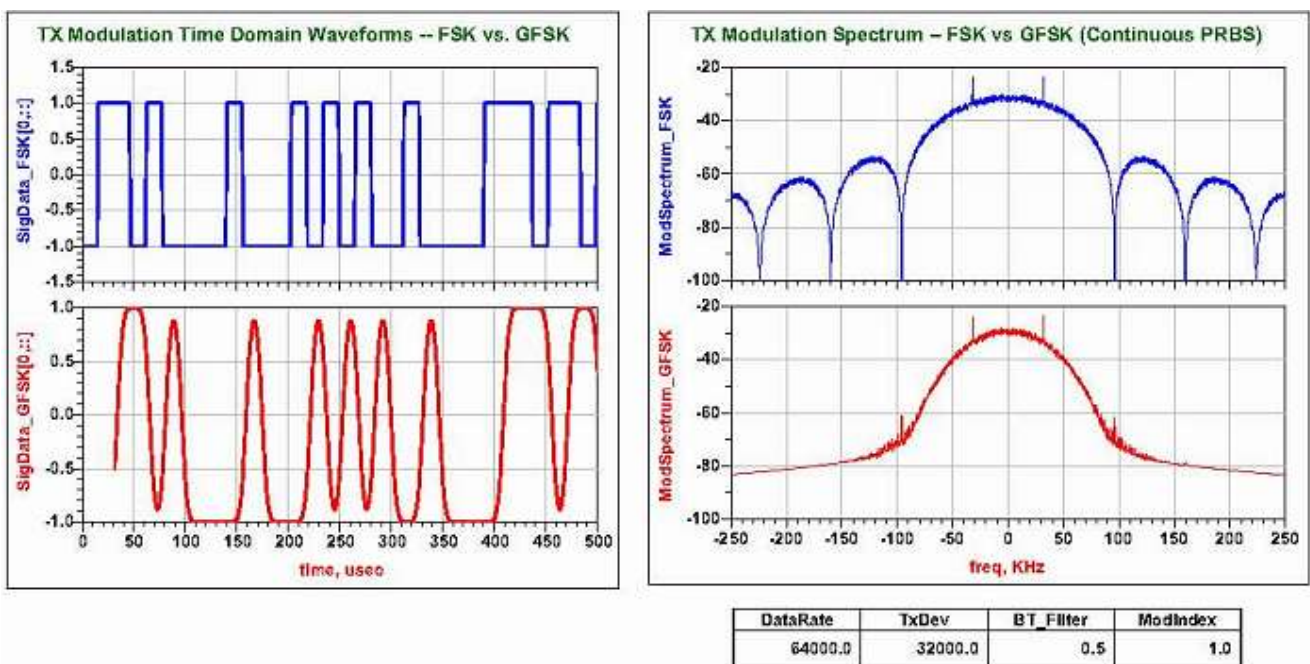


Figure 8. FSK vs GFSK Spectrums



## 4.2. Modulation Data Source

The RFM42/43 may be configured to obtain its modulation data from one of three different sources: FIFO mode, Direct Mode, and from a PN9 mode. Furthermore, in Direct Mode, the TX modulation data may be obtained from several different input pins. These options are set through the dtmod[1:0] field in "Register 71h. Modulation Mode Control 2".

| Add | R/W | Function/Description      | D7       | D6       | D5        | D4        | D3    | D2    | D1        | D0        | POR Def. |
|-----|-----|---------------------------|----------|----------|-----------|-----------|-------|-------|-----------|-----------|----------|
| 71  | R/W | Modulation Mode Control 2 | trclk[1] | trclk[0] | dtmod [1] | dtmod [0] | eninv | fd[8] | modtyp[1] | modtyp[0] | 23h      |

| modtyp[1:0] | Modulation Source  |
|-------------|--|
| 00          | Direct Mode using TX_Data via GPIO pin (GPIO needs programming accordingly also) |
| 01          | Direct Mode using TX_Data via SDI pin (only when nSEL is high)                   |
| 10          | FIFO Mode  |
| 11          | PN9 (internally generated)   |

## 4.3. FIFO Mode

In FIFO mode, the integrated FIFO is used to transmit the data. The FIFO is accessed via "Register 7Fh. FIFO Access" with burst write capability. The FIFO may be configured specific to the application packet size, etc. (see "6. Data Handling and Packet Handler" for further information).

When in FIFO mode the module will automatically exit the TX State when the *ipksent* interrupt occurs. The module will return to any of the other states based on the settings in "Register 07h. Operating Mode and Function Control 1".

For instance, if both the txon and pllcn bits are set, the module will transmit all of the contents of the FIFO and the ipksent interrupt will occur. When this event occurs the module will clear the txon bit and return to pllcn or Tune Mode. If no other bits are set in register 07h besides txon initially then the module will return to the Idle state.

## 4.4. Direct Mode

For legacy systems that have packet handling within an MCU or other baseband module, it may not be desirable to use the FIFO. For this scenario, a Direct Mode is provided which bypasses the FIFOs entirely. In Direct Mode, the TX modulation data is applied to an input pin of the module and processed in "real time" (i.e., not stored in a register for transmission at a later time). There are various configurations for choosing which pin is used for the TX Data.

Furthermore, an additional input pin is required for the TX Data Clock if GFSK modulation is desired (only the TX Data input pin is required for FSK). Two options for the source of the TX Data are available in the dtmod[1:0] field, and various configurations for the source of the TX Data Clock may be selected through the trclk[1:0] field.

| trclk[1:0] | TX Data Clock Configuration  |
|------------|--|
| 00         | No TX Clock (only for FSK)   |
| 01         | TX Data Clock is available via GPIO (GPIO needs programming accordingly as well) |
| 10         | TX Data Clock is available via SDO pin (only when nSEL is high)                  |
| 11         | TX Data Clock is available via the nIRQ pin                                      |

The eninv bit in Address 71h will invert the TX Data for testing purposes.



## 4.5. PN9 Mode

In this mode the TX Data is generated internally using a pseudorandom (PN9 sequence) bit generator. The primary purpose of this mode is for use as a test mode to observe the modulated spectrum without having to load/provide data.

## 4.6. Synchronous vs. Asynchronous

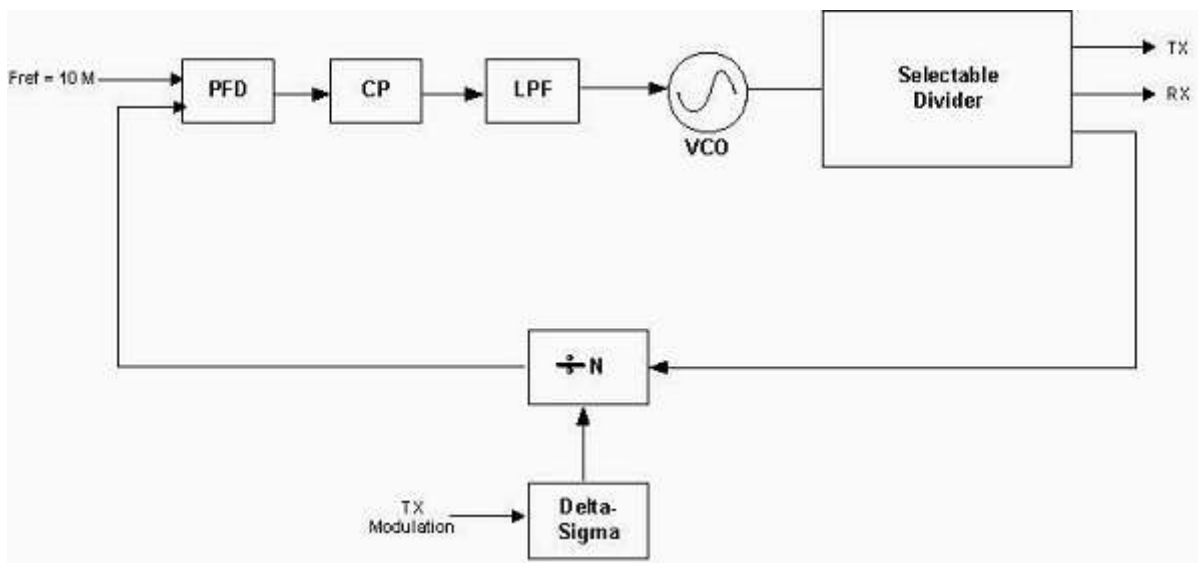
In Asynchronous mode no clock is used to synchronize the data to the internal modulator. This mode can only be used with FSK. The advantage of this mode that it saves a microcontroller pin because no data clock is required. The disadvantage is that you don't get the clean spectrum and limited BW of GFSK. If Asynchronous FSK is used the TX\_DR register should be set to its maximum value.

## 5. Internal Functional Blocks

This section provides an overview some of the key blocks of the internal radio architecture.

### 5.1. Synthesizer

An integrated Sigma Delta ( $\Sigma\Delta$ ) Fractional-N PLL synthesizer capable of operating from 240–930 MHz is provided on-chip. Using a  $\Sigma\Delta$  synthesizer has many advantages; it provides large amounts of flexibility in choosing data rate, deviation, channel frequency, and channel spacing. The transmit modulation is applied directly to the loop in the digital domain through the fractional divider which results in very precise accuracy and control over the transmit deviation. The PLL and  $\Delta-\Sigma$  modulator scheme is designed to support any desired frequency and channel spacing in the range from 240–930 MHz with a frequency resolution of 156.25 Hz (Low band) or 312.5 Hz (High band). The transmit data rate can be programmed between 1–128 kbps, and the frequency deviation can be programmed between  $\pm 1$ –160 kHz. These parameters may be adjusted via registers as shown in "3.6. Frequency Control".



**Figure 9. PLL Synthesizer Block Diagram**

The reference frequency to the PLL is 10 MHz. The PLL utilizes a differential L-C VCO, with integrated on-chip spiral inductors. The output of the VCO is followed by a configurable divider which will divide down the signal to the desired output frequency band. The modulus of this divider stage is controlled dynamically by the output from the  $\Delta-\Sigma$  modulator. The tuning resolution of the  $\Delta-\Sigma$  modulator is determined largely by the over-sampling rate and the number of bits carried internally. The tuning resolution is sufficient to tune to the commanded frequency with a maximum accuracy of 312.5 Hz anywhere in the range between 240–930 MHz.

#### 5.1.1. VCO

The output of the VCO is automatically divided down to the correct output frequency depending on the `hbsel` and `fb[4:0]` fields in "Register 75h. Frequency Band Select". A 2X VCO is utilized to help avoid problems due to frequency pulling, especially when turning on the integrated Power Amplifier. In receive mode, the LO frequency is automatically shifted downwards (without reprogramming) by the IF frequency of 937.5 kHz, allowing transmit operation on the same frequency. The VCO integrates the resonator inductor, tuning varactor, so no external VCO components are required. The VCO uses capacitance bank to cover the wide frequency range specified. The capacitance bank will automatically be calibrated every time the synthesizer is enabled. In certain fast hopping applications this might not be desirable so the VCO calibration may be skipped by setting the appropriate register.

## 5.2. Power Amplifier

The RFM42 contains an internal integrated power amplifier (PA) capable of transmitting at output levels between +8 to +17 dBm. The output power is programmable in 3 dB steps through the txpow[2:0] field in "Register 6Dh. TX Power". The RFM43 contains a PA which is capable of transmitting output levels between –8 to +13 dBm.

### 5.2.1. Output Power Selection

With the RFM42, the output power is configurable in 3 dB steps from +8 to +17 dBm with the txpow[2:0] field in "Register 6Dh. TX Power". The PA output is ramped up and down to prevent unwanted spectral splatter. The higher power setting of the module achieves maximum possible range, but of course comes at the cost of higher TX current consumption. However, depending on the duty cycle of the system, the effect on battery life may be insignificant. Contact Hoperf Support for help in evaluating this tradeoff.

The +13 dBm output power of the RFM43 is targeted at systems that require lower output power. The PA still offers high efficiency and a range of output power from –8 to +13 dBm.

| Add | R/W | Function/Description | D7 | D6 | D5 | D4 | D3 | D2       | D1       | D0       | POR Def. |
|-----|-----|----------------------|----|----|----|----|----|----------|----------|----------|----------|
| 6D  | R/W | TX Power             |    |    |    |    |    | txpow[2] | txpow[1] | txpow[0] | 07h      |

| txpow[1:0] | RFM42 Output Power |
|------------|--------------------|
| 00         | +8 dBm             |
| 01         | +11 dBm            |
| 10         | +14 dBm            |
| 11         | +17 dBm            |

| txpow[2:0] | RFM43 Output Power |
|------------|--------------------|
| 000        | –8 dBm             |
| 001        | –5 dBm             |
| 010        | –2 dBm             |
| 011        | +1 dBm             |
| 100        | +4 dBm             |
| 101        | +7 dBm             |
| 110        | +10 dBm            |
| 111        | +13 dBm            |

### 5.3. Crystal Oscillator For RF42/RF43 IC

The RF42/43 includes an integrated 30 MHz crystal oscillator with a fast start-up time of less than 600  $\mu$ s when a suitable parallel resonant crystal is used. The design is differential with the required crystal load capacitance integrated on-chip to minimize the number of external components. By default, all that is required off-chip is the 30 MHz crystal blank.

The crystal load capacitance can be digitally programmed to accommodate crystals with various load capacitance requirements and to slightly adjust the frequency of the crystal oscillator. The tuning of the crystal load capacitance is programmed through the xlc[6:0] field of "Register 09h. 30 MHz Crystal Oscillator Load Capacitance". The total internal capacitance is 12.5 pF and is adjustable in approximately 127 steps (97fF/step). The xtalshift bit is a course shift in frequency but is not binary with xlc[6:0].

The crystal load capacitance can be digitally programmed to accommodate crystals with various load capacitance requirements and to slightly adjust the frequency of the crystal oscillator. This latter function can be used to compensate for crystal production tolerances. Utilizing the on-chip temperature sensor and suitable control software even the temperature dependency of the crystal can be canceled.

The crystal load capacitance is programmed using register 09h. The typical value of the total on-chip (internal) capacitance C<sub>int</sub> can be calculated as follows:

$$C_{int} = 1.8 \text{ pF} + 0.085 \text{ pF} \times \text{xlc}[6:0] + 3.7 \text{ pF} \times \text{xtalshift}$$

Note that the course shift bit xtalshift is not binary with xlc[6:0]. The total load capacitance C<sub>load</sub> seen by the crystal can be calculated by adding the sum of all external parasitic PCB capacitances C<sub>ext</sub> to C<sub>int</sub>. If the maximum value of C<sub>int</sub> (16.3 pF) is not sufficient, an external capacitor can be added for exact tuning. See more on this, calculating C<sub>ext</sub> and crystal selection guidelines in "10. Application Notes".

If AFC is disabled then the synthesizer frequency may be further adjusted by programming the Frequency Offset field fo[9:0] in "Register 73h. Frequency Offset 1" and "Register 74h. Frequency Offset 2", as discussed in "3.6. Frequency Control".

The crystal oscillator frequency is divided down internally and may be output to the microcontroller through one of the GPIO pins for use as the System Clock. In this fashion, only one crystal oscillator is required for the entire system and the BOM cost is reduced. The available clock frequencies (i.e., internal division ratios) and the GPIO configuration are discussed further in "7.2. Microcontroller Clock".

| Add | R/W | Function/Description                | D7        | D6     | D5     | D4     | D3     | D2     | D1     | D0     | POR Def. |
|-----|-----|-------------------------------------|-----------|--------|--------|--------|--------|--------|--------|--------|----------|
| 09  | R/W | Crystal Oscillator Load Capacitance | xtalshift | xlc[6] | xlc[5] | xlc[4] | xlc[3] | xlc[2] | xlc[1] | xlc[0] | 40h      |

### 5.4. Regulators

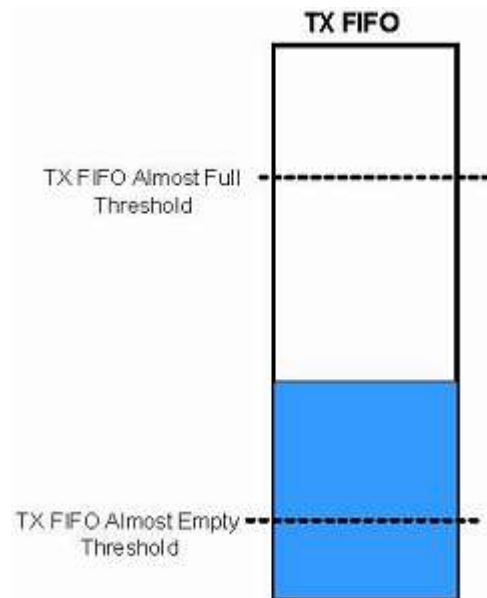
There are a total of six regulators integrated onto the RFM42/43. With the exception of the IF and Digital all regulators are designed to operate with only internal decoupling. The IF and Digital regulators both require an external 1  $\mu$ F decoupling capacitor. All of the regulators are designed to operate with an input supply voltage from +1.8 to +3.6 V, and produce a nominal regulated output voltage of +1.7 V  $\pm$ 5%. The internal circuitry nominally operates from this regulated +1.7 V supply. The output stage of the of PA is not connected internally to a regulator and is connected directly to the battery voltage.

A supply voltage should only be connected to the VDD pins. No voltage should be forced on the IF or DIG regulator outputs.

## 6. Data Handling and Packet Handler

### 6.1. TX FIFO

A 64 byte FIFO is integrated into the module for TX, as shown in Figure 10. "Register 7Fh. FIFO Access" is used to access the FIFO. A burst write, as described in "3.1. Serial Peripheral Interface (SPI)", to address 7Fh will write data to the TX FIFO.



**Figure 10. FIFO Threshold**

The TX FIFO has two programmable thresholds. An interrupt event occurs when the data in the TX FIFO reaches these thresholds. The first threshold is the FIFO Almost Full threshold, `txafthr[5:0]`. The value in this register corresponds to the desired threshold value in number of bytes. When the data being filled into the TX FIFO reaches this threshold limit, an interrupt to the microcontroller is generated so the module can enter TX mode to transmit the contents of the TX FIFO. The second threshold for TX is the FIFO Almost Empty Threshold, `txaethr[5:0]`. When the data being shifted out of the TX FIFO reaches the Almost Empty threshold an interrupt will be generated. The microcontroller will need to switch out of TX mode or fill more data into the TX FIFO. The Transmitter may be configured so that when the TX FIFO is empty the chip will automatically move to the Ready state. In this mode the TX FIFO Almost Empty Threshold may not be useful. This functionality is set by the `ffidle` bit in "Register 08h. Operating Mode and Function Control 2,".

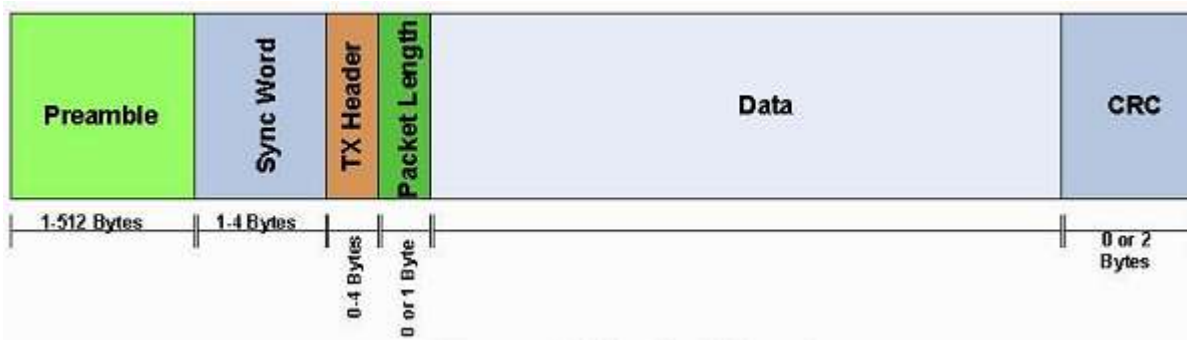
| Add | R/W | Function/Description          | D7       | D6       | D5         | D4         | D3         | D2         | D1         | D0         | POR Def. |
|-----|-----|-------------------------------|----------|----------|------------|------------|------------|------------|------------|------------|----------|
| 08  | R/W | Operating &Function Control 2 | Reserved | Reserved | Reserved   | Reserved   | autotx     | Reserved   | Reserved   | ffclrtx    | 00h      |
| 7C  | R/W | TX FIFO Control 1             |          |          | txafthr[5] | txafthr[4] | txafthr[3] | txafthr[2] | txafthr[1] | txafthr[0] | 37h      |
| 7D  | R/W | TX FIFO Control 2             |          |          | txafthr[5] | txafthr[4] | txafthr[3] | txafthr[2] | txafthr[1] | txafthr[0] | 04h      |

The TX FIFO may be cleared or reset with the ffclrtx bit in "Register 08h. Operating Mode and Function Control 2,". All interrupts may be enabled by setting the Interrupt Enabled bits in "Register 05h. Interrupt Enable 1" and "Register 06h. Interrupt Enable 2,". If the interrupts are not enabled the function will not generate an interrupt on the nIRQ pin but the bits will still be read correctly in the Interrupt Status registers.

## 6.2. Packet Configuration

When using the FIFO, automatic packet handling may be enabled for the TX mode. "Register 30h. Data Access Control" through "Register 3Eh. Packet Length," control the configuration for Packet Handling. The usual fields for network communication (such as preamble, synchronization word, headers, packet length, and CRC) can be configured to be automatically added to the data payload. The fields needed for packet generation normally change infrequently and can therefore be stored in registers. Automatically adding these fields to the data payload greatly reduces the amount of communication between the microcontroller and the RFM42/43 and therefore also reduces the required computational power of the microcontroller.

The general packet structure is shown in Figure 11. The length of each field is shown below the field. The preamble pattern is always a series of alternating ones and zeroes, starting with a one. All the fields have programmable lengths to accommodate different applications. The most common CRC polynomials are available for selection.



**Figure 11. Packet Structure**

An overview of the packet handler configuration registers is shown in Table 12. A complete register description can be found in "11.1. Complete Register Table and Descriptions".

## 6.3. Packet Handler TX Mode

If the TX packet length is set the packet handler will send the number of bytes in the packet length field before returning to ready mode and asserting the packet sent interrupt. To resume sending data from the FIFO the microcontroller needs to command the module to re-enter TX mode Figure 12 provides an example transaction where the packet length is set to three bytes.

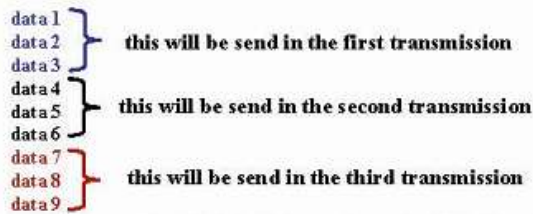


Figure 12. Multiple Packets in TX Packet Handler

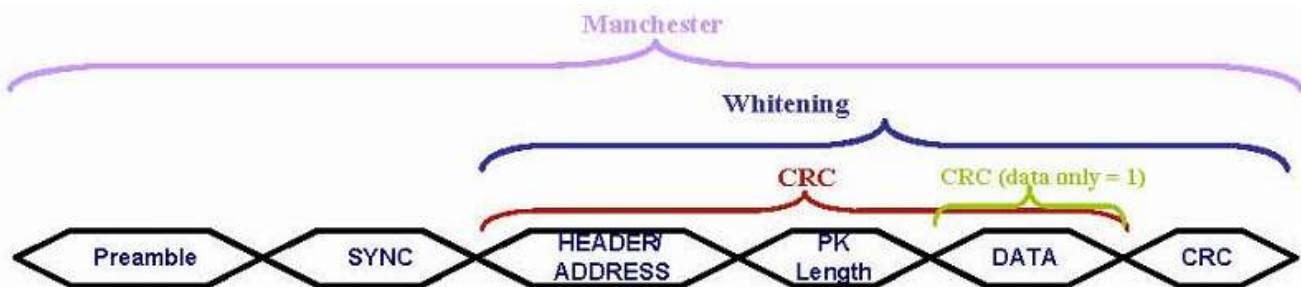
Table 12. Packet Handler Registers

| Add | R/W | Function/Description       | D7         | D6         | D5         | D4         | D3         | D2         | D1         | D0         | POR Def. |
|-----|-----|----------------------------|------------|------------|------------|------------|------------|------------|------------|------------|----------|
| 30  | R/W | Data Access Control        | enpactx    | lsbfrst    | crcdonly   | *          | enpactx    | encrc      | crc[1]     | crc[0]     | 1Dh      |
| 31  | R   | EzMAC status               | 0          | Reserved   | Reserved   | Reserved   | Reserved   | Reserved   | pktx       | pkstent    | —        |
| 32  | R/W | Header Control 1           | bcer[3]    | enbcas[2]  | enbcas[1]  | enbcas[0]  | Reserved   | Reserved   | Reserved   | Reserved   | 0Ch      |
| 33  | R/W | Header Control 2           | Reserved   | hdlen[2]   | hdlen[1]   | hdlen[0]   | fixpklen   | synclen[1] | synclen[0] | prealen[8] | 22h      |
| 34  | R/W | Preamble Length            | prealen[7] | prealen[6] | prealen[5] | prealen[4] | prealen[3] | prealen[2] | prealen[1] | prealen[0] | 07h      |
| 35  | R/W | Preamble Detection Control | preath[4]  | preath[3]  | preath[2]  | preath[1]  | preath[0]  | Reserved   | Reserved   | Reserved   | 20h      |
| 36  | R/W | Sync Word 3                | sync[31]   | sync[30]   | sync[29]   | sync[28]   | sync[27]   | sync[26]   | sync[25]   | sync[24]   | 2Dh      |
| 37  | R/W | Sync Word 2                | sync[23]   | sync[22]   | sync[21]   | sync[20]   | sync[19]   | sync[18]   | sync[17]   | sync[16]   | D4h      |
| 38  | R/W | Sync Word 1                | sync[15]   | sync[14]   | sync[13]   | sync[12]   | sync[11]   | sync[10]   | sync[9]    | sync[8]    | 00h      |
| 39  | R/W | Sync Word 0                | sync[7]    | sync[6]    | sync[5]    | sync[4]    | sync[3]    | sync[2]    | sync[1]    | sync[0]    | 00h      |
| 3A  | R/W | Transmit Header 3          | txhd[31]   | txhd[30]   | txhd[29]   | txhd[28]   | txhd[27]   | txhd[26]   | txhd[25]   | txhd[24]   | 00h      |
| 3B  | R/W | Transmit Header 2          | txhd[23]   | txhd[22]   | txhd[21]   | txhd[20]   | txhd[19]   | txhd[18]   | txhd[17]   | txhd[16]   | 00h      |
| 3C  | R/W | Transmit Header 1          | txhd[15]   | txhd[14]   | txhd[13]   | txhd[12]   | txhd[11]   | txhd[10]   | txhd[9]    | txhd[8]    | 00h      |
| 3D  | R/W | Transmit Header 0          | txhd[7]    | txhd[6]    | txhd[5]    | txhd[4]    | txhd[3]    | txhd[2]    | txhd[1]    | txhd[0]    | 00h      |
| 3E  | R/W | Transmit Packet Length     | pklen[7]   | pklen[6]   | pklen[5]   | pklen[4]   | pklen[3]   | pklen[2]   | pklen[1]   | pklen[0]   | 00h      |



## 6.4. Data Whitening, Manchester Encoding, and CRC

Data whitening can be used to avoid extended sequences of 0s or 1s in the transmitted data stream to achieve a more uniform spectrum. When enabled, the payload data bits are XORed with a pseudorandom sequence output from the built-in PN9 generator. The generator is initialized at the beginning of the payload. The receiver recovers the original data by repeating this operation. Manchester encoding can be used to ensure a dc-free transmission and good synchronization properties. When Manchester encoding is used, the effective datarate is unchanged but the actual datarate (preamble length, etc.) is doubled due to the nature of the encoding. The effective datarate when using Manchester encoding is **limited to 64 kbps**. Data Whitening and Manchester encoding can be selected with "Register 70h. Modulation Mode Control 1". The CRC is configured via "Register 30h. Data Access Control".



**Figure 13. Operation of Data Whitening, Manchester Encoding, and CRC**

## 6.5. TX Retransmission and Auto TX

The RFM42/43 is capable of automatically retransmitting the last packet in the FIFO if no additional packets were loaded into the TX FIFO. Automatic Retransmission is achieved by entering the TX state with the txon bit set. This feature is useful for Beacon transmission or when retransmission is required due to the absence of a valid acknowledgement. Only packets that fit completely in the TX FIFO are valid for retransmit. When it is necessary to transmit longer packets, the TX FIFO uses the circular read/write capability.

An Automatic Transmission is also available. When autotx = 1 the transceiver will enter automatically TX State when the TX FIFO is almost full. When the TX FIFO is empty the transceiver will automatically return to the IDLE State.

| Add | R/W | Function/Description          | D7       | D6 | D5 | D4 | D3     | D2       | D1       | D0      | POR Def. |
|-----|-----|-------------------------------|----------|----|----|----|--------|----------|----------|---------|----------|
| 08  | R/W | Operating &Function Control 2 | Reserved |    |    |    | autotx | Reserved | Reserved | ffclrtx | 00h      |



## 7. Auxiliary Functions

### 7.1. Smart Reset

The RFM42/43 contains an enhanced integrated SMART RESET or POR circuit. The POR circuit contains both a classic level threshold reset as well as a slope detector POR. This reset circuit was designed to produce reliable reset signal in any circumstances. Reset will be initiated if any of the following conditions occur:

- Initial power on, when VDD starts from 0V: reset is active till VDD reaches VRR (see table);
- When VDD decreases below VLD for any reason: reset is active till VDD reaches VRR again;
- A software reset via “Register 08h. Operating Mode and Function Control 2,”: reset is active for time  $T_{SWRST}$
- On the rising edge of a VDD glitch when the supply voltage exceeds the following time functioned limit:

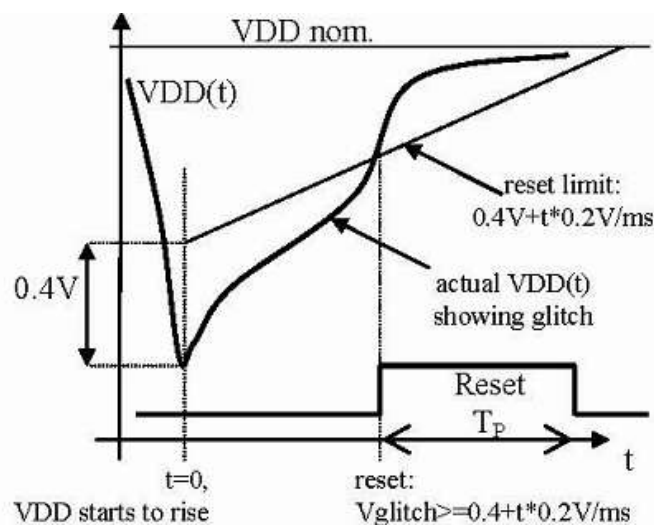


Figure 14. POR Glitch Parameters

Table 13. POR Parameters

| Parameter              | Symbol | Comment   | Min  | Typ | Max  | Unit |
|------------------------|--------|---|------|-----|------|------|
| Release Reset Voltage  | VRR    |   | 0.85 | 1.3 | 1.75 | V    |
| Power-On VDD Slope     | SVDD   | tested VDD slope region                                 | 0.03 |     | 300  | V/ms |
| Low VDD Limit          | VLD    | VLD < VRR is guaranteed                                 | 0.7  | 1   | 1.3  | V    |
| Software Reset Pulse   | TSWRST |   | 50   |     | 470  | us   |
| Threshold Voltage      | VTSD   |   |      | 0.4 |      | V    |
| Reference Slope        | k      |   |      | 0.2 |      | V/ms |
| VDD Glitch Reset Pulse | TP     | Also occurs after SDN <sub>i</sub> and initial power on | 5    | 15  | 40   | ms   |

The reset will initialize all registers to their default values. The reset signal is also available for output and use by the microcontroller by using the default setting for GPIO\_0. The inverted reset signal is available by default on GPIO\_1.

## 7.2. Microcontroller Clock

The crystal oscillator frequency is divided down internally and may be output to the microcontroller through GPIO2. This feature is useful to lower BOM cost by using only one crystal in the system. The system clock frequency is selectable from one of 8 options, as shown below. Except for the 32.768 kHz option, all other frequencies are derived by dividing the Crystal Oscillator frequency. The 32.768 kHz clock signal is derived from an internal RC Oscillator or an external 32 kHz Crystal, depending on which is selected. The GPIO2 default is the microcontroller clock with a 1 MHz microcontroller clock output.

| Add | R/W | Function/Description         | D7 | D6 | D5      | D4      | D3    | D2      | D1      | D0      | POR Def. |
|-----|-----|------------------------------|----|----|---------|---------|-------|---------|---------|---------|----------|
| A0  | R/W | Microcontroller Output Clock |    |    | clkt[1] | clkt[0] | enlfc | mclk[2] | mclk[1] | mclk[0] | 00h      |

| mclk[2:0] | Modulation Source |
|-----------|-------------------|
| 000       | 30 MHz            |
| 001       | 15 MHz            |
| 010       | 10 MHz            |
| 011       | 4 MHz             |
| 100       | 3 MHz             |
| 101       | 2 MHz             |
| 110       | 1 MHz             |
| 111       | 32.768 KHz        |

If the microcontroller clock option is being used there may be the need of a System Clock for the microcontroller while the RFM42/43 is in SLEEP mode. Since the Crystal Oscillator is disabled in SLEEP mode in order to save current, the low-power 32.768 kHz clock can be automatically switched to become the microcontroller clock. This feature is called Enable Low Frequency Clock and is enabled by the enlfc bit. When enlfc = 1 and the module is in SLEEP mode then the 32.768 kHz clock will be provided to the microcontroller as the System Clock, regardless of the setting of mclk[2:0]. For example, if mclk[2:0] = 000, 30 MHz will be provided through the GPIO output pin to the microcontroller as the System Clock in all IDLE or TX states. When the module is commanded to SLEEP mode, the System Clock will become 32.768 kHz.

Another available feature for the microcontroller clock is the Clock Tail, clkt[1:0]. If the Enable Low Frequency Clock feature is not enabled (enlfc = 0), then the System Clock to the microcontroller is disabled in SLEEP mode. However, it may be useful to provide a few extra cycles for the microcontroller to complete its operation prior to the shutdown of the System Clock signal. Setting the clkt[1:0] field will provide additional cycles of the System Clock before it shuts off.

| clkt[1:0] | Modulation Source |
|-----------|-------------------|
| 00        | 0 cycles          |
| 01        | 128 cycles        |
| 10        | 256 cycles        |
| 11        | 512 cycles        |

If an interrupt is triggered, the microcontroller clock will remain enabled regardless of the selected mode. As soon as the interrupt is read the state machine will then move to the selected mode. For instance, if the module is commanded to Sleep mode but an interrupt has occurred the 30 MHz XTAL will not disable until the interrupt has been cleared.

## 7.3. General Purpose ADC

An 8-bit SAR ADC is integrated onto the module for general purpose use, as well as for digitizing the temperature sensor reading. "Register 0Fh. ADC Configuration," must be configured depending on the use of the GP ADC before use. The architecture of the ADC is demonstrated in Figure 15. First the input of the ADC must be selected by setting the ADCSEL[2:0] depending on the use of the ADC. For instance, if the ADC is going to be used to read out the internal temperature sensor, then ADCSEL[2:0] should be set to 000. Next, the input reference voltage to the ADC must be chosen. By default, the ADC uses the bandgap voltage as a reference so the input range of the ADC is from 0–1.02 V with an LSB resolution of 4 mV (1.02/255). Changing the ADC reference will change the LSB resolution accordingly.

Every time the ADC conversion is desired, the ADCStart bit in "Register 0Fh. ADC Configuration," must be set to 1. This is a self clearing bit that will be cleared at the end of the conversion cycle of the ADC. The conversion time for the ADC is 350 us. After the 350 us or when the ADCstart/busy bit is cleared, then the ADC value may be read out of "Register 11h. ADC Value". Setting the "Register 10h. ADC Sensor Amplifier Offset", ADC Sensor Amplifier Offset is only necessary when the ADC is configured to used as a Bridge Sensor as described in the following section.

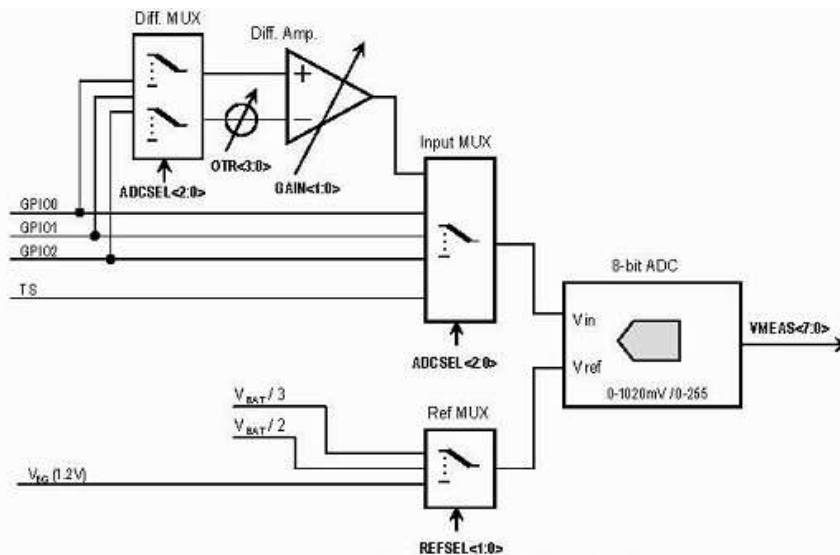
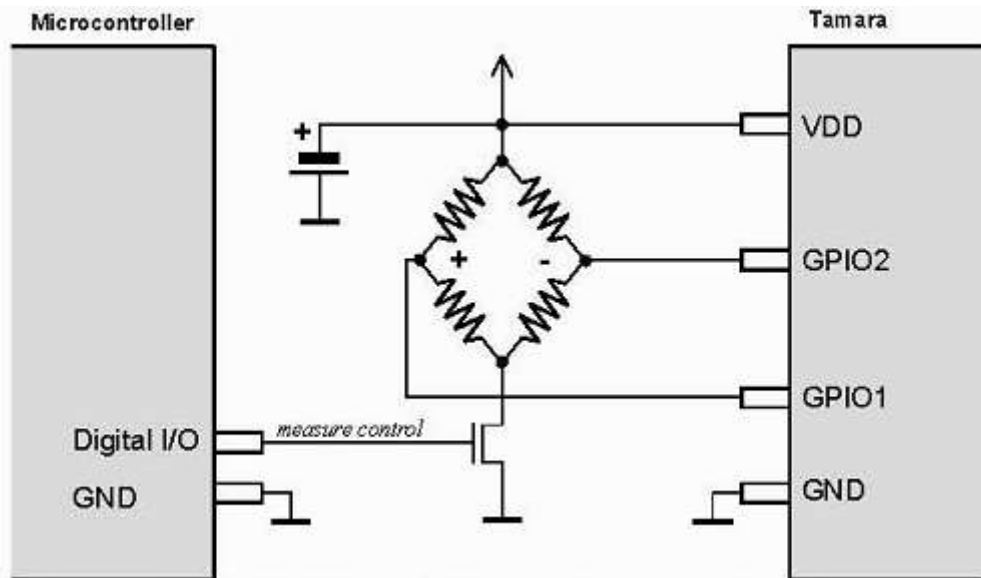


Figure 15. General Purpose ADC Architecture

| Addr | R/W | Function/Description        | D7               | D6       | D5       | D4       | D3         | D2         | D1         | D0         | POR Def. |
|------|-----|-----------------------------|------------------|----------|----------|----------|------------|------------|------------|------------|----------|
| 0F   | R/W | ADC Configuration           | adcstart/adcbusy | adcse[2] | adcse[1] | adcse[0] | adcref[1]  | adcref[0]  | adcgain[1] | adcgain[0] | 00h      |
| 10   | R/W | ADC Sensor Amplifier Offset |                  |          |          |          | adcoffs[3] | adcoffs[2] | adcoffs[1] | adcoffs[0] | 00h      |
| 11   | R   | ADC Value                   | adc[7]           | adc[6]   | adc[5]   | adc[4]   | adc[3]     | adc[2]     | adc[1]     | adc[0]     | —        |

### 7.3.1. ADC Differential Input Mode—Bridge Sensor Example

The differential input mode of ADC8 is designed to directly interface any bridge-type sensor, which is demonstrated in the figure below. As seen in the figure the use of the ADC in this configuration will utilize two GPIO pins. The supply source of the bridge and module should be the same to eliminate the measuring error caused by battery discharging. For proper operation one of the VDD dependent references (VDD/2 or VDD/3) should be selected for the reference voltage of ADC8. VDD/2 reference should be selected for VDD lower than 2.7 V, VDD/3 reference should be selected for VDD higher than 2.7 V. The differential input mode supports programmable gain to match the input range of ADC8 to the characteristic of the sensor and VDD proportional programmable offset adjustment to compensate the offset of the sensor.



**Figure 16. ADC Differential Input Example—Bridge Sensor**

The `adcgain[1:0]` bits in "Register 0Eh. I/O Port Configuration" determine the gain of the differential/single ended amplifier. This is used to fit the input range of the ADC8 to bridge sensors having different sensitivity:

| adcgain[1] | adcgain[0] | Differential Gain |               | Input Range (% of VDD) |
|------------|------------|-------------------|---------------|------------------------|
|            |            | adcref[0] = 0     | adcref[0] = 1 |                        |
| 0          | 0          | 22/13             | 33/13         | 16.7                   |
| 0          | 1          | 44/13             | 66/13         | 8.4                    |
| 1          | 0          | 66/13             | 99/13         | 5.6                    |
| 1          | 1          | 88/13             | 132/13        | 4.2                    |

**Note:** The input range is the differential voltage measured between the selected GPIO pins corresponding to the full ADC range (255).

The gain is different for different VDD dependent references so the reference change has no influence on input range and digital measured values.

The differential offset can be coarse compensated by the `adcoffs[3:0]` bits found in "Register 11h. ADC Value". Fine compensation should be done by the microcontroller software. The main reason for the offset compensation is to shift the negative offset voltage of the bridge sensor to the positive differential voltage range. This is essential as the differential input mode is unipolar. The offset compensation is VDD proportional, so the VDD change has no influence on the measured value.

| <code>adcoffs[3]</code> | Input Offset (% of VDD)                  |
|-------------------------|--|
| 0                       | 0 if <code>adcoffs[2:0] = 0</code>       |
|                         | $-(8 - \text{adcoffs}[2:0]) \times 0.12$ |
| 1                       | $\text{adcoffs}[2:0] \times 0.12$        |

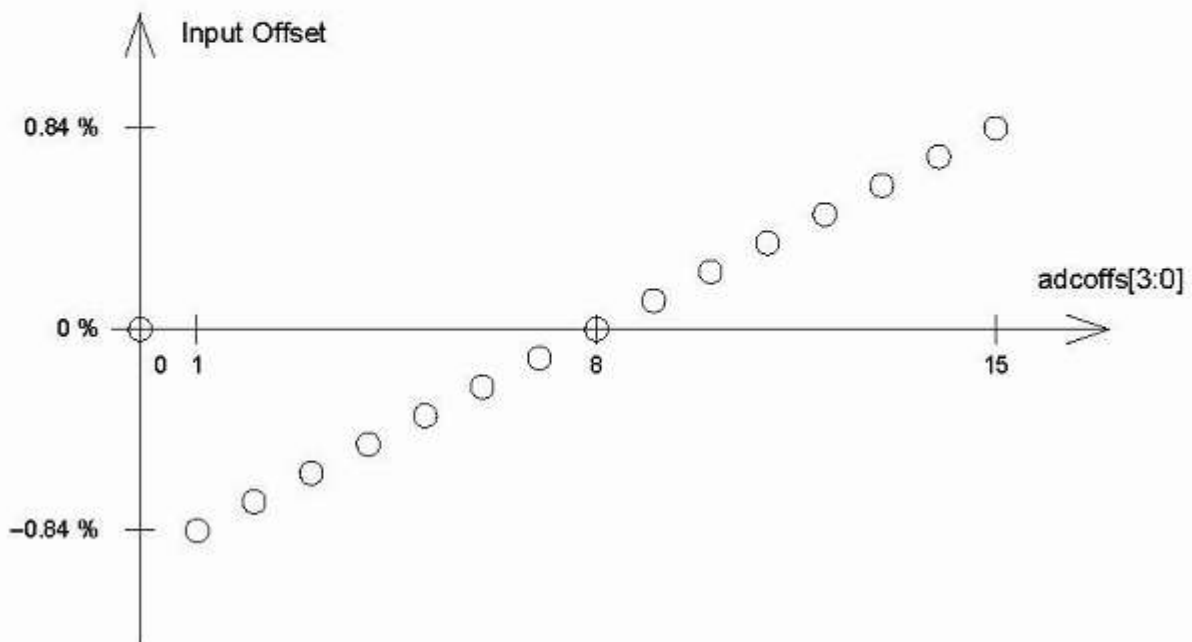


Figure 17. ADC Differential Input Offset for Sensor Offset Coarse Compensation

## 7.4. Temperature Sensor

An analog temperature sensor is integrated into the module. The temperature sensor will be automatically enabled when the temperature sensor is selected as the input of the ADC or when the analog temp voltage is selected on the analog test bus. The temperature sensor value may be digitized using the general-purpose ADC and read out over the SPI through "Register 10h. ADC Sensor Amplifier Offset". The range of the temperature sensor is selectable to configure to the desired application and performance. The table below demonstrates the settings for the different temperature ranges and performance.

To use the Temp Sensor:

1. Set input for ADC to be Temperature Sensor, "Register 0Fh. ADC Configuration"—`adcsel[2:0] = 000`
2. Set Reference for ADC, "Register 0Fh. ADC Configuration"—`adcref[1:0] = 00`
3. Set Temperature Range for ADC, "Register 12h. Temperature Sensor Calibration"—`tsrange[1:0]`
4. Set `entsoffs = 1`, "Register 12h. Temperature Sensor Calibration"
5. Trigger ADC Reading, "Register 0Fh. ADC Configuration"—`adcstart = 1`
6. Read-out Value—Read Address in "Register 11h. ADC Value"

| Add | R/W | Function/Description       | D7                      | D6                      | D5                     | D4                     | D3                      | D2                      | D1                      | D0                      | POR Def. |
|-----|-----|----------------------------|-------------------------|-------------------------|------------------------|------------------------|-------------------------|-------------------------|-------------------------|-------------------------|----------|
| 12  | R/W | Temperature Sensor Control | <code>tsrange[1]</code> | <code>tsrange[0]</code> | <code>entsoffs</code>  | <code>entstrim</code>  | <code>vbgtrim[3]</code> | <code>vbgtrim[2]</code> | <code>vbgtrim[2]</code> | <code>vbgtrim[2]</code> | 20h      |
| 13  | R/W | Temperature Value Offset   | <code>tvoffs[7]</code>  | <code>tvoffs[7]</code>  | <code>tvoffs[7]</code> | <code>tvoffs[7]</code> | <code>tvoffs[7]</code>  | <code>tvoffs[7]</code>  | <code>tvoffs[7]</code>  | <code>tvoffs[7]</code>  | 00h      |

**Table 14. Temperature Sensor Range**

| <code>entoff</code> | <code>tsrange[1]</code> | <code>tsrange[0]</code> | Temp. range   | Unit | Slope   | ADC8 LSB |
|---------------------|-------------------------|-------------------------|---------------|------|---------|----------|
| 1                   | 0                       | 0                       | -64 ... 64 °C | °C   | 8 mV/°C | 0.5 °C   |
| 1                   | 0                       | 1                       | -64 ... 192   | °C   | 4 mV/°C | 1 °C     |
| 1                   | 1                       | 0                       | 0 ... 128     | °C   | 8 mV/°C | 0.5 °C   |
| 1                   | 1                       | 1                       | -40 ... 216   | °F   | 4 mV/°F | 1 °F     |
| 0*                  | 1                       | 0                       | 0 ... 341     | °K   | 3 mV/°K | 1.333 °K |

**\*Note:** Absolute temperature mode, no temperature shift. This mode is only for test purposes. POR value of `EN_TOFF` is 1.

Control to adjust the temperature sensor accuracy is available by adjusting the bandgap voltage. By enabling the `envbgcal` and using the `vbgcal[3:0]` bits to trim the bandgap the temperature sensor accuracy may be fine tuned in the final application. The slope of the temperature sensor is very linear and monotonic but the exact accuracy or offset in temperature is difficult to control better than  $\pm 10$  °C. With the `vbgtrim` or bandgap trim though the initial temperature offset can be easily adjusted and be better than  $\pm 3$  °C.

The different ranges for the temperature sensor and ADC8 are demonstrated in Figure 18. The value of the ADC8 may be translated to a temperature reading by `ADC8Value x ADC8 LSB + Lowest Temperature in Temp Range`. For instance for a `tsrange = 00`, `Temp = ADC8Value x 0.5 - 64`.

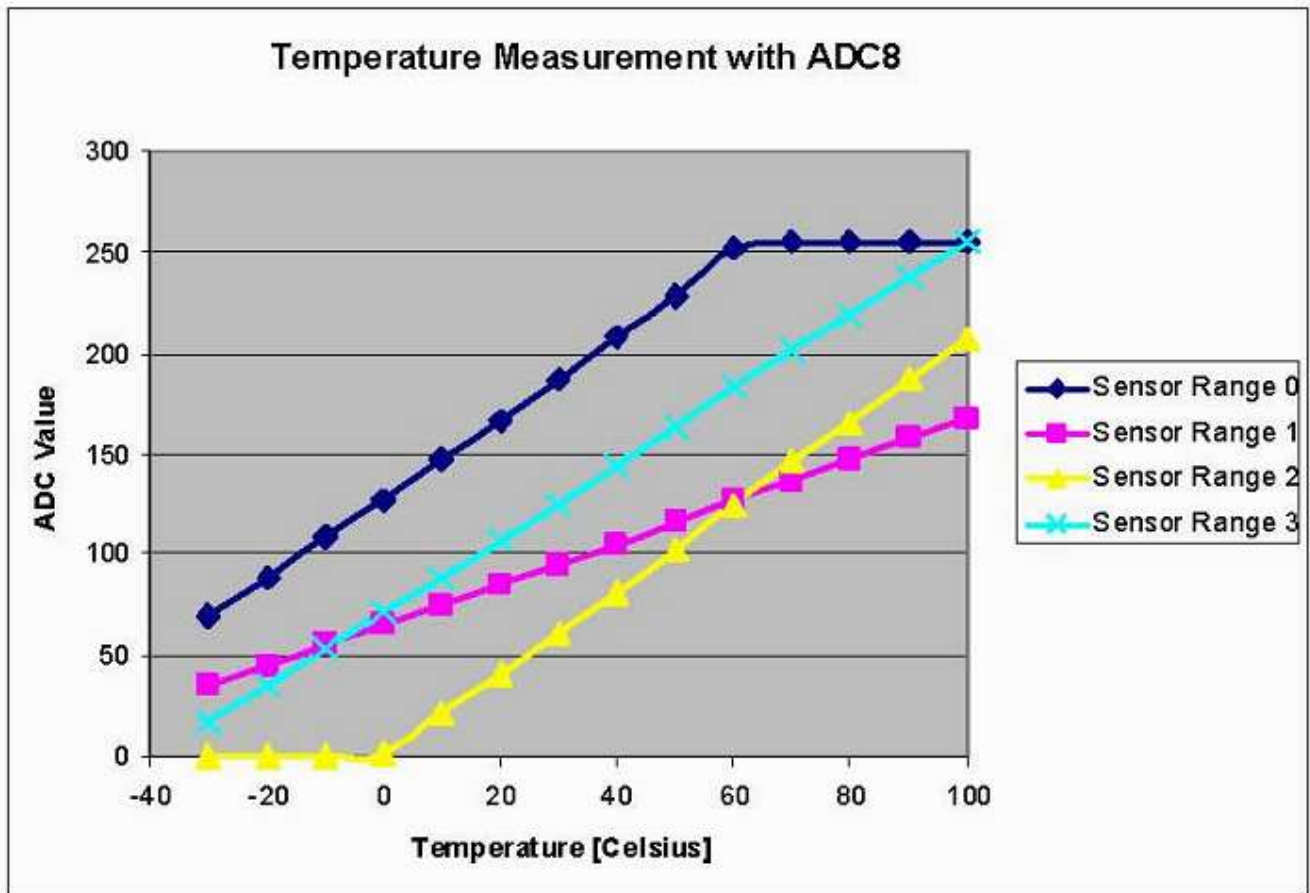


Figure 18. Temperature Ranges using ADC8



## 7.5. Low Battery Detector

A low battery detector (LBD) with digital read-out is integrated into the function is enabled by setting. A digital threshold may be programmed into the lbd[4:0] field in "Register 1Ah. Low Battery Detector Threshold". When the digitized battery voltage reaches this threshold an interrupt will be generated on the nIRQ pin to the microcontroller. The microcontroller will then need to verify the interrupt by reading "Register 03h. Interrupt/Status 1" and "Register 04h. Interrupt/Status 2.". If the LBD is enabled while the module is in SLEEP mode, it will automatically enable the RC oscillator which will periodically turn on the LBD circuit to measure the battery voltage. The battery voltage may also be read out through "Register 1Bh. Battery Voltage Level" at any time when the LBD is enabled. The Low Battery Detect function is enabled by setting enlbd=1 in "Register 07h. Operating Mode and Function Control 1".

| Ad | R/W | Function/Description           | D7 | D6 | D5 | D4      | D3      | D2      | D1      | D0      | POR Def. |
|----|-----|--------------------------------|----|----|----|---------|---------|---------|---------|---------|----------|
| 1A | R/W | Low Battery Detector Threshold |    |    |    | lbd[4]  | lbd[3]  | lbd[2]  | lbd[1]  | lbd[0]  | 14h      |
| 1B | R   | Battery Voltage Level          | 0  | 0  | 0  | vbat[4] | vbat[3] | vbat[2] | vbat[1] | vbat[0] | —        |

The LBD output is digitized by a 5-bit ADC. When the LBD function is enabled, enlbd = 1 in "Register 07h. Operating Mode and Function Control 1", the battery voltage may be read at anytime by reading "Register 1Bh. Battery Voltage Level". A Battery Voltage Threshold may be programmed to register 1Ah. When the battery voltage level drops below the battery voltage threshold an interrupt will be generated on nIRQ pin to the microcontroller if the LBD interrupt is enabled in "Register 06h. Interrupt Enable 2.". The microcontroller will then need to verify the interrupt by reading the interrupt status register, Addresses 03 and 04H. The LSB step size for the LBD ADC is 50 mV, with the ADC range demonstrated in the table below. If the LBD is enabled the LBD and ADC will automatically be enabled every 1 s for approximately 250 μs to measure the voltage which minimizes the current consumption in Sensor mode. Before an interrupt is activated four consecutive readings are required.

$$\text{BatteryVoltage}V = 1.7 + 50mV \times \text{ADCValue}$$

| ADC Value | VDD Voltage [V] |
|-----------|-----------------|
| 0         | < 1.7           |
| 1         | 1.7–1.75        |
| 2         | 1.75–1.8        |
| .....     | .....           |
| 29        | 3.1–3.15        |
| 30        | 3.15–3.2        |
| 31        | >3.2            |



## 7.6. Wake-Up Timer

The module contains an integrated wake-up timer which periodically wakes the module from SLEEP mode. The wake-up timer runs from the internal 32.768 kHz RC Oscillator. The wake-up timer can be configured to run when in SLEEP mode. If `enwt = 1` in "Register 07h. Operating Mode and Function Control 1" when entering SLEEP mode, the wake-up timer will count for a time specified by the Wake-Up Timer Period in Registers 10h–12h. At the expiration of this period an interrupt will be generated on the nIRQ pin if this interrupt is enabled. The microcontroller will then need to verify the interrupt by reading the Interrupt Status Registers 03h–04h. The wake-up timer value may be read at any time by the `wtv[15:0]` read only registers 13h–14h.

The formula for calculating the Wake-Up Period is the following:

$$WUT = \frac{32 \times M \times 2^{R-D}}{32.768} \text{ ms}$$

| WUT Register           | Description        |
|------------------------|--------------------|
| <code>wtr[3:0]</code>  | R Value in Formula |
| <code>wtd[1:0]</code>  | D Value in Formula |
| <code>wtm[15:0]</code> | M Value in Formula |

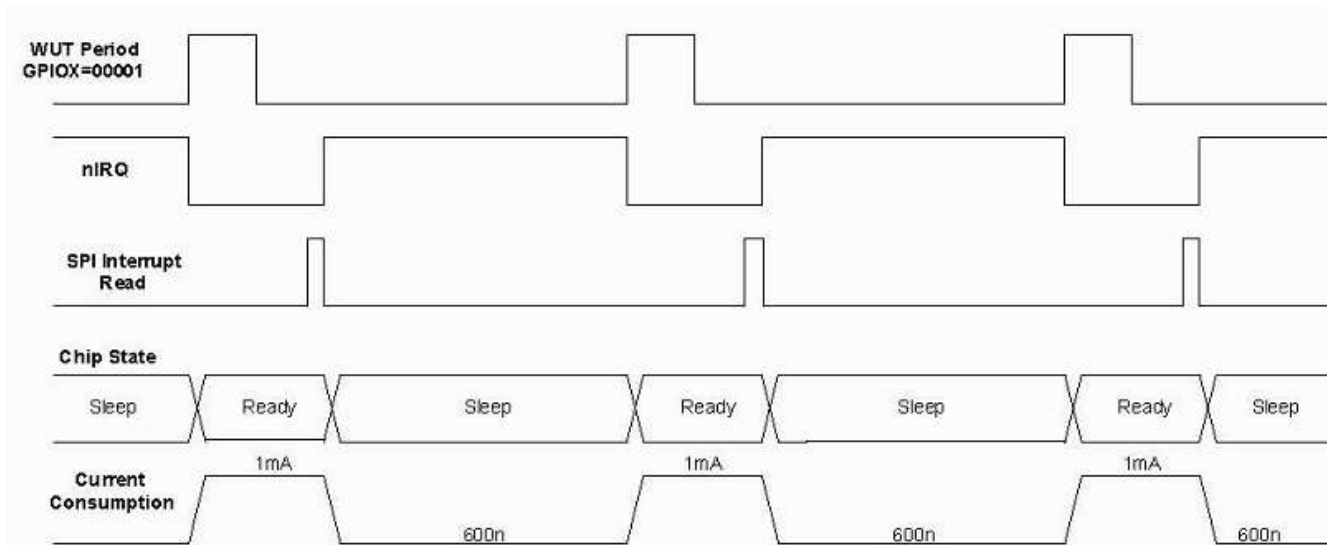
Use of the D variable in the formula is only necessary if finer resolution is required than the R value gives.

| Ad | R/W | Function/Description           | D7                   | D6                   | D5                   | D4                   | D3                   | D2                   | D1                  | D0                  | POR Def. |
|----|-----|--------------------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|---------------------|---------------------|----------|
| 14 | R/W | Wake-Up Timer Period 1         |                      |                      | <code>wtr[3]</code>  | <code>wtr[2]</code>  | <code>wtr[1]</code>  | <code>wtr[0]</code>  | <code>wtd[1]</code> | <code>wtd[0]</code> | 00h      |
| 15 | R/W | Wake-Up Timer Period 2         | <code>wtm[15]</code> | <code>wtm[14]</code> | <code>wtm[13]</code> | <code>wtm[12]</code> | <code>wtm[11]</code> | <code>wtm[10]</code> | <code>wtm[9]</code> | <code>wtm[8]</code> | 00h      |
| 16 | R/W | Wake-Up Timer Period 3         | <code>wtm[7]</code>  | <code>wtm[6]</code>  | <code>wtm[5]</code>  | <code>wtm[4]</code>  | <code>wtm[3]</code>  | <code>wtm[2]</code>  | <code>wtm[1]</code> | <code>wtm[0]</code> | 00h      |
| 17 | R   | Low Battery Detector Threshold | <code>wtv[15]</code> | <code>wtv[14]</code> | <code>wtv[13]</code> | <code>wtv[12]</code> | <code>wtv[11]</code> | <code>wtv[10]</code> | <code>wtv[9]</code> | <code>wtv[8]</code> | —        |
| 18 | R   | Battery Voltage Level          | <code>wtv[7]</code>  | <code>wtv[6]</code>  | <code>wtv[5]</code>  | <code>wtv[4]</code>  | <code>wtv[3]</code>  | <code>wtv[2]</code>  | <code>wtv[1]</code> | <code>wtv[0]</code> | —        |

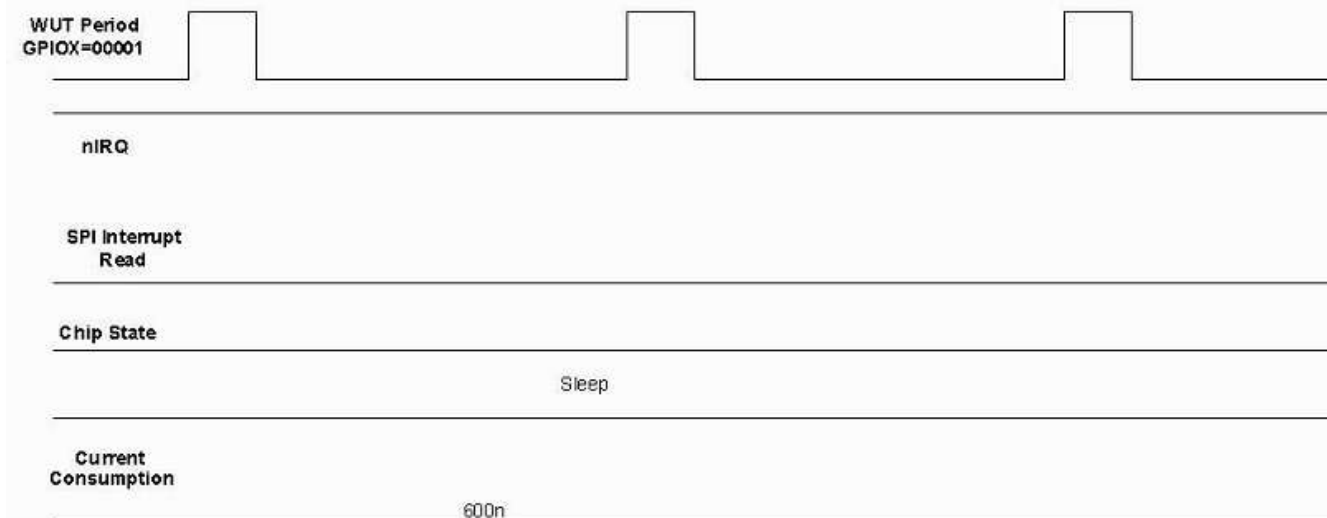
There are two different methods for utilizing the wake-up timer (WUT) depending on if the WUT interrupt is enabled in "Register 06h. Interrupt Enable 2.". If the WUT interrupt is enabled then nIRQ pin will go low when the timer expires. The module will also change state so that the 30 M XTAL is enabled so that the microcontroller clock output is available for the microcontroller to use process the interrupt. The other method of use is to not enable the WUT interrupt and use the WUT GPIO setting. In this mode of operation the module will not change state until commanded by the microcontroller. The two different modes of operation of the WUT are demonstrated in Figure 19.

A 32 kHz XTAL may also be used for better timing accuracy. By setting the `x32 ksel` bit in 07h, GPIO0 is automatically reconfigured so that an external 32 kHz XTAL may be connected to this pin. In this mode, the GPIO0 is extremely sensitive to parasitic capacitance, so only the XTAL should be connected to this pin and the XTAL should be physically located as close to the pin as possible. Once the `x32 ksel` bit is set, all internal functions such as WUT, micro-controller clock, and LDC mode will use the 32 K XTAL and not the 32 kHz RC oscillator.

**Interrupt Enable enwut=1 (Reg 06h)**



**Interrupt Enable enwut=0 (Reg 06h)**



**Figure 19. WUT Interrupt and WUT Operation**

## 7.7. GPIO Configuration

Three general purpose IOs (GPIOs) are available. Numerous functions such as specific interrupts, TRSW control, Microcontroller Output, etc. can be routed to the GPIO pins as shown in the tables below. When in Shutdown mode all the GPIO pads are pulled low.

**Note:** The ADC should not be selected as an input to the GPIO in Standby or Sleep Modes and will cause excess current consumption.

| Add | R/W | Function/Description   | D7          | D6             | D5         | D4         | D3       | D2       | D1       | D0       | POR Def. |
|-----|-----|------------------------|-------------|----------------|------------|------------|----------|----------|----------|----------|----------|
| 0B  | R/W | GPIO0 Configuration    | gpio0drv[1] | gpio0drv[1]    | pup0       | gpio0[4]   | gpio0[3] | gpio0[2] | gpio0[1] | gpio0[0] | 00h      |
| 0C  | R/W | GPIO1 Configuration    | Gpio1drv[1] | wt gpio1drv[1] | Pup1       | gpio1[4]   | gpio1[3] | gpio1[2] | gpio1[1] | gpio1[0] | 00h      |
| 0D  | R/W | GPIO2 Configuration    | Gpio2drv[1] | w gpio2drv[1]  | Pup2       | gpio2[4]   | gpio2[3] | gpio2[2] | gpio2[1] | gpio2[0] | 00h      |
| 0E  | R/W | I/O Port Configuration |             | extitst[2]     | extitst[1] | extitst[0] | itsdo    | dio2     | dio1     | dio0     | 00h      |

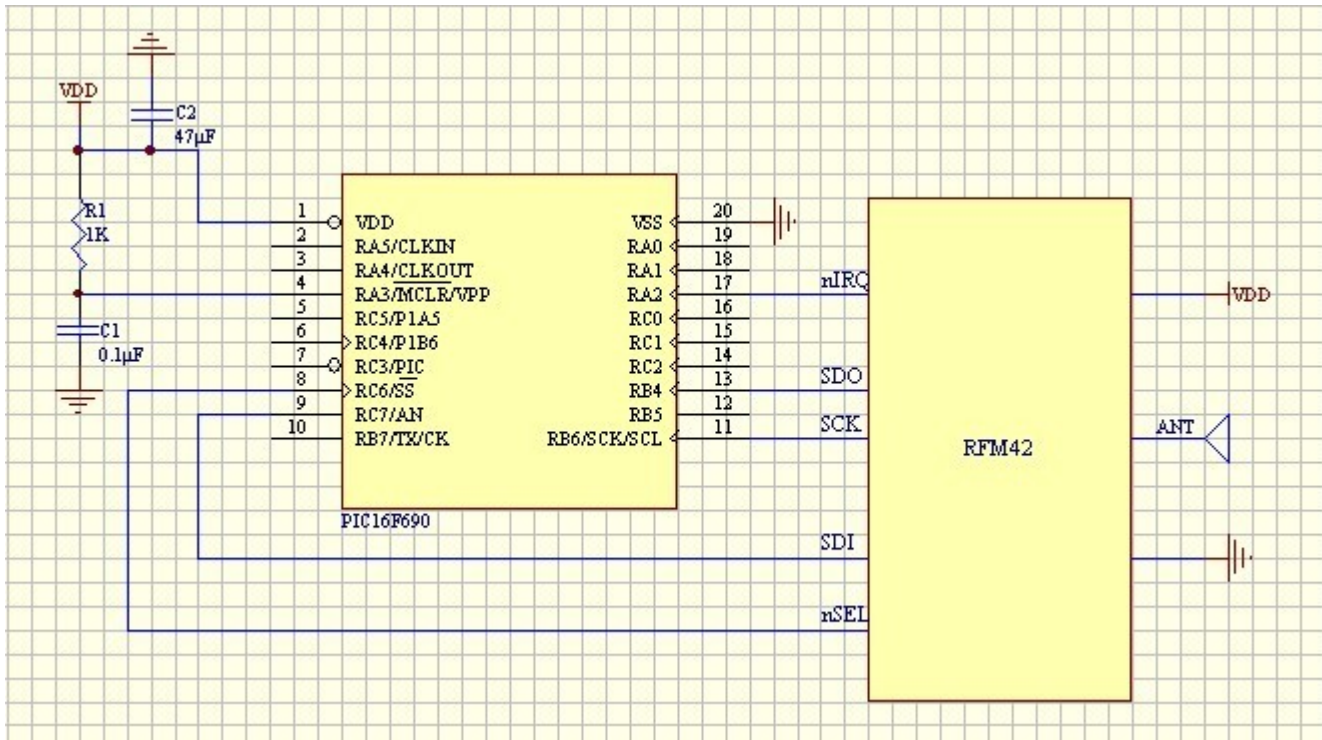
The GPIO settings for GPIO1 and GPIO2 are the same as for GPIO0 with the exception of the 00000 default setting. The default settings for each GPIO are listed below:

| GPIO  | 00000—Default Setting |
|-------|-----------------------|
| GPIO0 | POR                   |
| GPIO1 | POR Inverted          |
| GPIO2 | Microcontroller Clock |

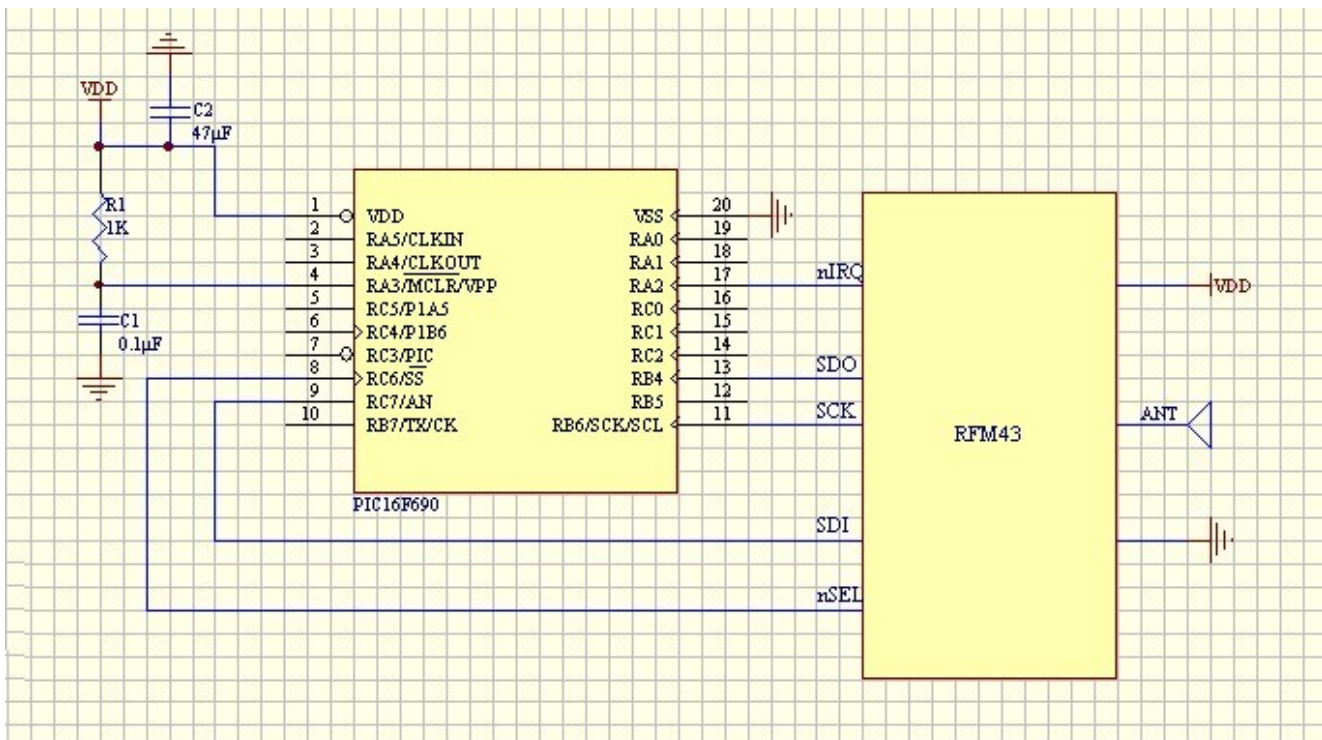
The module is configured to provide the System Clock output to the microcontroller so that only one crystal is needed in the system, therefore reducing the BOM cost. For the TX Data Source, Direct Mode is used because long packets are desired with a unique packet handling format already implemented in the microcontroller. In this configuration the TX Data Clock is configured onto GPIO0, the TX Data is configured onto GPIO1, and the Microcontroller System Clock output is configured onto GPIO2.

For a complete list of the available GPIO's see "Register 0Ch. GPIO Configuration 1," "Register 0Dh. GPIO Configuration 2," and "Register 0Eh. I/O Port Configuration,".

## 8. Reference Design



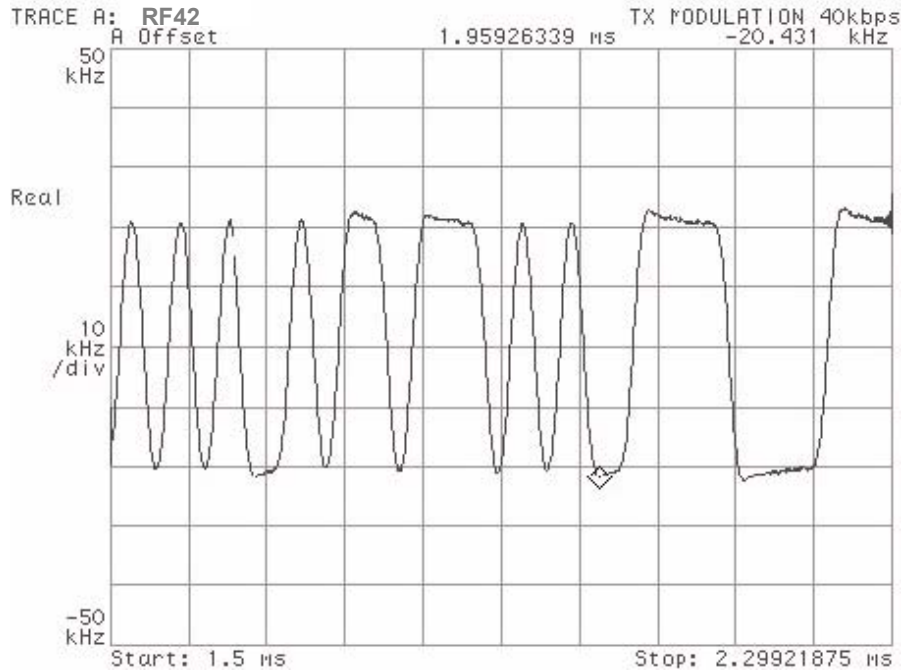
RFM42 Reference Design Schematic



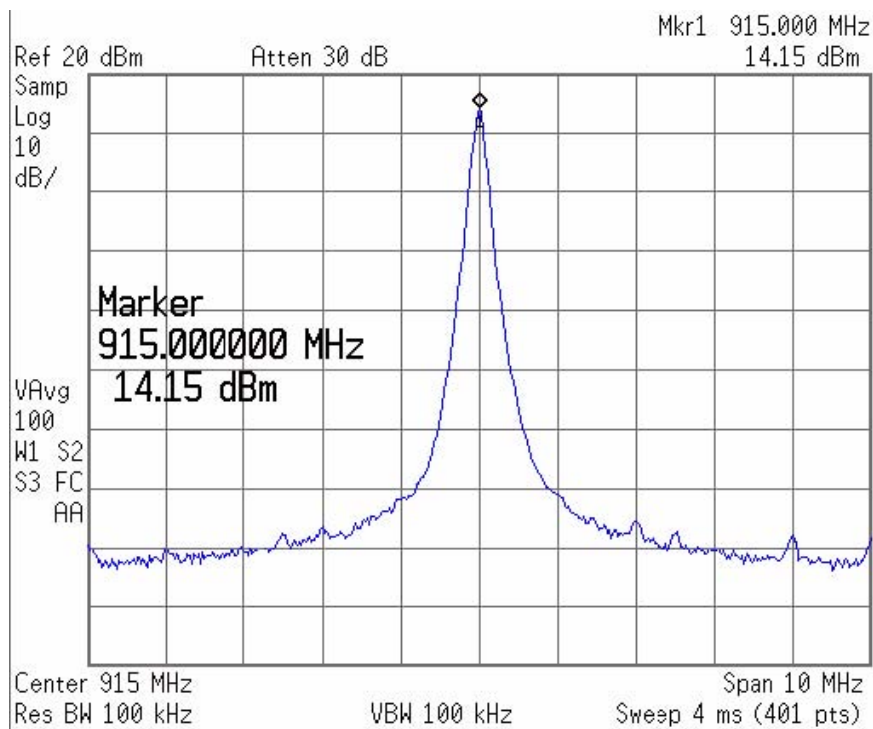
RFM43 Reference Design Schematic

**9. Measurement Results**

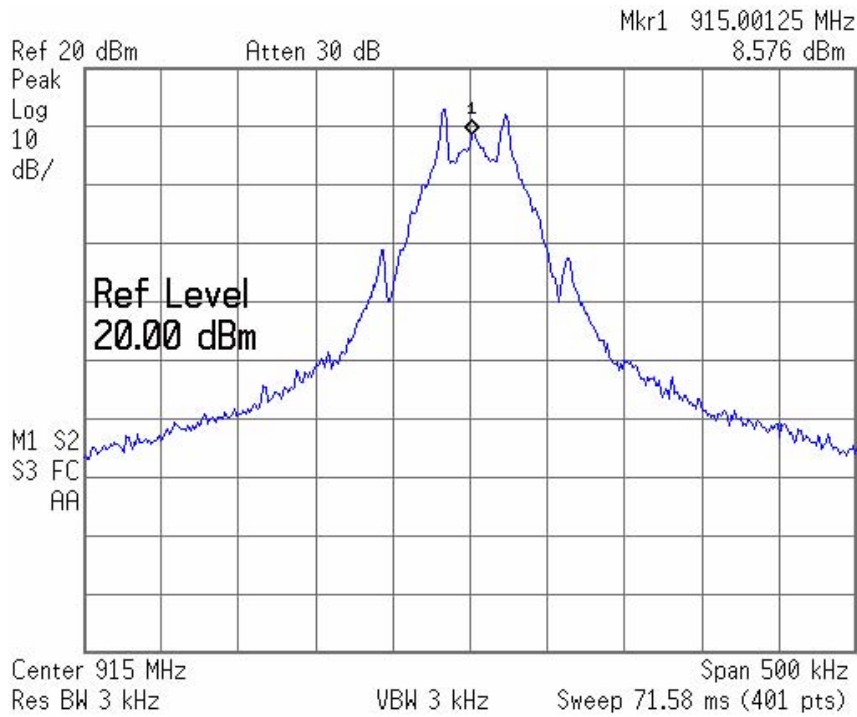
Date: 04-22-08 Time: 02:28 PM



**Figure 24. TX Modulation (40 kbps, 20 kHz Deviation)**

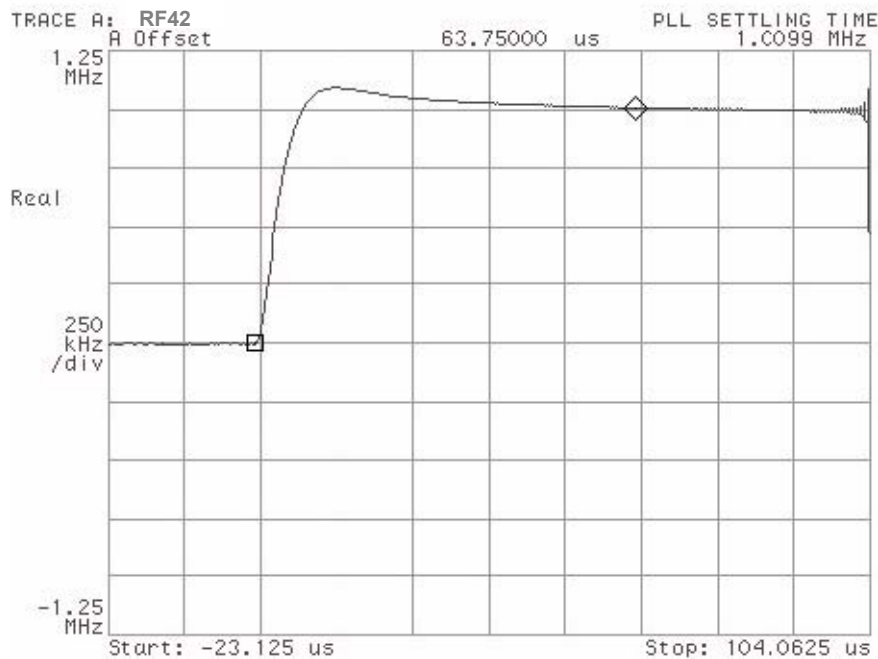


**Figure 25. RFM43 TX Unmodulated Spectrum (917 MHz)**



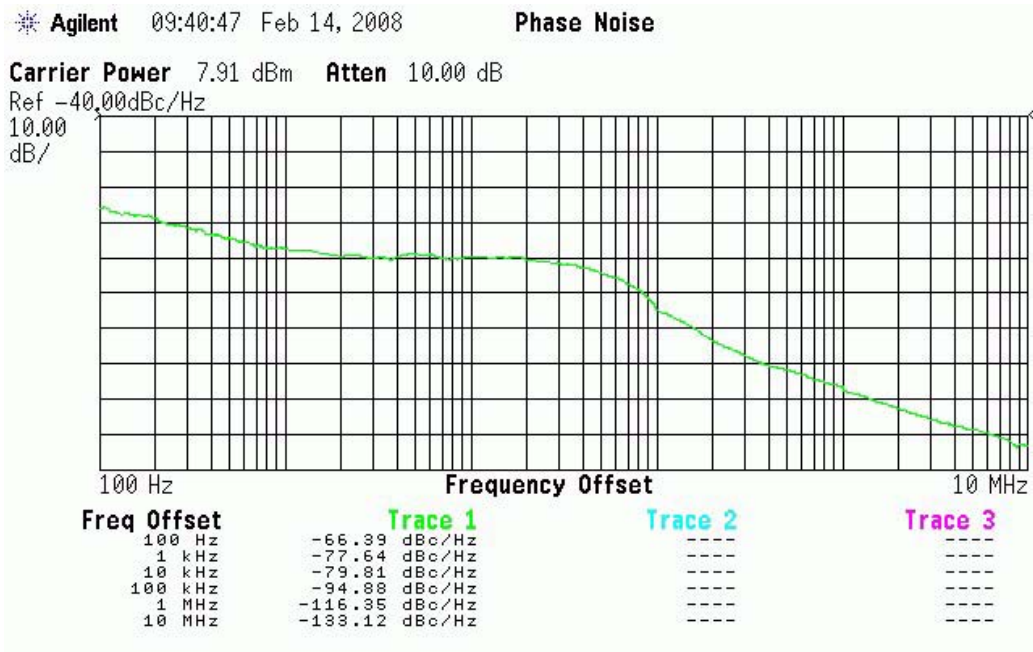
**Figure 26. RFM43 TX Modulated Spectrum (917 MHz, 40 kbps, 20 kHz Deviation, GFSK)**

**Date: 04-23-08 Time: 04:03 PM**



**Figure 27. Synthesizer Settling Time for 1 MHz Jump Settled within 10 kHz**





**Figure 28. Synthesizer Phase Noise (VCOCURR = 11)**



## 10. Reference Material

### 10.1. Complete Register Table and Descriptions

Table 17. Register Descriptions

| Add   | R/W | Function/Desc                          | Data              |              |               |               |               |               |              |                | POR Default |
|-------|-----|--|-------------------|--------------|---------------|---------------|---------------|---------------|--------------|----------------|-------------|
|       |     |  | D7                | D6           | D5            | D4            | D3            | D2            | D1           | D0             |             |
| 00    | R   | Device Type                            | 0                 | 0            | 0             | dt[4]         | dt[3]         | dt[2]         | dt[1]        | dt[0]          | —           |
| 01    | R   | Device Version                         | 0                 | 0            | 0             | vc[4]         | vc[3]         | vc[2]         | vc[1]        | vc[0]          | 04h         |
| 02    | R   | Device Status                          | ffovfl            | ffunfl       |               | headerr       | reserved      | reserved      | cps[1]       | cps[0]         | —           |
| 03    | R   | Interrupt Status 1                     | ifferr            | itxfafull    | itxfafem      | Reserved      | iext          | ipksent       | Reserved     | Reserved       | —           |
| 04    | R   | Interrupt Status 2                     | iswdet            | ipreaval     | ipreainval    | irssi         | iwut          | ilbd          | ichiprdy     | ipor           | —           |
| 05    | R/W | Interrupt Enable 1                     | enfferr           | entxfafull   | entxfafem     | enrxfafull    | enext         | enpkpsent     | enpkvalid    | enpcrerror     | 00h         |
| 06    | R/W | Interrupt Enable 2                     | enswdet           | enpreaval    | enpreainval   | enrssi        | enwut         | enlbd         | enchiprdy    | enpor          | 03h         |
| 07    | R/W | Operating & Function Control 1         | swres             | enlbd        | enwt          | x32ksel       | bxon          | rxon          | pllon        | xton           | 01h         |
| 08    | R/W | Operating & Function Control 2         | antdiv[2]         | antdiv[1]    | antdiv[0]     | rxmpk         | autotx        | enldm         | ffclrx       | ffclrx         | 00h         |
| 09    | R/W | Crystal Oscillator Load Capacitance    | xtalshft          | xic[6]       | xic[5]        | xic[4]        | xic[3]        | xic[2]        | xic[1]       | xic[0]         | 7Fh         |
| 0A    | R/W | Microcontroller Output Clock           | Reserved          | Reserved     | clkt[1]       | clkt[0]       | enlfc         | mclk[2]       | mclk[1]      | mclk[0]        | 06h         |
| 0B    | R/W | GPIO0 Configuration                    | gpio0drv[1]       | gpio0drv[0]  | pup0          | gpio0[4]      | gpio0[3]      | gpio0[2]      | gpio0[1]     | gpio0[0]       | 00h         |
| 0C    | R/W | GPIO1 Configuration                    | gpio1drv[1]       | gpio1drv[0]  | pup1          | gpio1[4]      | gpio1[3]      | gpio1[2]      | gpio1[1]     | gpio1[0]       | 00h         |
| 0D    | R/W | GPIO2 Configuration                    | gpio2drv[1]       | gpio2drv[0]  | pup2          | gpio2[4]      | gpio2[3]      | gpio2[2]      | gpio2[1]     | gpio2[0]       | 00h         |
| 0E    | R/W | I/O Port Configuration                 | Reserved          | Reserved     | extitst[2]    | extitst[1]    | extitst[0]    | itdo          | dio2         | dio1           | 00h         |
| 0F    | R/W | ADC Configuration                      | adcstar[adc-done] | adcsele[2]   | adcsele[1]    | adcsele[0]    | adcref[1]     | adcref[0]     | adcgain[1]   | adcgain[0]     | 00h         |
| 10    | R/W | ADC Sensor Amplifier Offset            | Reserved          | Reserved     | Reserved      | Reserved      | adcoffs[3]    | adcoffs[2]    | adcoffs[1]   | adcoffs[0]     | 00h         |
| 11    | R   | ADC Value                              | adc[7]            | adc[6]       | adc[5]        | adc[4]        | adc[3]        | adc[2]        | adc[1]       | adc[0]         | —           |
| 12    | R/W | Temperature Sensor Control             | tsrange[1]        | tsrange[0]   | entsoffs      | entstrim      | tstrim[3]     | tstrim[2]     | tstrim[1]    | tstrim[0]      | 20h         |
| 13    | R/W | Temperature Value Offset               | tvoffs[7]         | tvoffs[6]    | tvoffs[5]     | tvoffs[4]     | tvoffs[3]     | tvoffs[2]     | tvoffs[1]    | tvoffs[0]      | 00h         |
| 14    | R/W | Wake-Up Timer Period 1                 | Reserved          | Reserved     | Reserved      | wtr[4]        | wtr[3]        | wtr[2]        | wtr[1]       | wtr[0]         | 03h         |
| 15    | R/W | Wake-Up Timer Period 2                 | wtm[15]           | wtm[14]      | wtm[13]       | wtm[12]       | wtm[11]       | wtm[10]       | wtm[9]       | wtm[8]         | 00h         |
| 16    | R/W | Wake-Up Timer Period 3                 | wtm[7]            | wtm[6]       | wtm[5]        | wtm[4]        | wtm[3]        | wtm[2]        | wtm[1]       | wtm[0]         | 01h         |
| 17    | R   | Wake-Up Timer Value 1                  | wtv[15]           | wtv[14]      | wtv[13]       | wtv[12]       | wtv[11]       | wtv[10]       | wtv[9]       | wtv[8]         | —           |
| 18    | R   | Wake-Up Timer Value 2                  | wtv[7]            | wtv[6]       | wtv[5]        | wtv[4]        | wtv[3]        | wtv[2]        | wtv[1]       | wtv[0]         | —           |
| 19    | R/W | Low-Duty Cycle Mode Duration           | ldc[7]            | ldc[6]       | ldc[5]        | ldc[4]        | ldc[3]        | ldc[2]        | ldc[1]       | ldc[0]         | 00h         |
| 1A    | R/W | Low Battery Detector Threshold         | Reserved          | Reserved     | Reserved      | lbd[4]        | lbd[3]        | lbd[2]        | lbd[1]       | lbd[0]         | 14h         |
| 1B    | R   | Battery Voltage Level                  | 0                 | 0            | 0             | vbat[4]       | vbat[3]       | vbat[2]       | vbat[1]      | vbat[0]        | —           |
| 1C-2F |     |  | Reserved          |              |               |               |               |               |              |                |             |
| 30    | R/W | Data Access Control                    | enpacrx           | lsbrst       | crdonly       | Reserved      | enpacrx       | enrc          | crcl[1]      | crcl[0]        | 1Dh         |
| 31    | R   | EzMAC status                           | 0                 | rxrcr1       | pkscrh        | pkrx          | pkvalid       | crerror       | pktx         | pkstent        | —           |
| 32    |     |  | Reserved          |              |               |               |               |               |              |                |             |
| 33    | R/W | Header Control 2                       | Reserved          | hdlen[2]     | hdlen[1]      | hdlen[0]      | fixklen       | syncclen[1]   | syncclen[0]  | prealen[8]     | 22h         |
| 34    | R/W | Preamble Length                        | prealen[7]        | prealen[6]   | prealen[5]    | prealen[4]    | prealen[3]    | prealen[2]    | prealen[1]   | prealen[0]     | 08h         |
| 36    | R/W | Sync Word 3                            | sync[31]          | sync[30]     | sync[29]      | sync[28]      | sync[27]      | sync[26]      | sync[25]     | sync[24]       | 2Dh         |
| 37    | R/W | Sync Word 2                            | sync[23]          | sync[22]     | sync[21]      | sync[20]      | sync[19]      | sync[18]      | sync[17]     | sync[16]       | D4h         |
| 38    | R/W | Sync Word 1                            | sync[15]          | sync[14]     | sync[13]      | sync[12]      | sync[11]      | sync[10]      | sync[9]      | sync[8]        | 00h         |
| 39    | R/W | Sync Word 0                            | sync[7]           | sync[6]      | sync[5]       | sync[4]       | sync[3]       | sync[2]       | sync[1]      | sync[0]        | 00h         |
| 3A    | R/W | Transmit Header 3                      | txhd[31]          | txhd[30]     | txhd[29]      | txhd[28]      | txhd[27]      | txhd[26]      | txhd[25]     | txhd[24]       | 00h         |
| 3B    | R/W | Transmit Header 2                      | txhd[23]          | txhd[22]     | txhd[21]      | txhd[20]      | txhd[19]      | txhd[18]      | txhd[17]     | txhd[16]       | 00h         |
| 3C    | R/W | Transmit Header 1                      | txhd[15]          | txhd[14]     | txhd[13]      | txhd[12]      | txhd[11]      | txhd[10]      | txhd[9]      | txhd[8]        | 00h         |
| 3D    | R/W | Transmit Header 0                      | txhd[7]           | txhd[6]      | txhd[5]       | txhd[4]       | txhd[3]       | txhd[2]       | txhd[1]      | txhd[0]        | 00h         |
| 3E    | R/W | Transmit Packet Length                 | pklen[7]          | pklen[6]     | pklen[5]      | pklen[4]      | pklen[3]      | pklen[2]      | pklen[1]     | pklen[0]       | 00h         |
| 3F-50 |     |  | Reserved          |              |               |               |               |               |              |                |             |
| 51    | R/W | Digital Test Bus                       | Reserved          | enstest      | dtb[5]        | dtb[4]        | dtb[3]        | dtb[2]        | dtb[1]       | dtb[0]         | 00h         |
| 52    | R/W | TX Ramp Control                        | Reserved          | txmod[2]     | txmod[1]      | txmod[0]      | ldoramp[1]    | ldoramp[0]    | bramp[1]     | bramp[0]       | 2Fh         |
| 53    | R/W | PLL Tune Time                          | pllt[4]           | pllt[3]      | pllt[2]       | pllt[1]       | pllt[0]       | pllt0[2]      | pllt0[1]     | pllt0[0]       | 52h         |
| 54    | R/W | Invalid Preamble Threshold and PA Misc | Reserved          | Reserved     | inv_pre_th[3] | inv_pre_th[2] | inv_pre_th[1] | inv_pre_th[0] | ido_pa_boost | pa_vbias_boost | 14h         |
| 55    | R/W | Calibration Control                    | Reserved          | xtalstarhalf | Reserved      | enrccal       | rccal         | vcocaldp      | vcocal       | skipvco        | 44h         |
| 56    | R/W | Modem Test                             | bcrfbyp           | slicfbyp     | dttype        | oscdeten      | OOkth         | refclkssel    | refclkinv    | distogg        | 00h         |
| 57    | R/W | Chargepump Test                        | pfdrst            | fxdiv_rst    | cpforceup     | cpforcedn     | cdonly        | cdccur[2]     | cdccur[1]    | cdccur[0]      | 00h         |
| 58    | R/W | Chargepump Current Trimming/Override   | cpcurr[1]         | cpcurr[0]    | cpccorv       | cpccor[4]     | cpccor[3]     | cpccor[2]     | cpccor[1]    | cpccor[0]      | 80h         |
| 59    | R/W | Divider Current Trimming               | txcorboosten      | fbdivhc      | d3trim[1]     | d3trim[0]     | d2trim[1]     | d2trim[0]     | d1p5trim[1]  | d1p5trim[0]    | 40h         |
| 5A    | R/W | VCO Current Trimming                   | txcurboosten      | vcocorv      | vcocor[3]     | vcocor[2]     | vcocor[1]     | vcocor[0]     | vcocur[1]    | vcocur[0]      | 03h         |
| 5B    | R/W | VCO Calibration / Override             | vcocalov/vcdone   | vcocal[6]    | vcocal[5]     | vcocal[4]     | vcocal[3]     | vcocal[2]     | vcocal[1]    | vcocal[0]      | 00h         |
| 5C    | R/W | Synthesizer Test                       | dsmtd             | vcotype      | enloop        | dsmod         | dsorder[1]    | dsorder[0]    | dsrstmod     | dsrst          | 0Eh         |
| 5D    | R/W | Block Enable Override 1                | enmix             | enlna        | enpa          | enb5          | enb32         | enb12         | enmx2        | enmx2          | 00h         |
| 5E    | R/W | Block Enable Override 2                | ends              | enldet       | enmx3         | enb4          | enb3          | enb11         | enb2         | pllreset       | 40h         |
| 5F    | R/W | Block Enable Override 3                | enfrdv            | endv31       | endv2         | endv1p5       | dvbshunt      | envco         | enpc         | enbg           | 00h         |
| 60    | R/W | Channel Filter Coefficient Address     | Reserved          | Reserved     | Reserved      | Reserved      | chfladd[3]    | chfladd[2]    | chfladd[1]   | chfladd[0]     | 00h         |
| 61    | R/W | Channel Filter Coefficient Value       | Reserved          | Reserved     | chflval[5]    | chflval[4]    | chflval[3]    | chflval[2]    | chflval[1]   | chflval[0]     | 00h         |

**Table 17. Register Descriptions (Continued)**

| Add   | R/W | Function/Desc                             | Data        |          |            |            |            |                |            |            | POR Default |
|-------|-----|---|-------------|----------|------------|------------|------------|----------------|------------|------------|-------------|
|       |     |   | D7          | D6       | D5         | D4         | D3         | D2             | D1         | D0         |             |
| 62    | R/W | Crystal Oscillator / Control Test         | pwst[2]     | pwst[1]  | pwst[0]    | clkhyst    | enbias2x   | enamp2x        | bufovr     | enbuf      | 24h         |
| 63    | R/W | RC Oscillator Coarse Calibration/Override | rccov       | rcc[6]   | rcc[5]     | rcc[4]     | rcc[3]     | rcc[2]         | rcc[1]     | rcc[0]     | 00h         |
| 64    | R/W | RC Oscillator Fine Calibration/Override   | rcfov       | rcf[6]   | rcf[5]     | rcf[4]     | rcf[3]     | rcf[2]         | rcf[1]     | rcf[0]     | 00h         |
| 65    | R/W | LDO Control Override                      | enspor      | enbias   | envcoldo   | enifldo    | enrldo     | enpllldo       | endigldo   | endigpwn   | 81h         |
| 66    | R/W | LDO Level Setting                         | enovr       | enxtal   | ents       | enrc32     | Reserved   | diglvl[2]      | diglvl[1]  | diglvl[0]  | 02h         |
| 67-6A |     |   | Reserved    |          |            |            |            |                |            |            |             |
| 6B    | R/W | GFSK FIR Filter Coefficient Address       | Reserved    | Reserved | Reserved   | Reserved   | Reserved   | firadd[2]      | firadd[1]  | firadd[0]  | 00h         |
| 6C    | R/W | GFSK FIR Filter Coefficient Value         | Reserved    | Reserved | firval[5]  | firval[4]  | firval[3]  | firval[2]      | firval[1]  | firval[0]  | 01h         |
| 6D    | R/W | TX Power                                  | Reserved    | Reserved | Reserved   | Reserved   | lna_sw     | txpow[2]       | txpow[1]   | txpow[0]   | 08h         |
| 6E    | R/W | TX Data Rate 1                            | txdr[15]    | txdr[14] | txdr[13]   | txdr[12]   | txdr[11]   | txdr[10]       | txdr[9]    | txdr[8]    | 0Ah         |
| 6F    | R/W | TX Data Rate 0                            | txdr[7]     | txdr[6]  | txdr[5]    | txdr[4]    | txdr[3]    | txdr[2]        | txdr[1]    | txdr[0]    | 3Dh         |
| 70    | R/W | Modulation Mode Control 1                 | Reserved    | Reserved | txdtrscale | enphpwn    | manppol    | enmaninv       | enmanch    | enwhite    | 0Ch         |
| 71    | R/W | Modulation Mode Control 2                 | trclk[1]    | trclk[0] | dtmod[1]   | dtmod[0]   | eninv      | fd[8]          | modtyp[1]  | modtyp[0]  | 00h         |
| 72    | R/W | Frequency Deviation                       | fd[7]       | fd[6]    | fd[5]      | fd[4]      | fd[3]      | fd[2]          | fd[1]      | fd[0]      | 20h         |
| 73    | R/W | Frequency Offset 1                        | fo[7]       | fo[6]    | fo[5]      | fo[4]      | fo[3]      | fo[2]          | fo[1]      | fo[0]      | 00h         |
| 74    | R/W | Frequency Offset 2                        | Reserved    | Reserved | Reserved   | Reserved   | Reserved   | Reserved       | fo[9]      | fo[8]      | 00h         |
| 75    | R/W | Frequency Band Select                     | Reserved    | sbsel    | hbssel     | fb[4]      | fb[3]      | fb[2]          | fb[1]      | fb[0]      | 75h         |
| 76    | R/W | Nominal Carrier Frequency 1               | fc[15]      | fc[14]   | fc[13]     | fc[12]     | fc[11]     | fc[10]         | fc[9]      | fc[8]      | BBh         |
| 77    | R/W | Nominal Carrier Frequency 0               | fc[7]       | fc[6]    | fc[5]      | fc[4]      | fc[3]      | fc[2]          | fc[1]      | fc[0]      | 80h         |
| 78    | R/W | Miscellaneous Settings                    | Reserved    | Reserved | Reserved   | Reserved   | Alt_PA_Seq | rcosc[2]       | rcosc[1]   | rcosc[0]   | 09h         |
| 79    | R/W | Frequency Hopping Channel Select          | fhch[7]     | fhch[6]  | fhch[5]    | fhch[4]    | fhch[3]    | fhch[2]        | fhch[1]    | fhch[0]    | 00h         |
| 7A    | R/W | Frequency Hopping Step Size               | fhs[7]      | fhs[6]   | fhs[5]     | fhs[4]     | fhs[3]     | fhs[2]         | fhs[1]     | fhs[0]     | 00h         |
| 7B    | R/W | Turn Around and 15.4 Length Compliance    | 15.4 Length | Reserved | Reserved   | Reserved   | Reserved   | turn_around_en | Phase[1]   | Phase[0]   | 09h         |
| 7C    | R/W | TX FIFO Control 1                         | Reserved    | Reserved | txafthr[5] | txafthr[4] | txafthr[3] | txafthr[2]     | txafthr[1] | txafthr[0] | 37h         |
| 7D    | R/W | TX FIFO Control 2                         | Reserved    | Reserved | txaethr[5] | txaethr[4] | txaethr[3] | txaethr[2]     | txaethr[1] | txaethr[0] | 04h         |
| 7E    |     |   | Reserved    |          |            |            |            |                |            |            |             |
| 7F    | R/W | FIFO Access                               | fifod[7]    | fifod[6] | fifod[5]   | fifod[4]   | fifod[3]   | fifod[2]       | fifod[1]   | fifod[0]   | —           |

## Register 00h. Device Type Code (DT)

| Bit         | D7       | D6 | D5 | D4      | D3 | D2 | D1 | D0 |
|-------------|----------|----|----|---------|----|----|----|----|
| <b>Name</b> | Reserved |    |    | dt[4:0] |    |    |    |    |
| <b>Type</b> | R        |    |    | R       |    |    |    |    |

Reset value = 00000111

| Bit | Name     | Function                 |
|-----|----------|--------------------------|
| 7:5 | Reserved | <b>Reserved.</b>         |
| 4:0 | dt[4:0]  | <b>Device Type Code.</b> |

## Register 01h. Version Code (VC)

| Bit         | D7       | D6 | D5 | D4      | D3 | D2 | D1 | D0 |
|-------------|----------|----|----|---------|----|----|----|----|
| <b>Name</b> | Reserved |    |    | VC[4:0] |    |    |    |    |
| <b>Type</b> | R        |    |    | R       |    |    |    |    |

Reset value = xxxxxxxx

| Bit | Name     | Function   |
|-----|----------|--|
| 7:5 | Reserved | <b>Reserved.</b>   |
| 4:0 | VC[4:0]  | <b>Version Code.</b><br>Code indicating the version of the module.<br>Rev A0: 00100<br>Rev V2: 00011 |

## Register 02h. Device Status

| Bit         | D7     | D6     | D5       | D4       | D3       | D2       | D1       | D0     |
|-------------|--------|--------|----------|----------|----------|----------|----------|--------|
| <b>Name</b> | ffovfl | ffunfl | Reserved | Reserved | Reserved | Reserved | cps[1:0] | ffovfl |
| <b>Type</b> | R      | R      | R        | R        | R        | R        | R        | R      |

Reset value = xxxxxxxx

| Bit | Name     | Function   |
|-----|----------|--|
| 7   | ffovfl   | <b>TX</b>  |
| 6   | ffunfl   | <b>TX</b>  |
| 5:4 | Reserved | <b>Reserved.</b>   |
| 3:2 | Reserved | <b>Reserved.</b>   |
| 1:0 | cps[1:0] | <b>Module Power State.</b><br>00: Idle State<br>10: TX State |

## Register 03h. Interrupt/Status 1

| Bit         | D7     | D6         | D5       | D4       | D3   | D2      | D1       | D0       |
|-------------|--------|------------|----------|----------|------|---------|----------|----------|
| <b>Name</b> | ifferr | itxffafull | ixtffaem | Reserved | iext | ipksent | Reserved | Reserved |
| <b>Type</b> | R      | R          | R        | R        | R    | R       | R        | R        |

Reset value = xxxxxxxx

| Bit | Name       | Function   |
|-----|------------|--|
| 7   | ifferr     | <b>FIFO Underflow/Overflow Error.</b><br>When set to 1 the TX FIFO has overflowed or underflowed.  |
| 6   | itxffafull | <b>TX FIFO Almost Full.</b><br>When set to 1 the TX FIFO has met its almost full threshold and needs to be transmitted.  |
| 5   | ixtffaem   | <b>TX FIFO Almost Empty.</b><br>When set to 1 the TX FIFO is almost empty and needs to be filled.  |
| 4   | Reserved   | <b>Reserved.</b>   |
| 3   | iext       | <b>External Interrupt.</b><br>When set to 1 an interrupt occurred on one of the GPIO's if it is programmed so. The status can be checked in register 0Eh. See GPIOx Configuration section for the details. |
| 2   | ipksent    | <b>Packet Sent Interrupt.</b><br>When set to 1 a valid packet has been transmitted.  |
| 1:0 | Reserved   | <b>Reserved.</b>   |

When any of the Interrupt/Status 1 bits change state from 0 to 1 the device will notify the microcontroller by setting the nIRQ pin LOW if it is enabled in the Interrupt Enable 1 register. The nIRQ pin will go to HIGH and all the **enabled** interrupt bits will be cleared when the microcontroller reads this address. If any of these bits is not enabled in the Interrupt Enable 1 register then it becomes a status signal that can be read anytime in the same location and will not be cleared by reading the register.

**Table 18. Interrupt or Status 1 Bit Set/Clear Description**

| Bit | Status Name | Set/Clear Conditions   |
|-----|-------------|--|
| 7   | ifferr      | Set if there is a FIFO overflow or underflow. Cleared by applying FIFO reset.  |
| 6   | itxffafull  | Set when the number of bytes written to TX FIFO is greater than the Almost Full threshold. Automatically cleared at the start of transmission when the number of bytes in the FIFO is less than or equal to the threshold. |
| 5   | itxffaem    | Set when the number of bytes in the TX FIFO is less than or equal to the Almost Empty threshold. Automatically cleared when the number of data bytes in the TX FIFO is above the Almost Empty threshold.                   |
| 4   | Reserved    | <b>Reserved.</b>   |
| 3   | iext        | External interrupt source.   |
| 2   | ipksent     | Set once a packet is successfully sent (no TX abort). Cleared upon leaving FIFO mode or at the start of a new transmission.  |
| 1:0 | Reserved    | <b>Reserved.</b>   |

**Table 19. When are Individual Status Bits Set/Cleared if not Enabled as Interrupts?**

| Bit | Status Name | Set/Clear Conditions   |
|-----|-------------|--|
| 7   | ifferr      | Set if there is a FIFO Overflow or Underflow. It is cleared only by applying FIFO reset to the specific FIFO that caused the condition.  |
| 6   | itxffafull  | Will be set when the number of bytes written to TX FIFO is greater than the Almost Full threshold set by SPI. It is automatically cleared when we start transmitting and the FIFO data is read out and the number of bytes left in the FIFO is smaller or equal to the threshold).               |
| 5   | itxffaem    | Will be set when the number of bytes (not yet transmitted) in TX FIFO is smaller or equal than the Almost Empty threshold set by SPI. It is automatically cleared when we write enough data to TX FIFO so that the number of data bytes not yet transmitted is above the Almost Empty threshold. |
| 4   | Reserved    | <b>Reserved.</b>   |
| 3   | iext        | External interrupt source.   |
| 2   | ipksent     | Will go high once a packet is sent all the way through (no TX abort). This status will be cleaned if 1) We leave FIFO mode or 2) In FIFO mode we start a new transmission.   |
| 1:0 | Reserved    | <b>Reserved.</b>   |

## Register 04h. Interrupt/Status 2

| Bit         | D7       | D6 | D5 | D4 | D3   | D2   | D1       | D0   |
|-------------|----------|----|----|----|------|------|----------|------|
| <b>Name</b> | Reserved |    |    |    | iwut | ilbd | ichiprdy | ipor |
| <b>Type</b> | R        |    |    |    | R    | R    | R        | R    |

Reset value = xxxxxxxx

| Bit  | Name     | Function   |
|------|----------|--|
| 7: 4 | Reserved | <b>Reserved.</b>   |
| 3    | iwut     | <b>Wake-Up-Timer.</b><br>On the expiration of programmed wake-up timer this bit will be set to 1.  |
| 2    | ilbd     | <b>Low Battery Detect.</b><br>When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled. |
| 1    | ichiprdy | <b>Module Ready (XTAL).</b><br>When a module ready event has been detected this bit will be set to 1.  |
| 0    | ipor     | <b>Power-on-Reset (POR).</b><br>When the module detects a Power on Reset above the desired setting this bit will be set to 1.  |

When any of the Interrupt/Status Register 2 bits change state from 0 to 1 the control block will notify the microcontroller by setting the nIRQ pin LOW if it is enabled in the Interrupt Enable 2 register. The nIRQ pin will go to HIGH and all the **enabled** interrupt bits will be cleared when the microcontroller reads this address. If any of these bits is not enabled in the Interrupt Enable 2 register then it becomes a status signal that can be read anytime in the same location and will not be cleared by reading the register.



**Table 20. Interrupt or Status 2 Bit Set/Clear Description**

| Bit  | Name     | Set/Clear Conditions  |
|------|----------|---|
| 7: 4 | Reserved | <b>Reserved.</b>  |
| 3    | iwut     | Wake time timer interrupt. Use as an interrupt, not as a status.  |
| 2    | ilbd     | Low Battery Detect. When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled. Probably the status is cleared once the battery is replaced. |
| 1    | ichiprdy | Module ready goes high once we enable the xtal, TX and a settling time for the Xtal clock elapses. The status stay high unless we go back to Idle mode.   |
| 0    | ipor     | Power on status.  |

**Table 21. Detailed Description of Status Registers when not Enabled as Interrupts**

| Bit  | Name     | Set/Clear Conditions  |
|------|----------|---|
| 7: 4 | Reserved | <b>Reserved.</b>  |
| 3    | iwut     | Wake time timer interrupt. Use as an interrupt, not as a status.  |
| 2    | ilbd     | Low Battery Detect. When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled. Probably the status is cleared once the battery is replaced. |
| 1    | ichiprdy | Module ready goes high once we enable the xtal, TX and a settling time for the Xtal clock elapses. The status stay high unless we go back to Idle mode.   |
| 0    | ipor     | Power on status.  |

## Register 05h. Interrupt Enable 1

| Bit         | D7      | D6          | D5        | D4       | D3    | D2       | D1       | D0       |
|-------------|---------|-------------|-----------|----------|-------|----------|----------|----------|
| <b>Name</b> | enfferr | entxffafull | entxffaem | Reserved | enext | enpksent | Reserved | Reserved |
| <b>Type</b> | R/w     | R/w         | R/w       | R/w      | R/w   | R/w      | R/w      | R/w      |

Reset value = 00000000

| Bit | Name        | Function   |
|-----|-------------|--|
| 7   | enfferr     | <b>Enable FIFO Underflow/Overflow.</b><br>When set to 1 the FIFO Underflow/Overflow interrupt will be enabled. |
| 6   | entxffafull | <b>Enable TX FIFO Almost Full.</b><br>When set to 1 the TX FIFO Almost Full interrupt will be enabled.         |
| 5   | entxffaem   | <b>Enable TX FIFO Almost Empty.</b><br>When set to 1 the TX FIFO Almost Empty interrupt will be enabled.       |
| 4   | Reserved    | <b>Reserved.</b>   |
| 3   | enext       | <b>Enable External Interrupt.</b><br>When set to 1 the External Interrupt will be enabled.                     |
| 2   | enpksent    | <b>Enable Packet Sent.</b><br>When ipksent =1 the Packet Sense Interrupt will be enabled.                      |
| 1:0 | Reserved    | <b>Reserved.</b>   |

## Register 06h. Interrupt Enable 2

| Bit         | D7       | D6 | D5 | D4 | D3    | D2    | D1        | D0    |
|-------------|----------|----|----|----|-------|-------|-----------|-------|
| <b>Name</b> | Reserved |    |    |    | enwut | enlbd | enchiprdy | enpor |
| <b>Type</b> | R        |    |    |    | R/w   | R/w   | R/w       | R/w   |

Reset value = 00000011

| Bit | Name      | Function   |
|-----|-----------|--|
| 7:4 | Reserved  | <b>Reserved.</b>   |
| 3   | enwut     | <b>Enable Wake-Up Timer.</b><br>When set to 1 the Wake-Up Timer interrupt will be enabled.           |
| 2   | enlbd     | <b>Enable Low Battery Detect.</b><br>When set to 1 the Low Battery Detect interrupt will be enabled. |
| 1   | enchiprdy | <b>Enable Module Ready (XTAL).</b><br>When set to 1 the Module Ready interrupt will be enabled.      |
| 0   | enpor     | <b>Enable POR.</b><br>When set to 1 the POR interrupt will be enabled.                               |

## Register 07h. Operating Mode and Function Control 1

| Bit         | D7    | D6    | D5   | D4      | D3   | D2       | D1    | D0    |
|-------------|-------|-------|------|---------|------|----------|-------|-------|
| <b>Name</b> | swres | enlbd | enwt | x32ksel | txon | Reserved | pllon | xtion |
| <b>Type</b> | R/w   | R/w   | R/w  | R/w     | R/w  | R/w      | R/w   | R/w   |

Reset value = 00000001

| Bit | Name     | Function  |
|-----|----------|---|
| 7   | swres    | <b>Software Register Reset Bit.</b><br>This bit may be used to reset all registers simultaneously to a DEFAULT state, without the need for sequentially writing to each individual register. The RESET is accomplished by setting swres = 1. This bit will be automatically cleared.  |
| 6   | enlbd    | <b>Enable Low Battery Detect.</b><br>When this bit is set to 1 the Low Battery Detector circuit and threshold comparison will be enabled.   |
| 5   | enwt     | <b>Enable Wake-Up-Timer.</b><br>Enabled when enwt = 1. If the Wake-up-Timer function is enabled it will operate in any mode and notify the microcontroller through the GPIO interrupt when the timer expires.   |
| 4   | x32ksel  | <b>32,768 kHz Crystal Oscillator Select.</b><br>0: RC oscillator<br>1: 32 kHz crystal   |
| 3   | txon     | <b>TX on in Manual Transmit Mode.</b><br>Automatically cleared in FIFO mode once the packet is sent. Transmission can be aborted during packet transmission, however, when no data has been sent yet, transmission can only be aborted after the device is programmed to "unmodulated carrier" ("Register 71h. Modulation Mode Control 2"). |
| 2   | Reserved | <b>Reserved.</b>  |
| 1   | pllon    | <b>TUNE Mode (PLL is ON).</b><br>When pllon = 1 the PLL will remain enabled in Idle State. This will for faster turn-around time at the cost of increased current consumption in Idle State.  |
| 0   | xtion    | <b>READY Mode (Xtal is ON).</b>   |

## Register 08h. Operating Mode and Function Control 2

| Bit         | D7       | D6 | D5 | D4 | D3     | D2       | D1  | D0      |
|-------------|----------|----|----|----|--------|----------|-----|---------|
| <b>Name</b> | Reserved |    |    |    | autotx | Reserved |     | ffclrtx |
| <b>Type</b> | R/w      |    |    |    | R/w    | R/w      | R/w | R/w     |

Reset value = 00000000

| Bit  | Name     | Function   |
|------|----------|--|
| 7: 4 | Reserved | <b>Reserved.</b>   |
| 3    | autotx   | <b>Automatic Transmission.</b><br>When autotx = 1 the transceiver will enter automatically TX State when the FIFO is almost full. When the FIFO is empty it will automatically return to the Idle State. |
| 2: 1 | Reserved | <b>Reserved.</b>   |
| 0    | ffclrtx  | <b>TX FIFO Reset/Clear.</b><br>This has to be a two writes operation: Setting ffclrtx =1 followed by ffclrtx = 0 will clear the contents of the TX FIFO.   |

## Register 09h. 30 MHz Crystal Oscillator Load Capacitance

| Bit         | D7       | D6       | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----|----|----|----|----|----|
| <b>Name</b> | xtalshft | xlc[6:0] |    |    |    |    |    |    |
| <b>Type</b> | R/w      | R/w      |    |    |    |    |    |    |

Reset value = 01111111

| Bit | Name     | Function   |
|-----|----------|--|
| 7   | xtalshft | Additional capacitance to course shift the frequency if xlc[6:0] is not sufficient.<br>Not binary with xlc[6:0]. |
| 6:0 | xlc[6:0] | <b>Tuning Capacitance for the 30 MHz XTAL.</b>   |

## Register 0Ah. Microcontroller Output Clock

| Bit         | D7       | D6 | D5        | D4 | D3    | D2        | D1 | D0 |
|-------------|----------|----|-----------|----|-------|-----------|----|----|
| <b>Name</b> | Reserved |    | clkt[1:0] |    | enlfc | mclk[2:0] |    |    |
| <b>Type</b> | R        |    | R/w       |    | R/w   | R/w       |    |    |

Reset value = xx000110

| Bit | Name      | Function   |
|-----|-----------|--|
| 7:6 | Reserved  | <b>Reserved.</b>   |
| 5:4 | clkt[1:0] | <p><b>Clock Tail.</b><br/>If enlfc = 0 then it can be useful to provide a few extra cycles for the microcontroller to complete its operation. Setting the clkt[1:0] register will provide the addition cycles of the clock before it shuts off.</p> <p>00: 0 cycle<br/>01: 128 cycles<br/>10: 256 cycles<br/>11: 512 cycles</p>  |
| 3   | enlfc     | <p><b>Enable Low Frequency Clock.</b><br/>When enlfc = 1 and the module is in Sleep mode then the 32.768 kHz clock will be provided to the microcontroller no matter what the selection of mclk[2:0] is. For example if mclk[2:0] = '000', 30 MHz will be available through the GPIO to output to the microcontroller in all Idle or TX states. When the module is commanded to Sleep mode the 30 MHz clock will become 32.768 kHz.</p>                              |
| 2:0 | mclk[2:0] | <p><b>Microcontroller Clock.</b><br/>Different clock frequencies may be selected for configurable GPIO clock output. All clock frequencies are created by dividing the XTAL except for the 32 kHz clock which comes directly from the 32 kHz RC Oscillator. The mclk[2:0] setting is only valid when xton = 1 except the 111.</p> <p>000: 30 MHz<br/>001: 15 MHz<br/>010: 10 MHz<br/>011: 4 MHz<br/>100: 3 MHz<br/>101: 2 MHz<br/>110: 1 MHz<br/>111: 32.768 kHz</p> |

## Register 0Bh. GPIO Configuration 0

| Bit         | D7            | D6 | D5   | D4         | D3 | D2 | D1 | D0 |
|-------------|---------------|----|------|------------|----|----|----|----|
| <b>Name</b> | gpiodrv0[1:0] |    | pup0 | gpio0[4:0] |    |    |    |    |
| <b>Type</b> | R/w           |    | R/w  | R/w        |    |    |    |    |

Reset value = 00000000

| Bit | Name          | Function   |
|-----|---------------|--|
| 7:6 | gpiodrv0[1:0] | <b>GPIO Driving Capability Setting.</b>  |
| 5   | pup0          | <b>Pullup Resistor Enable on GPIO0.</b><br>When set to 1 the a 200 k $\Omega$ resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.   |
| 4:0 | gpio0[4:0]    | <b>GPIO0 pin Function Select.</b><br>00000: Power-On-Reset (output)<br>00001: Wake-Up Timer: 1 when WUT has expired (output)<br>00010: Low Battery Detect: 1 when battery is below threshold setting (output)<br>00011: Direct Digital Input<br>00100: External Interrupt, falling edge (input)<br>00101: External Interrupt, rising edge (input)<br>00110: External Interrupt, state change (input)<br>00111: ADC Analog Input<br>01000: Reserved (Analog Test N Input)<br>01001: Reserved (Analog Test P Input)<br>01010: Direct Digital Output<br>01011: Reserved (Digital Test Output)<br>01100: Reserved (Analog Test N Output)<br>01101: Reserved (Analog Test P Output)<br>01110: Reference Voltage (output)<br>01111: TX Data CLK output to be used in conjunction with TX Data pin (output)<br>10000: TX Data input for direct modulation (input)<br>10001: External Retransmission Request (input)<br>10010: TX State (output)<br>10011: TX FIFO Almost Full (output)<br>10100: Reserved<br>10101: Reserved<br>10110: Reserved<br>10111: Reserved<br>11000: Reserved<br>11001: Reserved<br>11010: Reserved<br>11011: Reserved<br>11100: Reserved<br>11101: VDD<br>else : GND |



## Register 0Ch. GPIO Configuration 1

| Bit         | D7            | D6 | D5   | D4         | D3 | D2 | D1 | D0 |
|-------------|---------------|----|------|------------|----|----|----|----|
| <b>Name</b> | gpiodrv1[1:0] |    | pup1 | Gpio1[4:0] |    |    |    |    |
| <b>Type</b> | R/W           |    | R/W  | R/W        |    |    |    |    |

Reset value = 00000000

| Bit | Name          | Function  |
|-----|---------------|---|
| 7:6 | gpiodrv1[1:0] | <b>GPIO Driving Capability Setting.</b>   |
| 5   | Pup1          | <b>Pullup Resistor Enable on GPIO1.</b><br>When set to 1 the a 200 k $\Omega$ resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.  |
| 4:0 | gpio1[4:0]    | <b>GPIO1 pin Function Select.</b><br>00000: Inverted Power-On-Reset (output)<br>00001: Wake-Up Timer: 1 when WUT has expired (output)<br>00010: Low Battery Detect: 1 when battery is below threshold setting (output)<br>00011: Direct Digital Input<br>00100: External Interrupt, falling edge (input)<br>00101: External Interrupt, rising edge (input)<br>00110: External Interrupt, state change (input)<br>00111: ADC Analog Input<br>01000: Reserved (Analog Test N Input)<br>01001: Reserved (Analog Test P Input)<br>01010: Direct Digital Output<br>01011: Reserved (Digital Test Output)<br>01100: Reserved (Analog Test N Output)<br>01101: Reserved (Analog Test P Output)<br>01110: Reference Voltage (output)<br>01111: TX Data CLK output to be used in conjunction with TX Data pin (output)<br>10000: TX Data input for direct modulation (input)<br>10001: External Retransmission Request (input)<br>10010: TX State (output)<br>10011: TX FIFO Almost Full (output)<br>10100: Reserved<br>10101: Reserved<br>10110: Reserved<br>10111: Reserved<br>11000: Reserved<br>11001: Reserved<br>11010: Reserved<br>11011: Reserved<br>11100: Reserved<br>11101: VDD<br>else : GND |

## Register 0Ch. GPIO Configuration 2

| Bit         | D7            | D6 | D5   | D4         | D3 | D2 | D1 | D0 |
|-------------|---------------|----|------|------------|----|----|----|----|
| <b>Name</b> | gpiodrv2[1:0] |    | pup2 | Gpio2[4:0] |    |    |    |    |
| <b>Type</b> | R/W           |    | R/W  | R/W        |    |    |    |    |

Reset value = 00000000

| Bit | Name          | Function  |
|-----|---------------|---|
| 7:6 | gpiodrv2[1:0] | <b>GPIO Driving Capability Setting.</b>   |
| 5   | Pup2          | <b>Pullup Resistor Enable on GPIO2.</b><br>When set to 1 the a 200 k $\Omega$ resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.  |
| 4:0 | gpio2[4:0]    | <b>GPIO1 pin Function Select.</b><br>00000: Inverted Power-On-Reset (output)<br>00001: Wake-Up Timer: 1 when WUT has expired (output)<br>00010: Low Battery Detect: 1 when battery is below threshold setting (output)<br>00011: Direct Digital Input<br>00100: External Interrupt, falling edge (input)<br>00101: External Interrupt, rising edge (input)<br>00110: External Interrupt, state change (input)<br>00111: ADC Analog Input<br>01000: Reserved (Analog Test N Input)<br>01001: Reserved (Analog Test P Input)<br>01010: Direct Digital Output<br>01011: Reserved (Digital Test Output)<br>01100: Reserved (Analog Test N Output)<br>01101: Reserved (Analog Test P Output)<br>01110: Reference Voltage (output)<br>01111: TX Data CLK output to be used in conjunction with TX Data pin (output)<br>10000: TX Data input for direct modulation (input)<br>10001: External Retransmission Request (input)<br>10010: TX State (output)<br>10011: TX FIFO Almost Full (output)<br>10100: Reserved<br>10101: Reserved<br>10110: Reserved<br>10111: Reserved<br>11000: Reserved<br>11001: Reserved<br>11010: Reserved<br>11011: Reserved<br>11100: Reserved<br>11101: VDD<br>else : GND |

## Register 0Eh. I/O Port Configuration

| Bit         | D7       | D6         | D5         | D4         | D3    | D2   | D1   | D0   |
|-------------|----------|------------|------------|------------|-------|------|------|------|
| <b>Name</b> | Reserved | extitst[2] | extitst[1] | extitst[0] | itsdo | dio2 | dio1 | dio0 |
| <b>Type</b> | R        | R          | R          | R          | R/w   | R/w  | R/w  | R/w  |

Reset value = 00000000

| Bit | Name       | Function   |
|-----|------------|--|
| 7   | Reserved   | <b>Reserved</b>  |
| 6   | extitst[2] | <b>External Interrupt Status.</b><br>If the GPIO2 is programmed to be external interrupt sources then the status can be read here.   |
| 5   | extitst[1] | <b>External Interrupt Status.</b><br>If the GPIO1 is programmed to be external interrupt sources then the status can be read here.   |
| 4   | extitst[0] | <b>External Interrupt Status.</b><br>If the GPIO0 is programmed to be external interrupt sources then the status can be read here.   |
| 3   | itsdo      | <b>Interrupt Request Output on the SDO Pin.</b><br>nIRQ output is present on the SDO pin if this bit is set and the nSEL input is inactive (high).   |
| 2   | dio2       | <b>Direct I/O for GPIO2.</b><br>If the GPIO2 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO2 is configured to be a direct input then the value of the pin can be read here. |
| 1   | dio1       | <b>Direct I/O for GPIO1.</b><br>If the GPIO1 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO1 is configured to be a direct input then the value of the pin can be read here. |
| 0   | dio0       | <b>Direct I/O for GPIO0.</b><br>If the GPIO0 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO0 is configured to be a direct input then the value of the pin can be read here. |

## Register 0Fh. ADC Configuration

| Bit         | D7                   | D6          | D5 | D4 | D3          | D2  | D1           | D0  |
|-------------|----------------------|-------------|----|----|-------------|-----|--------------|-----|
| <b>Name</b> | adcstart/<br>adcdone | adcsel[2:0] |    |    | adcref[1:0] |     | adcgain[1:0] |     |
| <b>Type</b> | R                    | R           | R  | R  | R/W         | R/W | R/W          | R/W |

Reset value = 00000000

| Bit | Name             | Function  |
|-----|------------------|---|
| 7   | adcstart/adcdone | <b>ADC Measurement Start Bit.</b><br>Reading this bit gives 1 if the ADC measurement cycle has been finished.   |
| 6:4 | adcsel[2:0]      | <b>ADC Input Source Selection.</b><br>The internal 8-bit ADC input source can be selected as follows:<br>000: Internal Temperature Sensor<br>001: GPIO0, single-ended<br>010: GPIO1, single-ended<br>011: GPIO2, single-ended<br>100: GPIO0(+) – GPIO1(-), differential<br>101: GPIO1(+) – GPIO2(-), differential<br>110: GPIO0(+) – GPIO2(-), differential<br>111: GND |
| 3:2 | adcref[1:0]      | <b>ADC Reference Voltage Selection.</b><br>The reference voltage of the internal 8-bit ADC can be selected as follows:<br>0X: bandgap voltage (1.2 V)<br>10: VDD / 3<br>11: VDD / 2   |
| 1:0 | adcgain[1:0]     | <b>ADC Sensor Amplifier Gain Selection.</b><br>The full scale range of the internal 8-bit ADC in differential mode (see adcsel) can be set as follows:<br>adcref[0] = 0:    adcref[0] = 1:<br>FS = 0.014 x (adcgain[1:0] + 1) x VDD    FS = 0.021 x (adcgain[1:0] + 1) x VDD  |

## Register 10h. ADC Sensor Amplifier Offset

| Bit         | D7       | D6 | D5 | D4 | D3           | D2 | D1 | D0 |
|-------------|----------|----|----|----|--------------|----|----|----|
| <b>Name</b> | Reserved |    |    |    | adcoffs[3:0] |    |    |    |
| <b>Type</b> | R        |    |    |    | R/w          |    |    |    |

Reset value = xxxx0000

| Bit   | Name         | Function                             |
|---|--------------|--------------------------------------|
| 7: 4  | Reserved     | <b>Reserved.</b>                     |
| 3: 0  | adcoffs[3:0] | <b>ADC Sensor Amplifier Offset*.</b> |
| *Note: The offset can be calculated as $\text{Offset} = \text{adcoffs}[2:0] \times \text{VDD} / 1000$ ; MSB = $\text{adcoffs}[3]$ = Sign bit. |              |                                      |

## Register 11h. ADC Value

| Bit         | D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----|----|----|----|----|----|----|
| <b>Name</b> | adc[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R        |    |    |    |    |    |    |    |

Reset value = xxxxxxxx

| Bit  | Name     | Function                                |
|------|----------|---|
| 7: 0 | adc[7:0] | <b>Internal 8 bit ADC Output Value.</b> |

## Register 12h. Temperature Sensor Calibration

| Bit         | D7           | D6 | D5       | D4       | D3          | D2 | D1 | D0 |
|-------------|--------------|----|----------|----------|-------------|----|----|----|
| <b>Name</b> | tsrange[1:0] |    | entsoffs | entstrim | tstrim[3:0] |    |    |    |
| <b>Type</b> | R/w          |    | R/w      | R/w      | R/w         |    |    |    |

Reset value = 00100000

| Bit  | Name         | Function   |
|------|--------------|--|
| 7: 6 | tsrange[1:0] | <b>Temperature Sensor Range Selection.</b><br>(FS range is 0..1024 mV)<br>00: -40°C .. 64°C (full operating range), with 0.5°C resolution (1 LSB in the 8-bit ADC)<br>01: -40°C ... 85°C, with 1°C resolution (1 LSB in the 8-bit ADC)<br>11: 0 °C ... 85°C, with 0.5°C resolution (1 LSB in the 8-bit ADC)<br>10: -40° F ... 216° F, with 1 ° F resolution (1 LSB in the 8-bit ADC) |
| 5    | entsoffs     | <b>Temperature Sensor Offset to Convert from K to °C.</b>  |
| 4    | entstrim     | <b>Temperature Sensor Trim Enable.</b>   |
| 3: 0 | tstrim[3:0]  | <b>Temperature Sensor Trim Value.</b>  |

## Register 13h. Temperature Value Offset

| Bit         | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|----|----|----|----|----|----|----|
| <b>Name</b> | tvoffs[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W         |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit  | Name        | Function  |
|------|-------------|---|
| 7: 0 | tvoffs[7:0] | <b>Temperature Value Offset.</b><br>This value is added to the measured temperature value. (MSB, tvoffs[8]: sign bit) |

**Note: If a new configuration is needed (e.g., for the WUT or the LDC), proper functionality is required. The function must first be disabled, then the settings changed, then enabled back on.**

## Register 14h. Wake-Up Timer Period 1

| Bit         | D7       | D6 | D5 | D4       | D3 | D2 | D1 | D0 |
|-------------|----------|----|----|----------|----|----|----|----|
| <b>Name</b> | Reserved |    |    | wtr[4:0] |    |    |    |    |
| <b>Type</b> | R/W      |    |    | R/W      |    |    |    |    |

Reset value = xxx00011

| Bit  | Name     | Function  |
|------|----------|---|
| 7: 5 | Reserved | <b>Reserved.</b>  |
| 4: 0 | wtr[4:0] | <b>Wake Up Timer Exponent (R) Value*.</b><br>Maximum value for R is decimal 20. A value greater than 20 will yield a result as if 20 were written. R Value = 0 can be written here. |

**\*Note:** The period of the wake-up timer can be calculated as  $TWUT = (4 \times M \times 2^R) / 32.768$  ms. R = 0 is allowed, and the maximum value for R is decimal 20. A value greater than 20 will result in the same as if 20 was written.

## Register 15h. Wake-Up Timer Period 2

| Bit         | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------|----|----|----|----|----|----|----|
| <b>Name</b> | wtm[15:8] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W       |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit  | Name      | Function                                  |
|------|-----------|---|
| 7: 0 | wtm[15:8] | <b>Wake Up Timer Mantissa (M) Value*.</b> |

**\*Note:** The period of the wake-up timer can be calculated as  $TWUT = (4 \times M \times 2^R) / 32.768$  ms.

## Register 16h. Wake-Up Timer Period 3

| Bit         | D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----|----|----|----|----|----|----|
| <b>Name</b> | wtm[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W      |    |    |    |    |    |    |    |

Reset value = 00000001

| Bit  | Name     | Function   |
|------|----------|--|
| 7: 0 | wtm[7:0] | <b>Wake Up Timer Mantissa (M) Value*.</b><br>M[7:0] = 0 is not valid here. Write at least decimal 1. |

**\*Note:** The period of the wake-up timer can be calculated as  $TWUT = (4 \times M \times 2^R) / 32.768$  ms.



## Register 17h. Wake-Up Timer Value 1

| Bit         | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------|----|----|----|----|----|----|----|
| <b>Name</b> | wtm[15:8] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W       |    |    |    |    |    |    |    |

Reset value = xxxxxxxx

| Bit   | Name      | Function                                  |
|---|-----------|---|
| 7: 0  | wtm[15:8] | <b>Wake Up Timer Mantissa (M) Value*.</b> |
| *Note: The period of the wake-up timer can be calculated as $TWUT = (4 \times M \times 2^R) / 32.768 \text{ ms.}$ |           |   |

## Register 18h. Wake-Up Timer Value 2

| Bit         | D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----|----|----|----|----|----|----|
| <b>Name</b> | wtm[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W      |    |    |    |    |    |    |    |

Reset value = xxxxxxxx

| Bit   | Name     | Function                                  |
|---|----------|---|
| 7: 0  | wtm[7:0] | <b>Wake Up Timer Mantissa (M) Value*.</b> |
| *Note: The period of the wake-up timer can be calculated as $TWUT = (4 \times M \times 2^R) / 32.768 \text{ ms.}$ |          |   |

## Register 1Ah. Low Battery Detector Threshold

| Bit         | D7       | D6 | D5 | D4       | D3 | D2 | D1 | D0 |
|-------------|----------|----|----|----------|----|----|----|----|
| <b>Name</b> | Reserved |    |    | lbd[4:0] |    |    |    |    |
| <b>Type</b> | R        |    |    | R/w      |    |    |    |    |

Reset value = xxx10100

| Bit  | Name     | Function   |
|------|----------|--|
| 7: 5 | Reserved | <b>Reserved.</b>   |
| 4: 0 | lbd[4:0] | <b>Low Battery Detector Threshold.</b><br>This threshold is compared to Battery Voltage Level. If the Battery Voltage is less than the threshold the Low Battery Interrupt is set. Default = 2.7 V.* |

\*Note: The threshold can be calculated as  $V_{\text{threshold}} = 1.7 + \text{lbd} \times 50 \text{ mV}$ .

## Register 1Bh. Battery Voltage Level

| Bit         | D7       | D6 | D5 | D4        | D3 | D2 | D1 | D0 |
|-------------|----------|----|----|-----------|----|----|----|----|
| <b>Name</b> | Reserved |    |    | vbat[4:0] |    |    |    |    |
| <b>Type</b> | R        |    |    | R         |    |    |    |    |

Reset value = xxxxxxxx

| Bit  | Name      | Function  |
|------|-----------|---|
| 7: 5 | Reserved  | <b>Reserved.</b>  |
| 4: 0 | vbat[4:0] | <b>Battery Voltage Level.</b><br>The battery voltage is converted by a 5 bit ADC. In Sleep Mode the register is updated in every 1 s. In other states it measures continuously. |

## Register 30h. Data Access Control

| Bit         | D7       | D6      | D5       | D4       | D3      | D2    | D1       | D0 |
|-------------|----------|---------|----------|----------|---------|-------|----------|----|
| <b>Name</b> | Reserved | lsbfrst | crcdonly | Reserved | enpactx | encrc | crc[1:0] |    |
| <b>Type</b> | R/w      | R/w     | R/w      | R/w      | R/w     | R/w   | R/w      |    |

Reset value = 10001101

| Bit | Name     | Function  |
|-----|----------|---|
| 7   | Reserved | <b>Reserved.</b>  |
| 6   | lsbfrst  | <b>LSB First Enable.</b><br>The LSB of the data will be transmitted first if this bit is set.   |
| 5   | crcdonly | <b>CRC Data Only Enable.</b><br>When this bit is set to 1 the CRC is calculated on the packet data fields only.   |
| 4   | Reserved | <b>Reserved.</b>  |
| 3   | enpactx  | <b>Enable Packet TX Handling.</b><br>If FIFO Mode (dtmod = 10) is being used automatic packet handling may be enabled. Setting enpactx = 1 will enable automatic packet handling in the TX path. Register 30–4D allow for various configurations of the packet structure. Setting enpactx = 0 will not do any packet handling in the TX path. It will only transmit what is loaded to the FIFO. |
| 2   | encrc    | <b>CRC Enable.</b><br>Cyclic Redundancy Check generation is enabled if this bit is set.   |
| 1:0 | crc[1:0] | <b>CRC Polynomial Selection.</b><br>00: CCITT<br>01: CRC-16 (IBM)<br>10: IEC-16<br>11: Biacheva   |

## Register 31h. EZMAC® Status

| Bit         | D7       | D6 | D5 | D4 | D3 | D2 | D1   | D0      |
|-------------|----------|----|----|----|----|----|------|---------|
| <b>Name</b> | Reserved |    |    |    |    |    | pktx | pkstent |
| <b>Type</b> | R        |    |    |    |    |    | R    | R       |

Reset value = 00000000

| Bit | Name     | Function  |
|-----|----------|---|
| 7:2 | Reserved | <b>Reserved.</b>  |
| 1   | pktx     | <b>Packet Transmitting.</b><br>When pktx = 1 the radio is currently transmitting a packet.  |
| 0   | pkstent  | <b>Packet Sent.</b><br>A pkstent = 1 a packet has been sent by the radio. (Same bit as in register 03, but reading it does not reset the IRQ) |

## Register 33h. Header Control 2

| Bit         | D7       | D6         | D5 | D4 | D3       | D2           | D1 | D0         |
|-------------|----------|------------|----|----|----------|--------------|----|------------|
| <b>Name</b> | Reserved | hdlen[2:0] |    |    | fixpklen | synclen[1:0] |    | prealen[8] |
| <b>Type</b> | R        | R/w        |    |    | R/w      | R/w          |    | R/w        |

Reset value = 00100010

| Bit | Name         | Function  |
|-----|--------------|---|
| 7   | Reserved     | <b>Reserved.</b>  |
| 6:4 | hdlen[2:0]   | <p><b>Header Length.</b><br/>Length of header used if packet handler is enabled for TX (enpactx). Headers are transmitted in descending order.</p> <p>000: No TX header<br/>001: Header 3<br/>010: Header 3 and 2<br/>011: Header 3 and 2 and 1<br/>100: Header 3 and 2 and 1 and 0</p>   |
| 3   | fixpklen     | <p><b>Fix Packet Length.</b><br/>When fixpklen = 1 the packet length (pklen[7:0]) is not included in the header. When fixpklen = 0 the packet length is included in the header.</p>   |
| 2:1 | synclen[1:0] | <p><b>Synchronization Word Length.</b><br/>The value in this register corresponds to the number of bytes used in the Synchronization Word. The synchronization word bytes are transmitted in descending order.</p> <p>00: Synchronization Word 3<br/>01: Synchronization Word 3 and 2<br/>10: Synchronization Word 3 and 2 and 1<br/>11: Synchronization Word 3 and 2 and 1 and 0</p> |
| 0   | prealen[8]   | <p><b>MSB of Preamble Length.</b><br/>See register Preamble Length.</p>   |

## Register 34h. Preamble Length

| Bit         | D7           | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|----|----|----|----|----|----|----|
| <b>Name</b> | prealen[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W          |    |    |    |    |    |    |    |

Reset value = 00001000

| Bit  | Name         | Function   |
|------|--------------|--|
| 7: 0 | prealen[7:0] | <p><b>Preamble Length.</b></p> <p>The value in the prealen[8:0] register corresponds to the number of nibbles (4 bits) in the packet. For example prealen[8:0] = '000001000' corresponds to a preamble length of 32 bits (8 x 4bits) or 4 bytes. The maximum preamble length is prealen[8:0] = 111111111 which corresponds to a 255 bytes Preamble. Writing 0 will have the same result as if writing 1, which corresponds to one single nibble of preamble.</p> |

## Register 36h. Synchronization Word 3

| Bit         | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|----|----|----|----|----|----|----|
| <b>Name</b> | sync[31:24] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W         |    |    |    |    |    |    |    |

Reset value = 00101101

| Bit  | Name        | Function  |
|------|-------------|---|
| 7: 0 | sync[31:24] | <p><b>Synchronization Word 3.</b></p> <p>4<sup>th</sup> byte of the synchronization word.</p> |

## Register 37h. Synchronization Word 2

| Bit         | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|----|----|----|----|----|----|----|
| <b>Name</b> | sync[23:16] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W         |    |    |    |    |    |    |    |

Reset value = 11010100

| Bit  | Name        | Function  |
|------|-------------|---|
| 7: 0 | sync[23:16] | <p><b>Synchronization Word 2.</b></p> <p>3<sup>rd</sup> byte of the synchronization word.</p> |

## Register 38h. Synchronization Word 1

| Bit         | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|----|----|----|----|----|----|----|
| <b>Name</b> | sync[15:8] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W        |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit  | Name       | Function  |
|------|------------|---|
| 7: 0 | sync[15:8] | <b>Synchronization Word 1.</b><br>2 <sup>nd</sup> byte of the synchronization word. |

## Register 39h. Synchronization Word 0

| Bit         | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------|----|----|----|----|----|----|----|
| <b>Name</b> | sync[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W       |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit  | Name      | Function  |
|------|-----------|---|
| 7: 0 | sync[7:0] | <b>Synchronization Word 0.</b><br>1 <sup>st</sup> byte of the synchronization word. |

## Register 3Ah. Transmit Header 3

| Bit         | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|----|----|----|----|----|----|----|
| <b>Name</b> | txhd[31:24] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W         |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit  | Name        | Function   |
|------|-------------|--|
| 7: 0 | txhd[31:24] | <b>Transmit Header 3.</b><br>4 <sup>th</sup> byte of the header to be transmitted. |

## Register 3Bh. Transmit Header 2

| Bit         | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|----|----|----|----|----|----|----|
| <b>Name</b> | txhd[23:16] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W         |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit  | Name        | Function   |
|------|-------------|--|
| 7: 0 | txhd[23:16] | <b>Transmit Header 2.</b><br>3 <sup>rd</sup> byte of the header to be transmitted. |

## Register 3Ch. Transmit Header 1

| Bit         | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|----|----|----|----|----|----|----|
| <b>Name</b> | txhd[15:8] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W        |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit  | Name       | Function   |
|------|------------|--|
| 7: 0 | txhd[15:8] | <b>Transmit Header 1.</b><br>2 <sup>nd</sup> byte of the header to be transmitted. |

## Register 3Ah. Transmit Header 3

| Bit         | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------|----|----|----|----|----|----|----|
| <b>Name</b> | txhd[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W       |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit  | Name      | Function   |
|------|-----------|--|
| 7: 0 | txhd[7:0] | <b>Transmit Header 0.</b><br>1 <sup>st</sup> byte of the header to be transmitted. |



## Register 3Eh. Packet Length

| Bit         | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|----|----|----|----|----|----|----|
| <b>Name</b> | pklen[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W        |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit  | Name       | Function   |
|------|------------|--|
| 7: 0 | pklen[7:0] | <p><b>Packet Length.</b></p> <p>The value in the pklen[7:0] register corresponds directly to the number of bytes in the Packet. For example pklen[7:0] = '00001000' corresponds to a packet length of 8 bytes. The maximum packet length is pklen[7:0] = '11111111', a 255 byte packet. Writing 0 is possible, in this case we do not send any data in the packet.</p> |

**Table 22. Internal Analog Signals Available on the Analog Test Bus**

| atb[3:0] | TESTp        | TESTn        |
|----------|--------------|--------------|
| 0        | NC           | NC           |
| 1        | PLL_Icp_Test | PLL_IBG_5u   |
| 2        | PLL_VBG_Bias | VSS_VCO      |
| 3        | PLL_Vctrl    | PLL_Iptat_5u |
| 4        | VCO_LDO_VBG  | VCO_LDO_VOUT |
| 5        | RF_LDO_VBG   | RF_LDO_VOUT  |
| 6        | PLL_LDO_VBG  | PLL_LDO_VOUT |
| 7        | RCOSC_65kout | RCOSC_VSS    |
| 8        | NC           | NC           |
| 9        | LBD_Comp     | LBD_VBG(TS)  |
| 10       | TS_VBG       | TS_VTemp     |
| 11       | DIG_LDO_VBG  | DIG_LDO_VFB  |
| 12       | PA_Ramp      | NC           |
| 13       | ADC_VIN      | ADC_VDAC     |
| 14       | NC           | NC           |
| 15       | NC           | NC           |

## Register 51h. Digital Test Bus Select

| Bit         | D7       | D6       | D5       | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----|----|----|----|----|
| <b>Name</b> | Reserved | ensctest | dtb[5:0] |    |    |    |    |    |
| <b>Type</b> | R/W      | R/W      | R/W      |    |    |    |    |    |

Reset value = 00000000

| Bit | Name     | Function  |
|-----|----------|---|
| 7   | Reserved | <b>Reserved.</b>  |
| 6   | ensctest | <b>Scan Test Enable.</b><br>When set to 1 then GPIO0 will be the ScanEn input.  |
| 5:0 | dtb[5:0] | <b>Digital Test Bus.</b><br>GPIO must be configured to Digital Test Mux output. |

**Table 23. Internal Digital Signals Available on the Digital Test Bus**

| dtb[4:0] | GPIO0           | Signal                         | GPIO1              | Signal                         | GPIO2           | Signal                        |
|----------|-----------------|--------------------------------|--------------------|--------------------------------|-----------------|-------------------------------|
| 0        | wkup_clk_32k    | wake-up 32kHz clock            | rbase_en           | first divided clock            | clk_base        | timebase clock                |
| 1        | wkup_clk_32k    | wake-up 32kHz clock            | wake_up            | wake-up event                  | tm1sec          | 1 sec timebase                |
| 2        | ts_adc_en       | aux. ADC enable                | adc_rdy_n          | aux. ADC conversion ready      | adc_done        | aux. ADC measurement done     |
| 3        | cont_lbd        | low battery continuous mode    | lbd_on             | low battery ON signal          | lbd             | unfiltered output of LBD      |
| 4        | div_clk_g       | gated divided clock            | uc_clk             | microcontroller clock          | ckout_rcsel     | slow clock selected           |
| 5        | en_div_sync     | clock divider enable (sync'ed) | en_ckout           | clock out enable               | en_ckout_s      | clock out enable (sync'ed)    |
| 6        | osc30_en        | oscillator enable              | osc30_bias2x       | oscillator bias control        | xok             | chip ready                    |
| 7        | xok             | chip ready                     | zero_cap           | cap. load zero                 | osc30_buff_en   | buffer enable                 |
| 8        | tsadc_needed    | aux. ADC enable                | ext_retran         | ext. retransmission request    | tx_mod_gpio     | TX modulation input           |
| 9        | gpio_0_oen_n    | GPIO0 output enable            | gpio_0_aen         | GPIO0 analog selection         | gpio_0_aden     | GPIO0 ADC input line enable   |
| 10       | int_ack1        | interrupt acknowledge 1        | int_ack2           | interrupt acknowledge 2        | int_store       | interrupt latch closed        |
| 11       | ext_int2        | ext. interrupt from GPIO2      | irq_bit8           | combined external status       | msk_bit8        | combined masked ext. int.     |
| 12       | sdo_aux_sel     | SDO aux. function select       | sdo_aux            | SDO aux. signal                | nirq_aux_sel    | nIRQ aux. function select     |
| 13       | trdata_on_sdi   | TX/RX data on SDI              | tx_mod             | TX modulation input            | tx_clk_out      | TX clock output               |
| 14       | start_full_sync | RC osc. full calibration start | start_fine_sync    | RC osc. fine calibration start | xtal_req        | crystal req. for RC osc. cal. |
| 15       | coarse_rdy      | RC osc. coarse cal. ready      | fine_rdy           | RC osc. fine cal. ready        | xtal_req_sync   | sync'ed crystal request       |
| 16       | vco_cal_rst_s_n | VCO calibration reset          | vco_cal            | VCO calibration is running     | vco_cal_done    | VCO calibration done          |
| 17       | vco_cal_en      | VCO calibration enable         | en_ref_cnt         | reference counter enable       | en_freq_cnt_s   | frequency counter enable      |
| 18       | vco_cal_en      | VCO calibration enable         | pos_diff           | positive difference to goal    | en_freq_cnt_s   | frequency counter enable      |
| 19       | dsm_clk_mux     | DSM multiplexed clock          | pll_fb_clk_tst     | PLL feedback clock             | pll_ref_clk_tst | PLL reference clock           |
| 20       | dsm[0]          | delta-sigma output             | dsm[1]             | delta-sigma output             | dsm[2]          | delta-sigma output            |
| 21       | dsm[3]          | delta-sigma output             | pll_fbdiv15        |                                | dsm_rst_s_n     | delta-sigma reset             |
| 22       | pll_en          | PLL enable: TUNE state         | pllt0_ok           | PLL initial settling OK        | pllts_ok        | PLL soft settling OK          |
| 23       | ch_freq_req     | frequency change request       | pllts_ok           | PLL soft settling OK           | vco_cal_done    | VCO calibration done          |
| 24       | vco_cal_en      | VCO calibration enable         | pll_vbias_shunt_en | VCO bias shunt enable          | prog_req        | frequency recalculation req.  |
| 25       | bandgap_en      | bandgap enable                 | frac_div_en        | fractional divider enable      | buff3_en        | buffer3 enable                |
| 26       | pll_pfd_up      | PFD up signal                  | pll_pfd_down       | PFD down signal                | pfd_up_down     | PFD output change (XOR'ed)    |
| 27       | pll_lock_detect | PLL lock detect                | pll_en             | PLL enable: TUNE state         | pllt0_ok        | PLL initial settling OK       |
| 28       | pll_en          | PLL enable: TUNE state         | pll_lock_detect    | PLL lock detect                | pllts_ok        | PLL soft settling OK          |
| 29       | pwst[0]         | internal power state           | pwst[1]            | internal power state           | pwst[2]         | internal power state          |

**Table 23. Internal Digital Signals Available on the Digital Test Bus (Continued)**

| dtb[4:0] | GPIO0          | Signal                       | GPIO1            | Signal                       | GPIO2                   | Signal                       |
|----------|----------------|------------------------------|------------------|------------------------------|-------------------------|------------------------------|
| 30       | xok            | chip ready: READY state      | pll_en           | PLL enable: TUNE state       | tx_en                   | TX enable: TX state          |
| 31       | ts_en          | temperature sensor enable    | auto_tx_on       | automatic TX ON              | tx_off                  | TX OFF                       |
| 32       | ch_freq_req    | frequency change request     | return_tx        | return from TX               | pk_sent                 | packet sent                  |
| 33       | retran_req     | retransmission request       | tx_ffpt_store    | TX FIFO pointer store        | tx_ffpt_restore         | TX FIFO pointer restore      |
| 34       | pa_on_trig     | PA ON trigger                | dly_5us_ok       | 5 us delay expired           | mod_dly_ok              | modulator delay expired      |
| 35       | tx_shdwn       | TX shutdown                  | ramp_start       | modulator ramp down start    | ramp_done               | modulator ramp down ended    |
| 36       | pk_sent_dly    | delayed packet sent          | tx_shdwn_done    | TX shutdown done             | pa_ramp_en              | PA ramp enable               |
| 37       | tx_en          | TX enable: TX state          | ldo_rf_precharge | RF LDO precharge             | pa_ramp_en              | PA ramp enable               |
| 38       | pa_on_trig     | TX enable: TX state          | dp_tx_en         | packet handler (TX) enable   | mod_en                  | modulator enable             |
| 39       | reg_wr_en      | register write enable        | reg_rd_en        | register rread enable        | addr_inc                | register address increment   |
| 40       | dp_tx_en       | packet handler (TX) enable   | data_start       | start of TX data             | pk_sent                 | packet has been sent         |
| 41       | data_start     | start of TX data             | tx_out           | packet handler TX data out   | pk_sent                 | packet has been sent         |
| 42       | ramp_done      | ramp is done                 | data_start       | start of TX data             | pk_tx                   | packet is being transmitted  |
| 43       | tx_ffaf        | TX FIFO almost full          | tx_fifo_wr_en    | TX FIFO write enable         | tx_ffem_tst             | internal TX FIFO empty       |
| 44       | clk_mod        | modulator gated 10MHz clock  | tx_clk           | TX clock from NCO            | rd_clk_x8               | read clock = tx_clk / 10     |
| 45       | mod_en         | modulator enable             | ramp_start       | start modulator ramping down | ramp_done               | modulator ramp done          |
| 46       | data_start     | data input start from PH     | ook_en           | OOK modulation enable        | ook (also internal PN9) | OOK modulation               |
| 47       | prog_req       | freq. channel update request | freq_err         | wrong freq. indication       | dsm_rst_s_n             | dsm sync. reset              |
| 48       | mod_en         | modulator enable             | tx_rdy           | TX ready                     | tx_clk                  | TX clock from NCO            |
| 49       | dp_rx_en       | packet handler (RX) enable   | prea_valid       | valid preamble               | pk_srch                 | packet is being searched     |
| 50       | pk_srch        | packet is being searched     | sync_ok          | sync. word has been detected | rx_data                 | packet handler RX data input |
| 51       | pk_rx          | packet is being received     | sync_ok          | sync. word has been detected | pk_valid                | valid packet received        |
| 52       | sync_ok        | sync. word has been detected | crc_error        | CRC error has been detected  | hdch_error              | header error detected        |
| 53       | direct_mode    | direct mode                  | rx_ffaf          | RX FIFO almost full          | rx_fifo_rd_en           | RX FIFO read enable          |
| 54       | bit_clk        | bit clock                    | prea_valid       | valid preamble               | rx_data                 | demodulator RX data output   |
| 55       | prea_valid     | valid preamble               | prea_inval       | invalid preamble             | ant_div_sw              | antenna switch (algorithm)   |
| 56       | sync_ok        | sync. word has been detected | bit_clk          | bit clock                    | rx_data                 | demodulator RX data output   |
| 57       | demod phase[4] | demodulator phase MSB        | demod phase [3]  | demodulator MSB-1            | demod phase [2]         | demodulator MSB-2            |
| 58       | prea_valid     | valid preamble               | demod_tst[2]     | demodulator test             | demod_tst[1]            | demodulator test             |
| 59       | agc_smp_clk    | AGC sample clock             | win_h_tp         | window comparator high       | win_l_tp                | window comparator low dly'd  |
| 60       | agc_smp_clk    | AGC sample clock             | win_h_dly_tp     | window comparator high       | win_l_dly_tp            | window comparator low dly'd  |
| 61       | ldc_on         | active low duty cycle        | pll_en           | PLL enable: TUNE state       | rx_en                   | RX enable: RX state          |
| 62       | ldc_on         | active low duty cycle        | no_sync_det      | no sync word detected        | prea_valid              | valid preamble               |
| 63       | adc_en         | ADC enable                   | adc_refdac_en    | ADC reference DAC enable     | adc_rst_n               | combined ADC reset           |

## Register 52h. TX Ramp Control

| Bit         | D7       | D6         | D5 | D4 | D3           | D2 | D1          | D0 |
|-------------|----------|------------|----|----|--------------|----|-------------|----|
| <b>Name</b> | Reserved | txmod[2:0] |    |    | ldoramp[1:0] |    | txramp[1:0] |    |
| <b>Type</b> | R/w      | R/w        |    |    | R/w          |    | R/w         |    |

Reset value = 00101111

| Bit | Name         | Function  |
|-----|--------------|---|
| 7   | Reserved     | <b>Reserved.</b>  |
| 6:4 | txmod[2:0]   | <b>TX Modulation Delay.</b><br>The time delay between PA enable and the beginning of the TX modulation to allow for PA ramp-up. It can be set from 0 $\mu$ s to 28 $\mu$ s in 4 $\mu$ s steps. This also works during PA ramp down. |
| 3:2 | ldoramp[1:0] | <b>TX LDO Ramp Time.</b><br>The RF LDO is used to help ramp the PA to prevent VCO pulling and spectral splatter.<br>00: 5 $\mu$ s<br>01: 10 $\mu$ s<br>10: 15 $\mu$ s<br>11: 20 $\mu$ s   |
| 1:0 | txramp[1:0]  | <b>TX Ramp Time.</b><br>The PA is ramped up slowly to prevent VCO pulling and spectral splatter. This register sets the time the PA is ramped up.<br>00: 5 $\mu$ s<br>01: 10 $\mu$ s<br>10: 15 $\mu$ s<br>11: 20 $\mu$ s            |



The total settling time (cold start) of the PLL after the calibration can be calculated as  $T_{cs} = T_s + T_o$ .

## Register 53h. PLL Tune Time

| Bit         | D7         | D6 | D5 | D4 | D3 | D2     | D1 | D0 |
|-------------|------------|----|----|----|----|--------|----|----|
| <b>Name</b> | pllts[4:0] |    |    |    |    | pllts0 |    |    |
| <b>Type</b> | R/w        |    |    |    |    | R/w    |    |    |

Reset value = 01010010

| Bit | Name       | Function  |
|-----|------------|---|
| 7:3 | pllts[4:0] | <b>PLL Soft Settling Time (Ts).</b><br>This register will set the settling time for the PLL from a previous locked frequency in Tune mode. The value is configurable between 0 $\mu$ s and 310 $\mu$ s, in 10 $\mu$ s intervals. The default plltime corresponds to 100 $\mu$ s. See formula above. |
| 2:0 | pllts0t    | <b>PLL Settling Time (To).</b><br>This register will set the time allowed for PLL settling after the calibrations are completed. The value is configurable between 0 $\mu$ s and 70 $\mu$ s, in 10 $\mu$ s steps. The default pllto corresponds to 20 $\mu$ s. See formula above.                   |

## Register 54h. PA Boost

| Bit         | D7            | D6 | D5         | D4 | D3 | D2           | D1             | D0 |
|-------------|---------------|----|------------|----|----|--------------|----------------|----|
| <b>Name</b> | Reserved[7:6] |    | inv_pre_th |    |    | ldo_pa_boost | pa_vbias_boost |    |
| <b>Type</b> | R/w           |    | R/w        |    |    | R/w          | R/w            |    |

Reset value = 01010100

| Bit | Name            | Function                           |
|-----|-----------------|------------------------------------|
| 7:6 | Reserved[7:6]   | <b>Reserved.</b>                   |
| 5:2 | inv_pre_th[5:2] | <b>Invalid Preamble Threshold.</b> |
| 1   | ldo_pa_boost    | <b>LDO PA Boost.</b>               |
| 0   | pa_vbias_boost  | <b>PA VBIAS Boost.</b>             |

Invalid preamble will be evaluated during this period:  $(\text{invalid\_preamble\_Threshold} \times 4) \times \text{Bit Rate period}$ .

## Register 55h. Calibration Control

| Bit         | D7       | D6           | D5       | D4       | D3    | D2       | D1     | D0      |
|-------------|----------|--------------|----------|----------|-------|----------|--------|---------|
| <b>Name</b> | Reserved | xtalstarhalf | Reserved | enrcfcal | rccal | vcocaldp | vcocal | skipvco |
| <b>Type</b> | R        | R/w          | R        | R/w      | R/w   | R/w      | R/w    | R/w     |

Reset value = x1x00100

| Bit | Name         | Function  |
|-----|--------------|---|
| 7   | Reserved     | <b>Reserved.</b>  |
| 6   | xtalstarhalf | <b>If Set, the Xtal Wake Time Period is Halved.</b>   |
| 5   | Reserved     | <b>Reserved.</b>  |
| 4   | enrcfcal     | <b>RC Oscillator Fine Calibration Enable.</b><br>If this bit is set to 1 then the RC oscillator performs fine calibration in every app. 30 s.   |
| 3   | rccal        | <b>RC Calibration Force.</b><br>If setting rccal = 1 will automatically perform a forced calibration of the 32 kHz RC Oscillator. The RC OSC will automatically be calibrated if the Wake-Up-Timer is enabled. The calibration takes 2 ms. The 32 kHz RC oscillator must be enabled to perform a calibration. Setting this signal from a 0 to 1 will initiate the calibration. This bit is cleared automatically. |
| 2   | vcocaldp     | <b>VCO Calibration Double Precision Enable.</b><br>When this bit is set to 1 then the VCO calibration measures longer thus calibrates more precisely.   |
| 1   | vcocal       | <b>VCO Calibration Force.</b><br>If in Idle Mode and plon = 1, setting vcocal = 1 will force a one time calibration of the synthesizer VCO. This bit is cleared automatically.  |
| 0   | skipvco      | <b>Skip VCO Calibration.</b><br>Setting skipvco = 1 will skip the VCO calibration when going from the Idle state to the TX state.   |

## Register 56h. Modem Test

| Bit         | D7      | D6       | D5     | D4       | D3    | D2         | D1        | D0      |
|-------------|---------|----------|--------|----------|-------|------------|-----------|---------|
| <b>Name</b> | bcrfbyp | slicfbyp | dttype | oscdeten | ookth | refclkssel | refclkinv | distogg |
| <b>Type</b> | R/w     | R/w      | R/w    | R/w      | R/w   | R/w        | R/w       | R/w     |

Reset value = 00000000

| Bit | Name       | Function  |
|-----|------------|---|
| 7   | bcrfbyp    | <b>If set, BCR phase compensation will be bypassed.</b>   |
| 6   | slicfbyp   | <b>If set, slicer phase compensation will be bypassed.</b>  |
| 5   | dttype     | <b>Dithering Type.</b><br>If low and dither enabled, we add +1/0, otherwise if high and dithering enabled, we add $\pm 1$ .                                       |
| 4   | oscdeten   | If low, the ADC Oscillation Detection mechanism is allowed to work. If set, we disable the function.  |
| 3   | ookth      | If set, in OOK mode, the slicer threshold will be estimated by 8 bits of preamble. By default, this bit is low and the demod estimate the threshold after 4 bits. |
| 2   | refclkssel | <b>Delta-Sigma Reference Clock Source Selection</b><br>1: 10 MHz<br>0: PLL  |
| 1   | refclkinv  | <b>Delta-Sigma Reference Clock Inversion Enable.</b>  |
| 0   | distogg    | If reset, the discriminator toggling is disabled.   |

## Register 57h. Charge Pump Test

| Bit         | D7     | D6        | D5        | D4        | D3     | D2          | D1 | D0 |
|-------------|--------|-----------|-----------|-----------|--------|-------------|----|----|
| <b>Name</b> | pfdrst | fbdiv_rst | cpforceup | cpforcedn | cdonly | cdcurr[2:0] |    |    |
| <b>Type</b> | R/w    | R/w       | R/w       | R/w       | R/w    | R/w         |    |    |

Reset value = 00000000

| Bit | Name        | Function                                 |
|-----|-------------|--|
| 7   | pfdrst      | <b>Direct Control to Analog.</b>         |
| 6   | fbdiv_rst   | <b>Direct Control to Analog.</b>         |
| 5   | cpforceup   | <b>Charge Pump Force Up.</b>             |
| 4   | cpforcedn   | <b>Charge Pump Force Down.</b>           |
| 3   | cdonly      | <b>Charge Pump DC Offset Only.</b>       |
| 2:0 | cdcurr[2:0] | <b>Charge Pump DC Current Selection.</b> |

## Register 58h. Charge Pump Current Trimming/Override

| Bit         | D7          | D6 | D5       | D4         | D3 | D2 | D1 | D0 |
|-------------|-------------|----|----------|------------|----|----|----|----|
| <b>Name</b> | cpcurr[1:0] |    | cpcorrov | cporr[4:0] |    |    |    |    |
| <b>Type</b> | R/w         |    | R/w      | R/w        |    |    |    |    |

Reset value = 100xxxxx

| Bit | Name        | Function   |
|-----|-------------|--|
| 7:6 | cpcurr[1:0] | <b>Charge Pump Current (Gain Setting).</b><br>Changing these bits will change the BW of the PLL. The default setting is adequate for all data rates.   |
| 5   | cpcorrov    | <b>Charge Pump Correction Override Enable.</b>   |
| 4:0 | cporr[4:0]  | <b>Charge Pump Correction Value.</b><br>During read, you read what the Charge Pump sees. If cpcorrov = 1, then the value you write will go to the Charge Pump, and will also be the value you read. By default, cpcorr[4:0] wakes up as all Zeros. |

## Register 59h. Divider Current Trimming/Delta-Sigma Test

| Bit         | D7           | D6      | D5          | D4 | D3          | D2 | D1            | D0 |
|-------------|--------------|---------|-------------|----|-------------|----|---------------|----|
| <b>Name</b> | txcorboosten | fbdivhc | d3trim[1:0] |    | d2trim[1:0] |    | d1p5trim[1:0] |    |
| <b>Type</b> | R/w          | R/w     | R/w         |    | R/w         |    | R/w           |    |

Reset value = 10000000

| Bit | Name          | Function  |
|-----|---------------|---|
| 7   | txcorboosten  | <b>If this is Set, then vcocorr (reg 5A[5:2]) = 1111 during TX Mode and VCO CAL followed by TX.</b> |
| 6   | fbdivhc       | <b>Feedback (fractional) Divider High Current Enable (+5 <math>\mu</math>A).</b>                    |
| 5:4 | d3trim[1:0]   | <b>Divider 3 Current Trim Value.</b>  |
| 3:2 | d2trim[1:0]   | <b>Divider 2 Current Trim Value.</b>  |
| 1:0 | d1p5trim[1:0] | <b>Divider 1.5 (div-by-1.5) Current Trim Value.</b>   |



## Register 5Ah. VCO Current Trimming

| Bit         | D7           | D6        | D5           | D4 | D3 | D2          | D1 | D0 |
|-------------|--------------|-----------|--------------|----|----|-------------|----|----|
| <b>Name</b> | txcurboosten | vcocorrov | vcocorr[3:0] |    |    | vcocur[1:0] |    |    |
| <b>Type</b> | R/w          | R/w       | R/w          |    |    | R/w         |    |    |

Reset value = 00000011

| Bit | Name         | Function   |
|-----|--------------|--|
| 7.  | txcurboosten | <b>If this is Set, then vcocur = 11 during TX Mode and VCO CAL followed by TX.</b> |
| 6   | vcocorrov    | <b>VCO Current Correction Override.</b>  |
| 5:2 | vcocorr[3:0] | <b>VCO Current Correction Value.</b>   |
| 1:0 | vcocur[1:0]  | <b>VCO Current Trim Value.</b>   |

## Register 5Bh. VCO Calibration/Override

| Bit         | D7              | D6          | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------------|-------------|----|----|----|----|----|----|
| <b>Name</b> | vcocalov/vcdone | vcocal[6:0] |    |    |    |    |    |    |
| <b>Type</b> | R/w             | R/w         |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name            | Function   |
|-----|-----------------|--|
| 7.  | vcocalov/vcdone | <b>VCO Calibration Override/Done.</b><br>When vcocalov = 0 the internal VCO calibration results may be viewed by reading the vcocal register. When vcocalov = 1 the VCO results may be overridden externally through the SPI by writing to the vcocal register. Reading this bit gives 1 if the calibration process has been finished. |
| 6:0 | vcocal[6:0]     | <b>VCO Calibration Results.</b>  |

## Register 5Ch. Synthesizer Test

| Bit         | D7    | D6      | D5      | D4    | D3           | D2 | D1        | D0    |
|-------------|-------|---------|---------|-------|--------------|----|-----------|-------|
| <b>Name</b> | dsmdt | vcotype | enoloop | dsmod | dsorder[1:0] |    | dsrstmode | dsrst |
| <b>Type</b> | R/w   | R       | R/w     | R/w   | R/w          |    | R/w       | R/w   |

Reset value = 0x001110

| Bit | Name         | Function   |
|-----|--------------|--|
| 7   | dsmdt        | <b>Enable DSM Dithering.</b><br>If low, dithering is disabled.   |
| 6   | vcotype      | <b>VCO Type.</b><br>0: basic, constant K<br>1: single varactor, changing K   |
| 5   | enoloop      | <b>Open Loop Mode Enable.</b>  |
| 4   | dsmod        | <b>Delta-Sigma Modulus.</b><br>0: 64 000<br>1: 65 536  |
| 3:2 | dsorder[1:0] | <b>Delta-Sigma Order.</b><br>00: 0 order<br>01: 1 <sup>st</sup> order<br>10: 2 <sup>nd</sup> order<br>11: Mash 111 |
| 1   | dsrstmode    | <b>Delta-Sigma Reset Mode.</b>   |
| 0   | dsrst        | <b>Delta-Sigma Reset.</b>  |

## Register 5Dh. Block Enable Override 1

| Bit         | D7    | D6    | D5    | D4   | D3    | D2     | D1     | D0    |
|-------------|-------|-------|-------|------|-------|--------|--------|-------|
| <b>Name</b> | enmix | enina | enpga | enpa | enbf5 | endv32 | enbf12 | enmx2 |
| <b>Type</b> | R/W   | R/W   | R/W   | R/W  | R/W   | R/W    | R/W    | R/W   |

Reset value = 00000000

| Bit | Name   | Function                                |
|-----|--------|---|
| 7   | enmix  | <b>Mixer Enable Override.</b>           |
| 6   | enina  | <b>LNA Enable Override.</b>             |
| 5   | enpga  | <b>PGA Enable Override.</b>             |
| 4   | enpa   | <b>Power Amplifier Enable Override.</b> |
| 3   | enbf5  | <b>Buffer 5 Enable Override.</b>        |
| 2   | endv32 | <b>Divider 3_2 Enable Override.</b>     |
| 1   | enbf12 | <b>Buffer 1_2 Enable Override.</b>      |
| 0   | enmx2  | <b>Multiplexer 2 Enable Override.</b>   |

## Register 5Eh. Block Enable Override 2

| Bit         | D7   | D6     | D5    | D4    | D3    | D2     | D1    | D0       |
|-------------|------|--------|-------|-------|-------|--------|-------|----------|
| <b>Name</b> | ends | enldet | enmx3 | enbf4 | enbf3 | enbf11 | enbf2 | pllreset |
| <b>Type</b> | R/W  | R/W    | R/W   | R/W   | R/W   | R/W    | R/W   | R/W      |

Reset value = 01000000

| Bit | Name     | Function  |
|-----|----------|---|
| 7   | ends     | <b>Delta-Sigma Enable Override.</b>                                     |
| 6   | enldet   | <b>Lock Detect Enable.</b><br>(direct control, does not need override!) |
| 5   | enmx3    | <b>Multiplexer 3 Enable Override.</b>                                   |
| 4   | enbf4    | <b>Buffer 4 Enable Override.</b>  |
| 3   | enbf3    | <b>Buffer 3 Enable Override.</b>  |
| 2   | enbf11   | <b>Buffer 1_1 Enable Override.</b>                                      |
| 1   | enbf2    | <b>Buffer 2 Enable Override.</b>  |
| 0   | pllreset | <b>PLL Reset Enable Override.</b>                                       |

## Register 5Fh. Block Enable Override 3

| Bit         | D7     | D6     | D5    | D4      | D3       | D2    | D1   | D0   |
|-------------|--------|--------|-------|---------|----------|-------|------|------|
| <b>Name</b> | enfrdv | endv31 | endv2 | endv1p5 | dvbshunt | envco | encp | enbg |
| <b>Type</b> | R/W    | R/W    | R/W   | R/W     | R/W      | R/W   | R/W  | R/W  |

Reset value = 00000000

| Bit | Name     | Function   |
|-----|----------|--|
| 7   | enfrdv   | <b>Fractional Divider Enable Override.</b>       |
| 6   | endv31   | <b>Divider 3_1 Enable Override.</b>              |
| 5   | endv2    | <b>Divider 2 Enable Override.</b>                |
| 4   | endv1p5  | <b>Divider 1.5 (div-by-1.5) Enable Override.</b> |
| 3   | dvbshunt | <b>VCO Bias Shunt Enable Override Mode.</b>      |
| 2   | envco    | <b>VCO Enable Override.</b>                      |
| 1   | encp     | <b>Charge Pump Enable Override.</b>              |
| 0   | enbg     | <b>Bandgap Enable Override.</b>                  |

## Register 62h. Crystal Oscillator/Power-on-Reset Control

| Bit         | D7        | D6 | D5 | D4      | D3       | D2      | D1     | D0    |
|-------------|-----------|----|----|---------|----------|---------|--------|-------|
| <b>Name</b> | pwst[2:0] |    |    | clkhyst | enbias2x | enamp2x | bufovr | enbuf |
| <b>Type</b> | R         |    |    | R/W     | R/W      | R/W     | R/W    | R/W   |

Reset value = xxx00100

| Bit | Name      | Function  |
|-----|-----------|---|
| 7:5 | pwst[2:0] | <b>Internal Power States of the Module.</b><br>LP: 000<br>RDY: 001<br>Tune: 011<br>TX: 010  |
| 4   | clkhyst   | <b>Clock Hysteresis Setting.</b>  |
| 3   | enbias2x  | <b>2 Times Higher Bias Current Enable.</b>  |
| 2   | enamp2x   | <b>2 Times Higher Amplification Enable.</b>   |
| 1   | bufovr    | <b>Output Buffer Enable Override.</b><br>If set to 1 then the enbuf bit controls the output buffer.<br>0: output buffer is controlled by the state machine.<br>1: output buffer is controlled by the enbuf bit. |
| 0   | enbuf     | <b>Output Buffer Enable.</b><br>This bit is active only if the bufovr bit is set to 1.  |

## Register 63h. RC Oscillator Coarse Calibration/Override

| Bit         | D7    | D6       | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------|----------|----|----|----|----|----|----|
| <b>Name</b> | rccov | rcc[6:0] |    |    |    |    |    |    |
| <b>Type</b> | R/W   | R/W      |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name     | Function  |
|-----|----------|---|
| 7   | rccov    | <b>RC Oscillator Coarse Calibration Override.</b><br>When rccov = 0 the internal Coarse Calibration results may be viewed by reading the rcccal register. When rccov = 1 the Coarse results may be overridden externally through the SPI by writing to the rcccal register. |
| 6:0 | rcc[6:0] | <b>RC Oscillator Coarse Calibration Override Value/Results.</b>   |

## Register 64h. RC Oscillator Fine Calibration/Override

| Bit         | D7    | D6       | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------|----------|----|----|----|----|----|----|
| <b>Name</b> | rcfov | rcf[6:0] |    |    |    |    |    |    |
| <b>Type</b> | R/W   | R/W      |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name     | Function  |
|-----|----------|---|
| 7   | rcfov    | <b>RC Oscillator Fine Calibration Override.</b><br>When rcfov = 0 the internal Fine Calibration results may be viewed by reading the rcfcacal register. When rcfov = 1 the Fine results may be overridden externally through the SPI by writing to the rcfcacal register. |
| 6:0 | rcf[6:0] | <b>RC Oscillator Fine Calibration Override Value/Results.</b>   |

## Register 65h. LDO Control Override

| Bit         | D7     | D6     | D5       | D4      | D3      | D2      | D1       | D0       |
|-------------|--------|--------|----------|---------|---------|---------|----------|----------|
| <b>Name</b> | enspor | enbias | envcoldo | enifldo | enrfldo | enplldo | endigldo | endigpwn |
| <b>Type</b> | R/W    | R/W    | R/W      | R/W     | R/W     | R/W     | R/W      | R/W      |

Reset value = 10000001

| Bit | Name     | Function   |
|-----|----------|--|
| 7   | enspor   | <b>Smart POR Enable.</b>                                   |
| 6   | enbias   | <b>Bias Enable.</b>  |
| 5   | envcoldo | <b>VCO LDO Enable.</b>                                     |
| 4   | enifldo  | <b>IF LDO Enable.</b>                                      |
| 3   | enrfldo  | <b>RF LDO Enable.</b>                                      |
| 2   | enplldo  | <b>PLL LDO Enable.</b>                                     |
| 1   | endigldo | <b>Digital LDO Enable.</b>                                 |
| 0   | endigpwn | <b>Digital Power Domain Powerdown Enable in Idle Mode.</b> |

## Register 66h. LDO Level Settings

| Bit         | D7    | D6     | D5   | D4     | D3       | D2     | D1 | D0 |
|-------------|-------|--------|------|--------|----------|--------|----|----|
| <b>Name</b> | enovr | enxtal | ents | enrc32 | Reserved | diglvl |    |    |
| <b>Type</b> | R/W   | R/W    | R/W  | R/W    | R        | R/W    |    |    |

Reset value = 00000011

| Bit | Name     | Function  |
|-----|----------|---|
| 7   | enovr    | <b>Enable Overrides.</b><br>If high, ovr values are output to the blocks and can enable or disable them, if low, some ovr value can only enable the blocks. |
| 6   | enxtal   | <b>Xtal Override Enable Value.</b>  |
| 5   | ents     | <b>Temperature Sensor Enable.</b>   |
| 4   | enrc32   | <b>32K Oscillator Enable.</b>   |
| 3   | Reserved | <b>Reserved.</b>  |
| 2:0 | diglvl   | <b>Digital LDO Level Setting.</b>   |

## Register 6Bh. GFSK FIR Filter Coefficient Address

| Bit         | D7       | D6 | D5 | D4 | D3 | D2          | D1 | D0 |
|-------------|----------|----|----|----|----|-------------|----|----|
| <b>Name</b> | Reserved |    |    |    |    | firadd[2:0] |    |    |
| <b>Type</b> | R        |    |    |    |    | R/W         |    |    |

Reset value = xxxxx000

| Bit | Name        | Function   |
|-----|-------------|--|
| 7:3 | Reserved    | <b>Reserved.</b>   |
| 2:0 | firadd[2:0] | <p><b>GFSK FIR Filter Coefficient Look-up Table Address.</b><br/>           The address for Gaussian filter coefficients used in the TX path. The default GFSK setting is for BT = 0.5. It is not needed to change or load the GFSK Coefficients if BT = 0.5 is satisfactory for the system.</p> <p>000: i_coe0 (Default = d1)<br/>           001: i_coe1 (Default = d3)<br/>           010: i_coe2 (Default = d6)<br/>           011: i_coe3 (Default = d10)<br/>           100: i_coe4 (Default = d15)<br/>           101: i_coe5 (Default = d19)<br/>           110: i_coe6 (Default = d20)</p> |

## Register 6Ch. GFSK FIR Filter Coefficient Value

| Bit         | D7       | D6 | D5          | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----|-------------|----|----|----|----|----|
| <b>Name</b> | Reserved |    | firval[5:0] |    |    |    |    |    |
| <b>Type</b> | R/W      |    | R/W         |    |    |    |    |    |

Reset value = xxxxx000

| Bit | Name        | Function  |
|-----|-------------|---|
| 7:6 | Reserved    | <b>Reserved.</b>  |
| 5:0 | firval[5:0] | <p><b>FIR Coefficient Value in the ILook-up Table Addressed by the firadd[2:0].</b><br/>           The default coefficient can be read or modified.</p> |



## Register 6Dh. TX Power

| Bit         | D7       | D6 | D5 | D4 | D3     | D2         | D1  | D0 |
|-------------|----------|----|----|----|--------|------------|-----|----|
| <b>Name</b> | Reserved |    |    |    | lna_sw | txpow[2:0] |     |    |
| <b>Type</b> | R        |    |    |    | R/W    |            | R/W |    |

Reset value = xxxx1000

| Bit | Name       | Function   |
|-----|------------|--|
| 7:4 | Reserved   | <b>Reserved.</b>   |
| 3   | lna_sw     | <b>LNA Switch Controller.</b><br>If set, lna_sw control from the digital will go high during TX modes, and low during other times. If reset, the digital control signal is low at all times. |
| 2:0 | txpow[2:0] | <b>TX Output Power.</b><br>The output power is configurable in ~3 dBm steps.   |

## Register 6Eh. TX Data Rate 1

| Bit         | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|----|----|----|----|----|----|----|
| <b>Name</b> | txdr[15:8] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W        |    |    |    |    |    |    |    |

Reset value = 00001010

| Bit | Name       | Function   |
|-----|------------|--|
| 7:0 | txdr[15:8] | <b>Data Rate Upper Byte.</b><br>See formula above. |

The data rate can be calculated as:  $TX\_DR = 10^3 \times txdr[15:0] / 2^{16}$  [kbps] (if address 70[5] = 0) **or**

The data rate can be calculated as:  $TX\_DR = 10^3 \times txdr[15:0] / 2^{21}$  [kbps] (if address 70[5] = 1)

## Register 6Fh. TX Data Rate 0

| Bit         | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------|----|----|----|----|----|----|----|
| <b>Name</b> | txdr[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W       |    |    |    |    |    |    |    |

Reset value = 00111101

| Bit | Name      | Function   |
|-----|-----------|--|
| 7:0 | txdr[7:0] | <b>Data Rate Lower Byte.</b><br>See formula above. Defaults = 40 kbps. |

## Register 70h. Modulation Mode Control 1

| Bit         | D7       | D6 | D5          | D4       | D3      | D2       | D1      | D0      |
|-------------|----------|----|-------------|----------|---------|----------|---------|---------|
| <b>Name</b> | Reserved |    | txdtrtscale | enphpwdn | manppol | enmaninv | enmanch | enwhite |
| <b>Type</b> | R        |    | R/W         | R/W      | R/W     | R/W      | R/W     | R/W     |

Reset value = 00001100

| Bit | Name        | Function  |
|-----|-------------|---|
| 7:6 | Reserved    | <b>Reserved.</b>  |
| 5   | txdtrtscale | <b>This bit should be set for Data Rates below 30 kbps.</b>   |
| 4   | enphpwdn    | <b>If set, the Packet Handler will be powered down when module is in low power mode.</b>  |
| 3   | manppol     | <b>Manchester Preamble Polarity (will transmit a series of 1 if set, or series of 0 if reset).</b><br>This bit affects ONLY the transmitter side, not the receiver. This is valid ONLY if Manchester Mode is enabled. |
| 2   | enmaninv    | <b>Manchester Data Inversion is Enabled if this bit is set.</b>   |
| 1   | enmanch     | <b>Manchester Coding is Enabled if this bit is set.</b>   |
| 0   | enwhite     | <b>Data Whitening is Enabled if this bit is set.</b>  |

## Register 71h. Modulation Mode Control 2

| Bit         | D7         | D6 | D5         | D4 | D3    | D2    | D1          | D0 |
|-------------|------------|----|------------|----|-------|-------|-------------|----|
| <b>Name</b> | trclk[1:0] |    | dtmod[1:0] |    | eninv | fd[8] | modtyp[1:0] |    |
| <b>Type</b> | R/W        |    | R/W        |    | R/W   | R/W   | R/W         |    |

Reset value = 00000000

| Bit  | Name        | Function  |
|------|-------------|---|
| 7:6  | trclk[1:0]  | <b>TX Data Clock Configuration.</b><br>00: No TX Data CLK is available (asynchronous mode – Can only work with modulations FSK or OOK).<br>01: TX Data CLK is available via the GPIO (one of the GPIO's should be programmed as well).<br>10: TX Data CLK is available via the SDO pin.<br>11: TX Data CLK is available via the nIRQ pin. |
| 5:4  | dtmod[1:0]  | <b>Modulation Source.</b><br>00: Direct Mode using TX_Data function via the GPIO pin (one of the GPIO's should be programmed accordingly as well)<br>01: Direct Mode using TX_Data function via the SDI pin (only when nSEL is high)<br>10: FIFO Mode<br>11: PN9 (internally generated)   |
| 3    | eninv       | <b>TX Data.</b>   |
| 2    | fd[8]       | <b>MSB of Frequency Deviation Setting, see "Register 72h. Frequency Deviation".</b>   |
| 1: 0 | modtyp[1:0] | <b>Modulation Type.</b><br>00: Unmodulated carrier<br>01: OOK<br>10: FSK<br>11: GFSK (enable TX Data CLK (trclk[1:0]) when direct mode is used)   |

The frequency deviation can be calculated:  $Fd = 625 \text{ Hz} \times fd[8:0]$ .

## Register 72h. Frequency Deviation

| Bit         | D7      | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|---------|----|----|----|----|----|----|----|
| <b>Name</b> | fd[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W     |    |    |    |    |    |    |    |

Reset value = 00100000

| Bit | Name    | Function  |
|-----|---------|---|
| 7:0 | fd[7:0] | <b>Frequency Deviation Setting.</b><br>See formula above. |

**Note:** It's recommended to use modulation index of 1 or higher (maximum allowable modulation index is 32). The modulation index is defined by  $2F_D/R_B$  where  $F_D$  is the deviation and  $R_B$  is the data rate. When Manchester coding is enabled the modulation index is defined by  $F_D/R_B$ .

## Register 73h. Frequency Offset 1

| Bit         | D7      | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|---------|----|----|----|----|----|----|----|
| <b>Name</b> | fo[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W     |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name    | Function   |
|-----|---------|--|
| 7:0 | fo[7:0] | <b>Frequency Offset Setting.</b><br>The frequency offset can be calculated as $\text{Offset} = 156.25 \text{ Hz} \times (\text{hbsel} + 1) \times \text{fo}[7:0]$ .<br>fo[9:0] is a twos complement value. |

## Register 74h. Frequency Offset 2

| Bit         | D7       | D6 | D5 | D4 | D3 | D2 | D1      | D0 |
|-------------|----------|----|----|----|----|----|---------|----|
| <b>Name</b> | Reserved |    |    |    |    |    | fo[9:8] |    |
| <b>Type</b> | R        |    |    |    |    |    | R/W     |    |

Reset value = 00000000

| Bit | Name     | Function  |
|-----|----------|---|
| 7:2 | Reserved | <b>Reserved.</b>  |
| 1:0 | fo[9:8]  | <b>Upper Bits of the Frequency Offset Setting.</b><br>fo[9] is the sign bit. The frequency offset can be calculated as Offset = 156.25 Hz x (hbssel + 1) x fo[7:0]. fo[9:0] is a twos complement value. |

## Register 75h. Frequency Band Select

| Bit         | D7       | D6    | D5     | D4      | D3 | D2 | D1 | D0 |
|-------------|----------|-------|--------|---------|----|----|----|----|
| <b>Name</b> | Reserved | sbsel | hbssel | fb[4:0] |    |    |    |    |
| <b>Type</b> | R        | R/W   | R/W    | R/W     |    |    |    |    |

Reset value = 01110101

| Bit | Name     | Function  |
|-----|----------|---|
| 7   | Reserved | <b>Reserved.</b>  |
| 6   | sbse     | <b>Side Band Select.</b>  |
| 5   | hbssel   | <b>High Band Select.</b><br>Setting hbssel = 1 will choose the frequency range from 480–930 MHz (high bands). Setting hbssel = 0 will choose the frequency range from 240–479.9 MHz (low bands).  |
| 4:0 | fb[4:0]  | <b>Frequency Band Select.</b><br>Every increment corresponds to a 10 MHz Band for the Low Bands and a 20 MHz Band for the High Bands. Setting fb[4:0] = 00000 corresponds to the 240–250 MHz Band for hbssel = 0 and the 480–500 MHz Band for hbssel = 1. Setting fb[4:0] = 00001 corresponds to the 250–260 MHz Band for hbssel = 0 and the 500–520 MHz Band for hbssel = 1. |

The RF carrier frequency can be calculated as follows:

$$f_{\text{carrier}} = (f_b + 24 + (f_c + f_o) / 64000) \times 10000 \times (\text{hb\_ssel} + 1) + (f_{\text{hch}} \times f_{\text{hs}} \times 10) \text{ [kHz]},$$

where parameters  $f_c$ ,  $f_o$ ,  $f_b$  and  $\text{hb\_sel}$  come from registers 73h–77h. Parameters  $f_{\text{hch}}$  and  $f_{\text{hs}}$  come from register 79h and 7Ah.

## Register 76h. Nominal Carrier Frequency

| Bit         | D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----|----|----|----|----|----|----|
| <b>Name</b> | fc[15:8] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W      |    |    |    |    |    |    |    |

Reset value = 10111011

| Bit | Name     | Function  |
|-----|----------|---|
| 7:0 | fc[15:8] | <b>Nominal Carrier Frequency Setting.</b><br>See formula above. |

## Register 77h. Nominal Carrier Frequency

| Bit         | D7      | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|---------|----|----|----|----|----|----|----|
| <b>Name</b> | fc[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W     |    |    |    |    |    |    |    |

Reset value = 10000000

| Bit | Name    | Function  |
|-----|---------|---|
| 7:0 | fc[7:0] | <b>Nominal Carrier Frequency Setting.</b><br>See formula above. |

## Register 78h. Miscellaneous Settings

| Bit         | D7            | D6 | D5 | D4 | D3         | D2             | D1 | D0 |
|-------------|---------------|----|----|----|------------|----------------|----|----|
| <b>Name</b> | Reserved[7:4] |    |    |    | Alt_PA_Seq | rcosc_cal[2:0] |    |    |
| <b>Type</b> | R/W           |    |    |    | R/W        | R/W            |    |    |

Reset value = 01111000

| Bit | Name           | Function   |
|-----|----------------|--|
| 7:0 | Reserved[7:4]  | <b>Reserved.</b>   |
| 3   | Alt_PA_Seq     | <b>Alternative PA sequencing.</b><br>If set, we will enable the alternative PA sequence. By default, this is not enabled.  |
| 2:0 | rcosc_cal[2:0] | <b>rcosc_cal[2:0].</b><br>Fine changes on the RC OSC Calibration target frequency, to help compensate for "calibration biases." <b>This register should not be changed by costumers.</b> |

## Register 79h. Frequency Hopping Channel Select

| Bit         | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------|----|----|----|----|----|----|----|
| <b>Name</b> | fhch[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W       |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name      | Function                                 |
|-----|-----------|--|
| 7:0 | fhch[7:0] | <b>Frequency Hopping Channel Number.</b> |

## Register 7Ah. Frequency Hopping Step Size

| Bit         | D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----|----|----|----|----|----|----|
| <b>Name</b> | fhs[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W      |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name     | Function  |
|-----|----------|---|
| 7:0 | fhs[7:0] | <b>Frequency Hopping Step Size in 10 kHz Increments.</b><br>See formula for the nominal carrier frequency at "Register 76h. Nominal Carrier Frequency". |



## Register 7Bh. Turn Around and 15.4 Length Compliance

| Bit         | D7          | D6            | D5 | D4 | D3 | D2             | D1         | D0 |
|-------------|-------------|---------------|----|----|----|----------------|------------|----|
| <b>Name</b> | 15.4 Length | Reserved[6:3] |    |    |    | turn_around_en | phase[1:0] |    |
| <b>Type</b> | R/W         | R/W           |    |    |    | R/W            | R/W        |    |

Reset value = 01111011

| Bit | Name           | Function  |
|-----|----------------|---|
| 7   | 15.4 Length    | <b>15.4 Packet Length Compliance.</b><br>If set, then PK Length definition for both TX and RX will also include the CRC bytes, If reset, then the Length refers ONLY to the DATA payload. For example, writing “9” to this register when it is set, means we are sending/expecting “7” bytes of DATA, and the other “2” should be the CRC (CRC should be enabled separately). |
| 6:3 | Reserved[6:3]  | <b>Reserved.</b>  |
| 2   | turn_around_en | <b>Turn Around Enable.</b><br>Enabling for the turn around functionality.   |
| 1:0 | phase[1:0]     | <b>Turn Around Phase.</b><br>The RX to TX and vice-versa change in frequency will happen (if bit [2] is set) at the last byte, and these two registers set the bit position in which the frequency shifts should occur. Make sure it does not happen too early otherwise the last bits will be missed.  |

## Register 7Ch. TX FIFO Control 1

| Bit         | D7       | D6 | D5           | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----|--------------|----|----|----|----|----|
| <b>Name</b> | Reserved |    | txafthr[5:0] |    |    |    |    |    |
| <b>Type</b> | R/W      |    | R/W          |    |    |    |    |    |

Reset value = 00110111

| Bit  | Name         | Function                              |
|------|--------------|---------------------------------------|
| 7: 6 | Reserved     | <b>Reserved.</b>                      |
| 5: 0 | txafthr[5:0] | <b>TX FIFO Almost Full Threshold.</b> |

## Register 7Dh. TX FIFO Control 2

| Bit         | D7       | D6 | D5            | D4 | D3  | D2 | D1 | D0 |
|-------------|----------|----|---------------|----|-----|----|----|----|
| <b>Name</b> | Reserved |    | txfaethr[5:0] |    |     |    |    |    |
| <b>Type</b> | R/W      |    |               |    | R/W |    |    |    |

Reset value = 00000100

| Bit  | Name          | Function                               |
|------|---------------|--|
| 7: 6 | Reserved      | <b>Reserved.</b>                       |
| 5: 0 | txfaethr[5:0] | <b>TX FIFO Almost Empty Threshold.</b> |

## Register 7Fh. FIFO Access

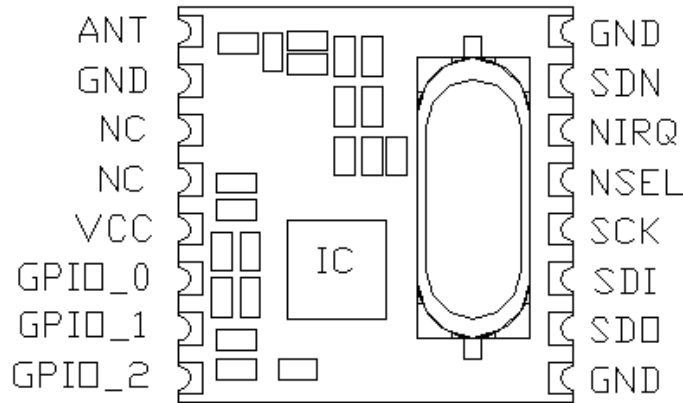
| Bit         | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|----|----|----|----|----|----|----|
| <b>Name</b> | fifod[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W        |    |    |    |    |    |    |    |

Reset value = NA

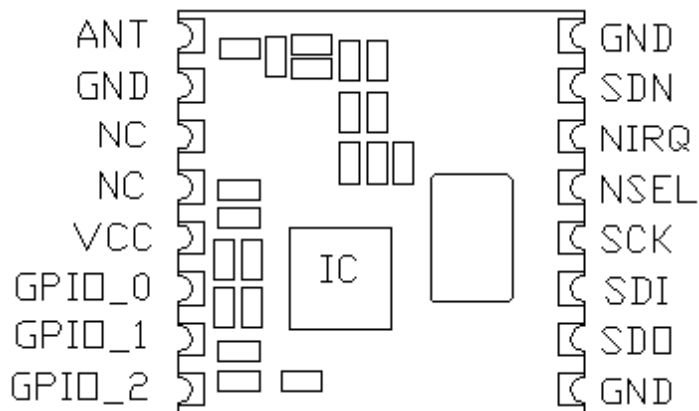
| Bit  | Name       | Function  |
|------|------------|---|
| 7: 0 | fifod[7:0] | <p><b>FIFO Data.</b></p> <p>A Write (R/W = 1) to this Address will begin a Burst Write to the TX FIFO. The FIFO will be loaded in the same manner as a Burst SPI Write but the SPI address will not be incremented. To conclude the TX FIFO Write the SEL pin should be brought HIGH, in the same manner.</p> |

**11. Pin Descriptions: RFM42/43**

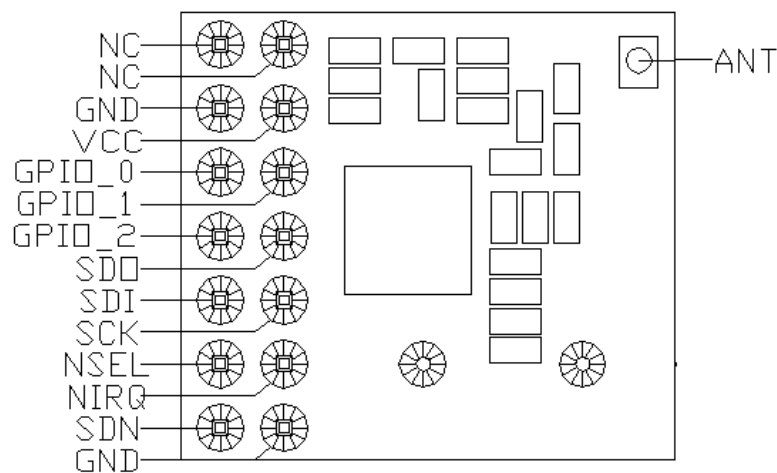
**RFM42/43-S1**



**RFM42/43-S2**



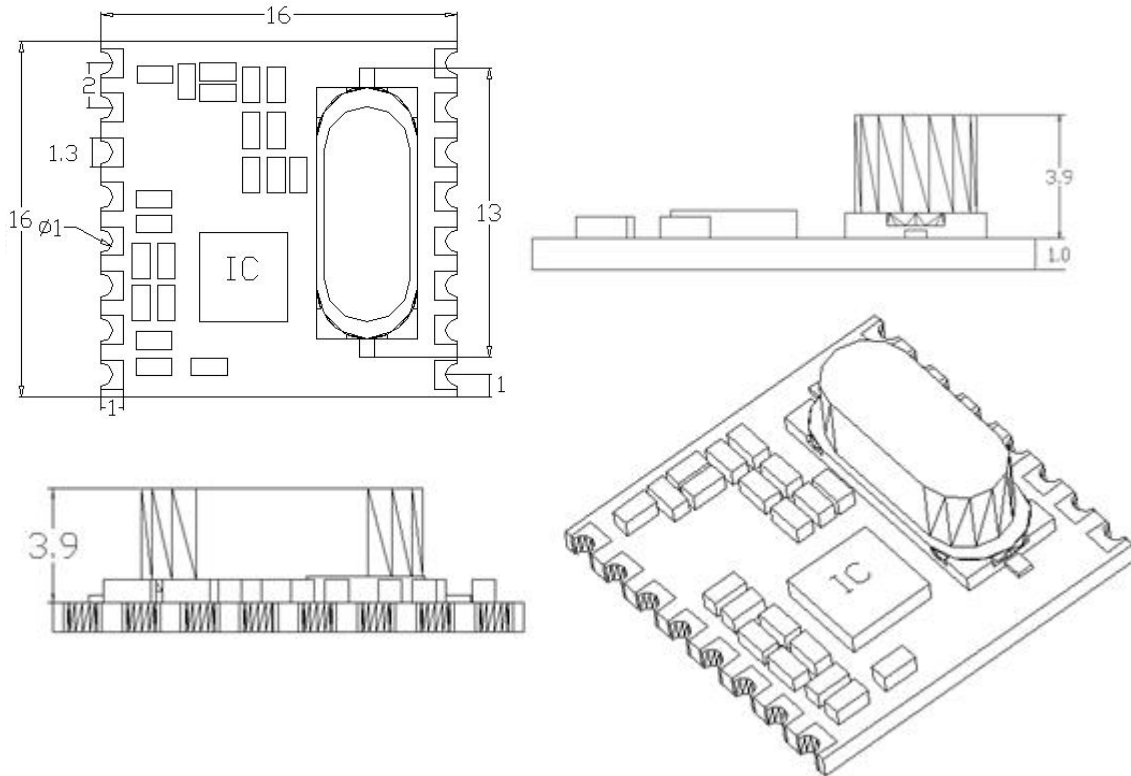
**RFM42/43-D**



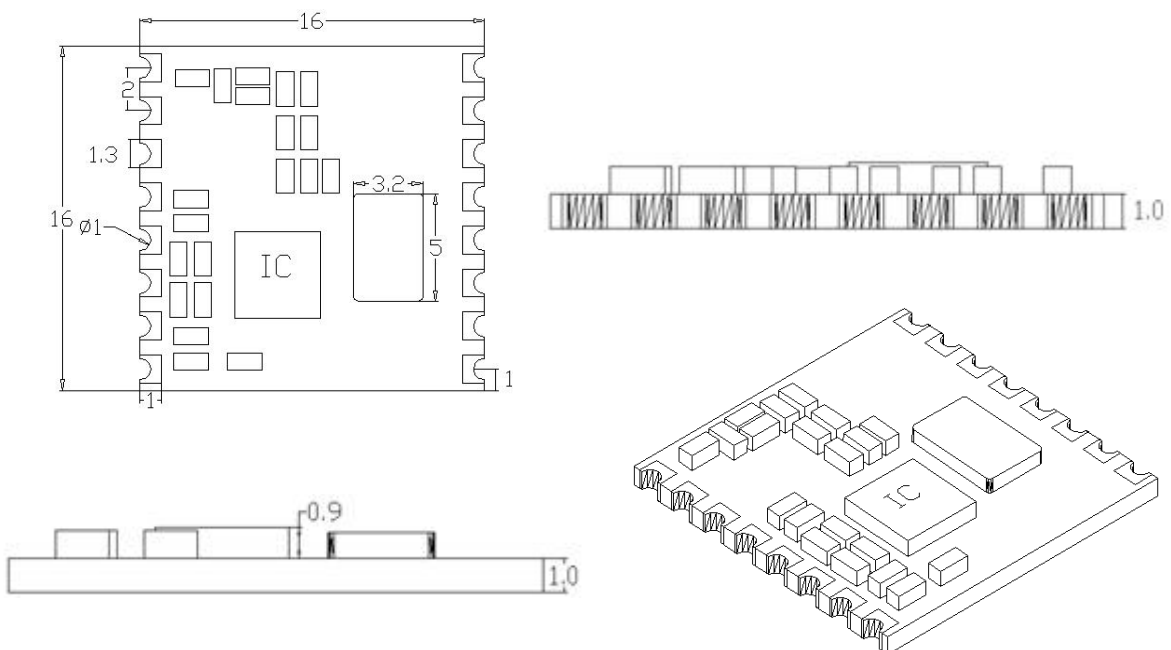
|        |     |   |
|--------|-----|---|
| VCC    | S   | +1.8 to +3.6 V supply voltage. The recommended Vcc supply voltage is +3.3 V.  |
| GND    | S   | Ground reference.   |
| GPIO_0 | I/O | General Purpose Digital I/O that may be configured through the registers to perform various functions including: Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, TRSW, AntDiversity control, etc. See the SPI GPIO Configuration Registers, Address 0Bh, 0Ch, and 0Dh for more information.  |
| GPIO_1 | I/O |   |
| GPIO_2 | I/O |   |
| SDO    | O   | 0–Vcc V digital output that provides a serial readback function of the internal control registers.  |
| SDI    | I   | Serial Data input. 0–Vcc V digital input. This pin provides the serial data stream for the 4-line serial data bus.  |
| SCLK   | I   | Serial Clock input. 0–VDD V digital input. This pin provides the serial data clock function for the 4-line serial data bus. Data is clocked into the RFM42/43 on positive edge transitions.   |
| nSEL   | I   | Serial Interface Select input. 0– Vcc V digital input. This pin provides the Select/Enable function for the 4-line serial data bus. The signal is also used to signify burst read/write mode.   |
| nIRQ   | O   | General Microcontroller Interrupt Status output. When the RFM42/43 exhibits anyone of the Interrupt Events the nIRQ pin will be set low=0. Please see the Control Logic registers section for more information on the Interrupt Events. The Microcontroller can then determine the state of the interrupt by reading a corresponding SPI Interrupt Status Registers, Address 03h and 04h. |
| SDN    | I   | Shutdown input pin. 0–Vcc V digital input. SDN should be = 0 in all modes except Shutdown mode. When SDN =1 the chip will be completely shutdown and the contents of the registers will be lost.  |
| ANT    | I/O | RF signal output/input.(50 OHM output /input Impedance)   |
| NC     |     | No Connection   |

**12. Mechanical Dimension:RFM42/43**

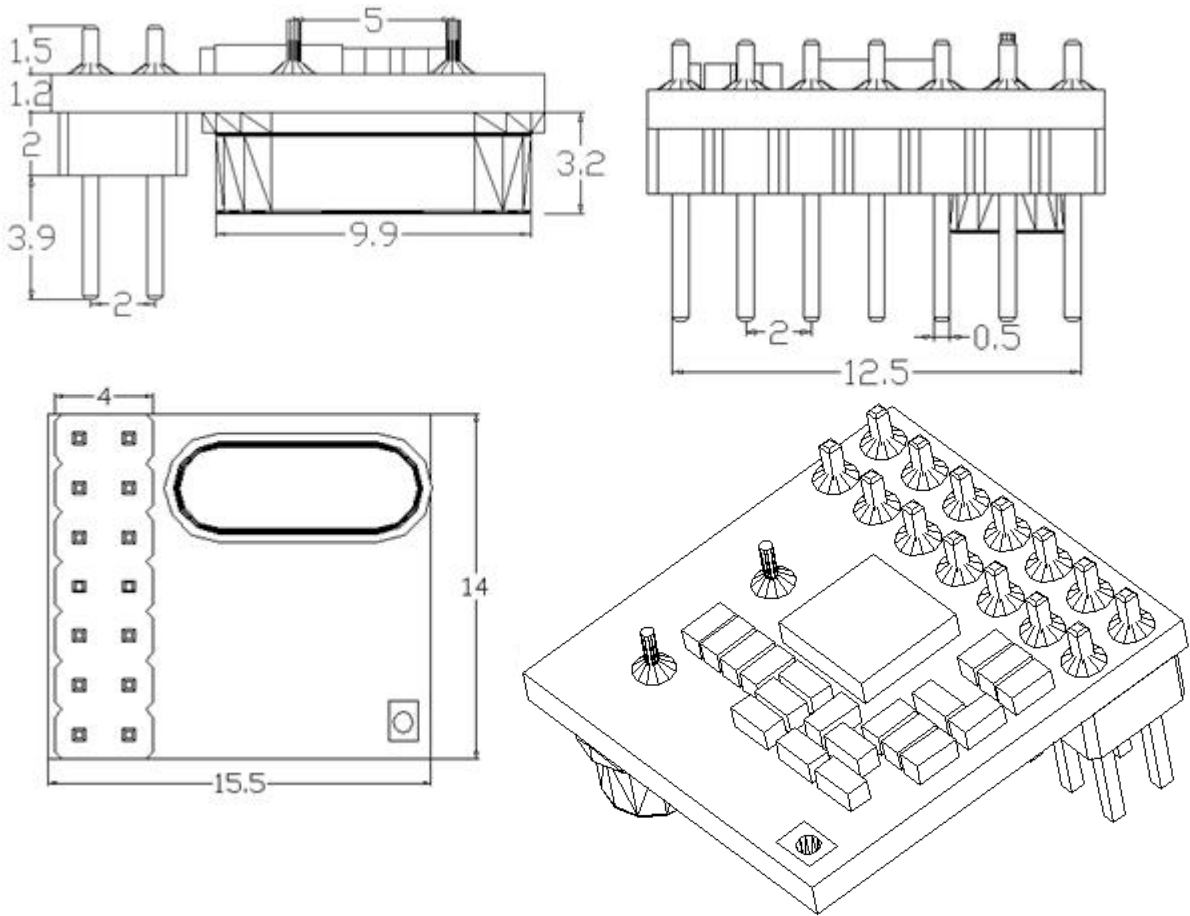
**SMD PACKAGE (S1)**



**SMD PACKAGE (S2)**



DIP PACKAGE (D)



### 13. Ordering Information

Part Number=module type—operation band—package type

**RFM42/43—433—D**

↑                      ↑                      ↑  
module type    operation band    Package

example: 1, RFM43 module at 433MHz band, DIP : RFM43-433-D.

2, RFM42 module at 868MHZ band, SMD, thickness at 4.9mm: RFM42-868-S1.

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