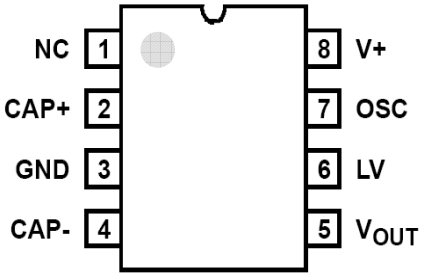
FEATURES

- Simple Conversion of +5V Logic Supply to ±5V Supplies
- Simple Voltage Multiplication (VOUT = (-) nVIN)
- Typical Open Circuit Voltage Conversion Efficiency 99.9%
- Typical Power Efficiency 98%
- Wide Operating Voltage Range- TJ7660 1.5V to 10.0V
- Easy to Use - Requires Only 2 External Non-Critical Passive Components
- No External Diode Over Full Temp. and Voltage Range
- Moisture Sensitivity Level 3

SOP-8 PKG

DIP-8 PKG



< Pin Configuration >

APPLICATION

- On Board Negative Supply for Dynamic RAMs
- Localized µProcessor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

ORDERING INFORMATION

Device	Package
TJ7660D	SOP-8
TJ7660N	D I P-8

DESCRIPTION

The HTC TJ7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices.
The TJ7660 performs supply voltage conversions from positive to negative for an input range of +1.5V to +10.0V resulting in complementary output voltages of −1.5V to −10.0V. Only 2 noncritical external capacitors are needed for the charge pump and charge reservoir functions.
The TJ7660 can also be connected to function as voltage doublers and will generate output voltages up to +18.6V with a +10V input. Contained on the chip are a series DC supply regulator, RC oscillator, voltage level translator, and four output power MOS switches.
A unique logic element senses the most negative voltage in the device and ensures that the output N-Channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0V.
This frequency can be lowered by the addition of an external capacitor to the “OSC” terminal, or the oscillator may be overdriven by an external clock.

The “LV” terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5V to +10.0V for the TJ7660), the LV pin is left floating to prevent device latchup.

Absolute Maximum Ratings

Supply Voltage TJ7660	+10.5V	V
LV and OSC Input Voltage (Note2)	−0.3V to [(V+ +0.3V) for V+] < 5.5V	V
	(V+ −5.5V) to [(V+ +0.3V) for V+] > 5.5V	
Current into LV (Note 2)	20μA for V+ > 3.5V	uA
Output Short Duration (VSUPPLY ≤ 5.5V)	Continuous	
Operating Ambient Temperature	−20 to 70	℃

Thermal Information

Thermal Resistance (Typical, Note 1)	Θ_{JA} (℃/W)	Θ_{JC} (℃/W)
PDIP Package	150	N/A
SOIC Package	165	N/A
Metal Can Package (TJ7660 Only)	160	70
Maximum Storage Temperature Range	−65℃ to 150℃	
Maximum Lead Temperature (Soldering, 10s)	300℃	
(SOIC − Lead Tips Only)		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

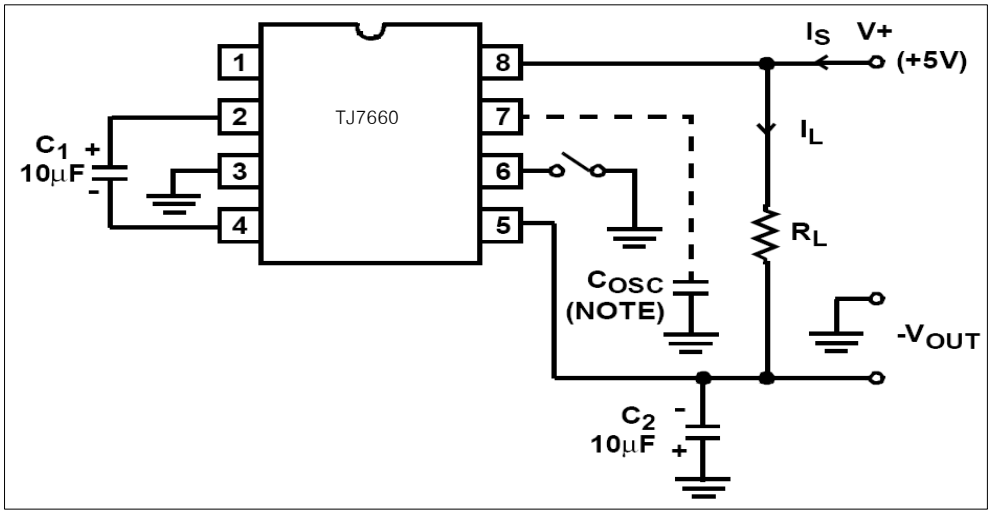
ELECTRICAL CHARACTERISTIC (TJ7660, V+ = 5V, TA = 25oC, COSC = 0, unless Otherwise Specified)

PARAMETER	SYMBOL	TEST CONDITIONS	TJ7660			UNITS
			MIN	TYP	MAX	
Supply Current	I+	$R_L = \infty$	–	100	180	μA
Supply Voltage Range −Lo	V_{L+}	MIN ≤ T_A ≤ MAX, R_L =10kΩ, LV to GND	2.0	–	3.5	V
Supply Voltage Range −Hi	V_{H+}	MIN ≤ T_A ≤ MAX, RL =10kΩ,LVto Open	3	–	–	V
Output Source Resistance	R_{OUT}	I_{OUT} =20mA, T_A =25℃	–	60	100	Ω
		I_{OUT} =20mA, −20℃ ≤ T_A ≤ 70℃	–	–	–	Ω
		V+ = 2V, I_{OUT} = 3mA, LV to GND −20℃≤ T_A ≤ 70℃	–	–	300	Ω
		V+ = 2V, I_{OUT} = 3mA, LV to GND, −20℃ ≤ T_A ≤ 70℃	–	–	400	Ω
Oscillator Frequency	f_{OSC}		–	10	–	kHz
Power Efficiency	P_{EF}	R_L =5kΩ	95	98	–	%
Voltage Conversion Efficie	$V_{OUT\ EF}$	$R_L = \infty$	98	99.9	–	%

NOTES

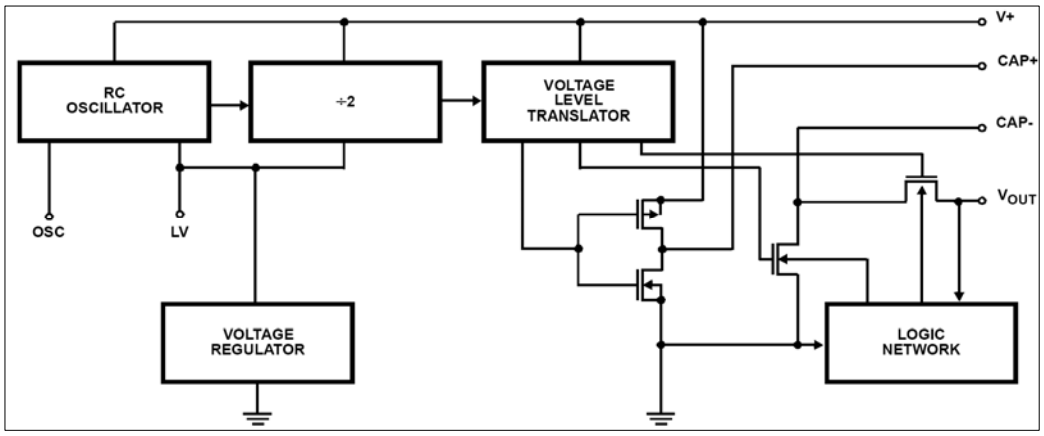
1. ΘJA is measured with the component mounted on an evaluation PC board in free air.
2. Connecting any input terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TJ7660.

Test Circuit

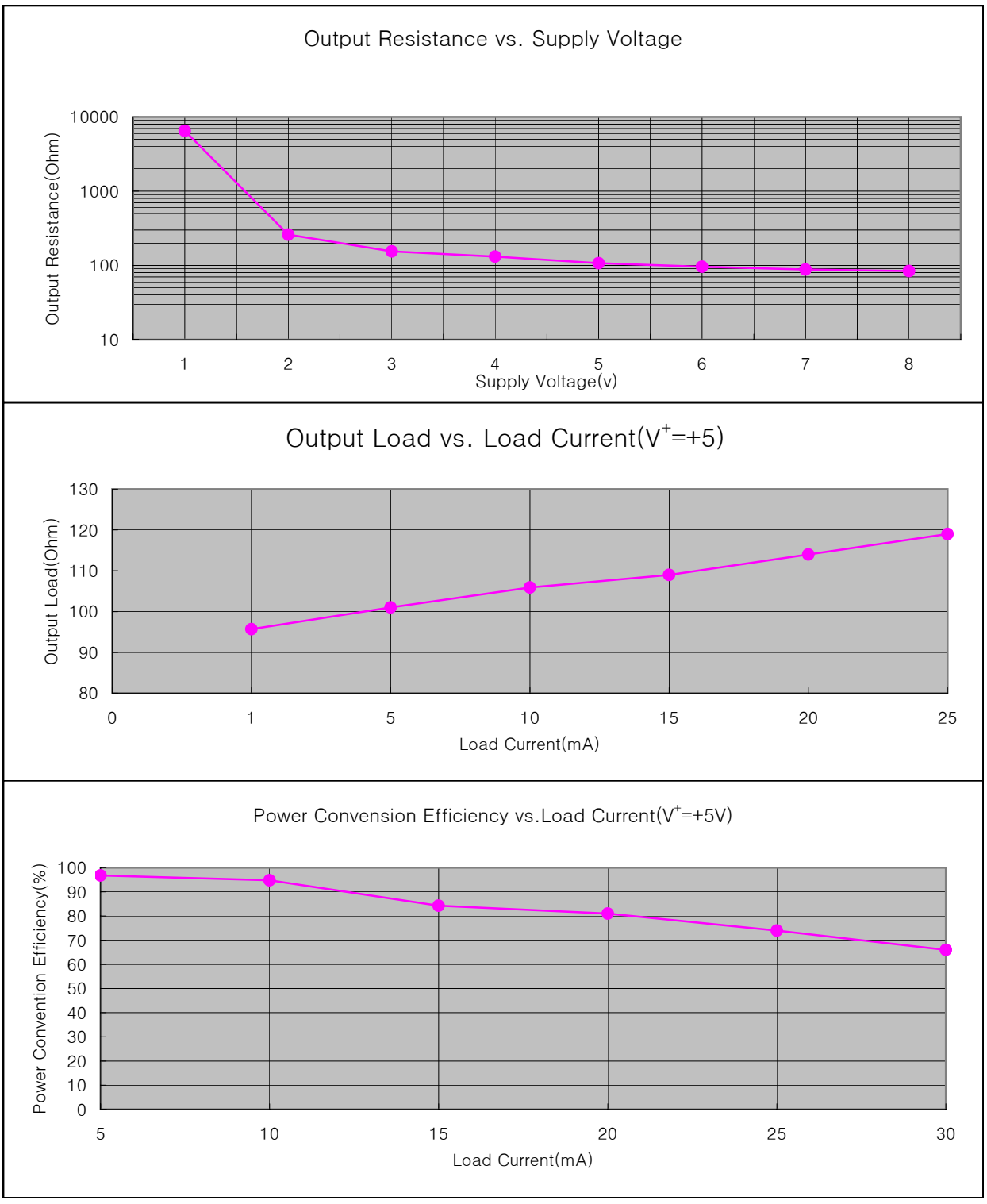


NOTE: For large values of C_{OSC} (>1000pF) the values of C_1 and C_2 should be increased to 100μF.

BLOCK DIAGRAM



Typical Performance Curves



NOTE:

6. These curves include in the supply current that current fed directly into the load RL from the V+ (See Figure 11). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the TJ7660, to the negative side of the load. Ideally, $V_{OUT} = 2V_{IN}$, $I_S = 2I_L$, so $V_{IN} \times I_S = V_{OUT} \times I_L$.

Detailed Description

The TJ7660 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10μF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure12, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second halfcycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V+, assuming ideal switches and no load on C_2. The TJ 7660 approaches this ideal situation more closely than existing non-mechanical circuits.
In the TJ7660, the 4 switches of Figure 12 are MOS power switches; S_1 is a P-Channel device and S_2, S_3 and S_4 are N-Channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit start-up, and under output short circuit conditions (V_{OUT} = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.
This problem is eliminated in the TJ7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.
The voltage regulator portion of the TJ7660 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5V the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

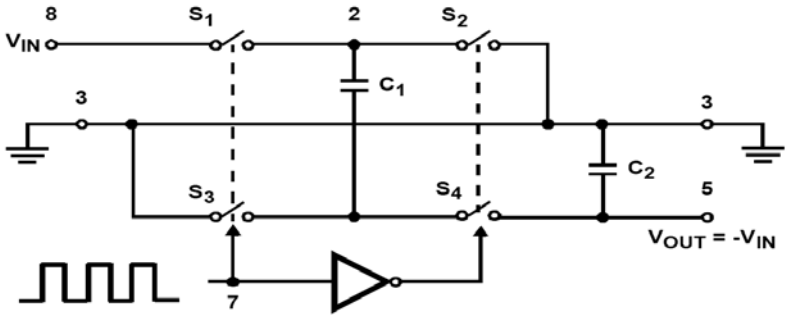


FIGURE 12. IDEALIZED NEGATIVE VOLTAGE CONVERTER

Theoretical Power Efficiency Considerations

In theory a voltage converter can approach 100% efficiency if certain conditions are met.
1. The driver circuitry consumes minimal power.
2. The output switches have extremely low ON resistance and virtually no offset.
3. The impedances of the pump and reservoir capacitors are negligible at the pump frequency.
The TJ7660 approaches these conditions for negative voltage conversion if large values of C_1 and C_2 are used.

ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS. The energy lost is defined by: $E = 1/2\ C_1\ (V_1^2 - V_2^2)$
where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 12) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Do's And Don'ts

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5V.
3. Do not short circuit the output to V+ supply for supply voltages above 5.5V for extended periods, however, transient conditions including start-up are okay.
4. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the TJ7660 and the + terminal of C_2 must be connected to GROUND.
5. If the voltage supply driving the TJ7660 has a large source impedance (25Ω – 30Ω), then a 2.2μF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/μs.
6. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions. A 1N914 or similar diode placed in parallel with C_2 will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 3).

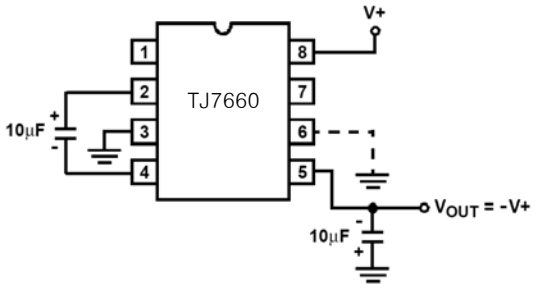


FIGURE 13A. CONFIGURATION

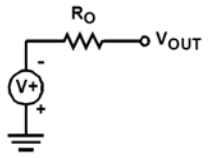


FIGURE 13B. THEVENIN EQUIVALENT

FIGURE 13. SIMPLE NEGATIVE CONVERTER

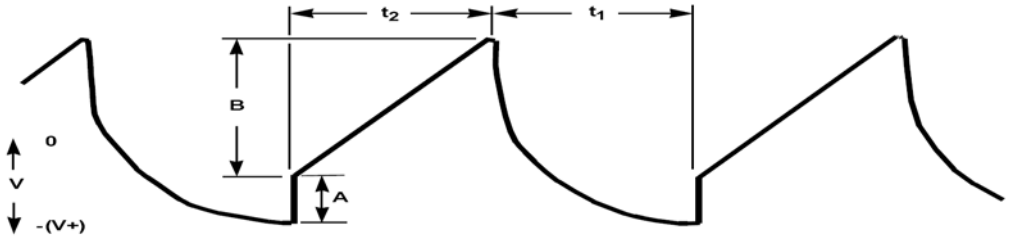


FIGURE 14. OUTPUT RIPPLE

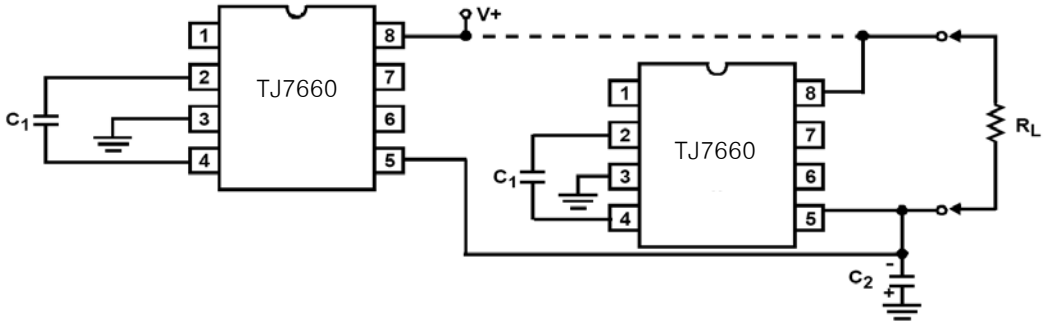


FIGURE 15. PARALLELING DEVICES

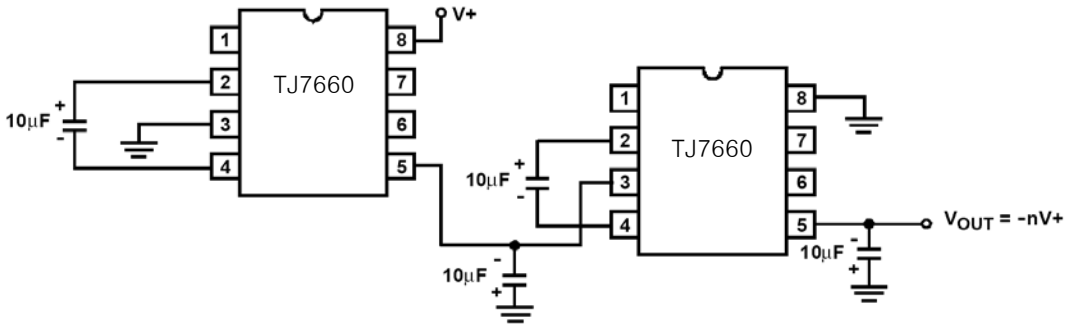


FIGURE 16. CASCADING DEVICES FOR INCREASED OUTPUT VOLTAGE

Typical Applications

Simple Negative Voltage Converter

Themajority of applications will undoubtedly utilize the TJ7660 for generation of negative supply voltages. Figure 13 shows typical connections to provide a negative supply negative (GND) for supply voltages below 3.5V.

The output characteristics of the circuit in Figure 13A can be approximated by an ideal voltage source in series with a resistance as shown in Figure 13B. The voltage source has a value of −V+. The output impedance (R_O) is a function of the ON resistance of the internal MOS switches (shown in Figure 12), the switching frequency, the value of C_1 and C_2, and the ESR (equivalent series resistance) of C1 and C2. A good first order approximation for R_O is:

$$R_O = 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) +$$

$$R_O = 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 1/(f_{PUMP})\ (C1) + ESR_{C2}$$

($f_{PUMP} = f_{OSC}/2$, R_{SWX} = MOSFET switch resistance)

Combining the four R_{SWX} terms as R_{SW}, we see that:

$$R_O = 2\ (R_{SW}) + 1/(f_{PUMP})\ (C1) + 4\ (ESR_{C1}) + ESR_{C2}$$

RSW, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 23Ω at 25°C and 5V. Careful selection of C_1 and C_2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \bullet C_1)$ component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \bullet C1)$ term, but may have the side effect of a net increase in output impedance when C_1 > 10µF and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where f_{OSC} = 10kHz and C = C_1 = C_2 = 10µF:

$$R_O = 2\ (23) + 1/(5 \bullet 10^3)\ (10^{-5}) + 4\ (ESR_{C1}) + ESR_{C2}$$

$$R_O = 46 + 20 + 5\ (ESR_C)$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \bullet C_1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 14. Segment A is the voltage drop across the ESR of C_2 at the instant it goes from being charged by C_1 (current flow into C_2) to being discharged through the load (current flowing out of C_2). The magnitude of this current change is 2• I_{OUT}, hence the total drop is 2• I_{OUT} • $eSR_{C2}V$. Segment
B is the voltage change across C_2 during time t_2, the half of the cycle when C_2 supplies current to the load. The drop at B is I_{OUT} • $t2/C_2V$. The peak-to-peak ripple voltage is the sum of these voltage drops:

$VRIPPLE = [\ 1/2\ (f_{PUMP})\ (C2) + 2\ (ESR_{C2})]\ I_{OUT}$
Again, a low ESR capacitor will reset in a higher performance output.

Paralleling Devices

Any number of TJ7660 voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$R_{OUT} = R_{OUT}$ (of TJ7660)/n (number of devices)

Cascading Devices

The TJ7660 may be cascaded as shown to produced larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$V_{OUT} = -n\ (V_{IN})$,

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TJ7660 R_{OUT} values.

Changing the TJ7660 Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 17. In order to prevent possible device latchup, a 1kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

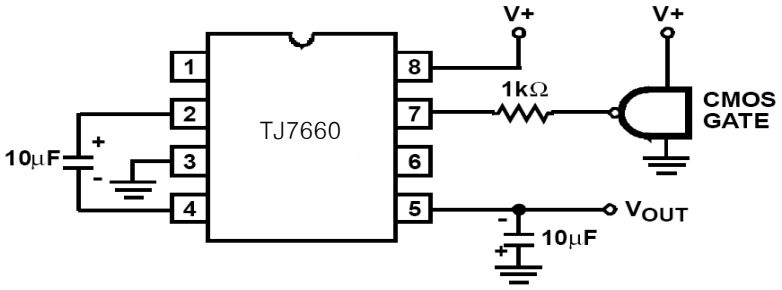


FIGURE 17. EXTERNAL CLOCKING

It is also possible to increase the conversion efficiency of the TJ7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 18. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7(OSC) and V+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2(from 10μF to 100μF).

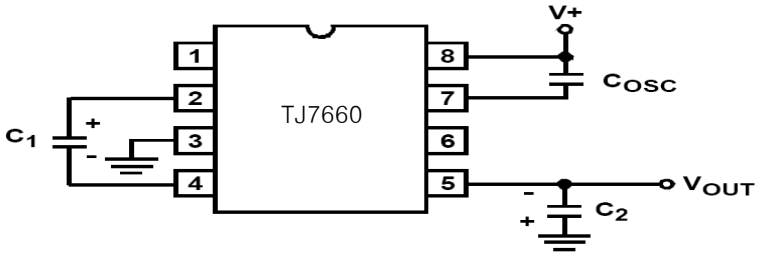


FIGURE 18. LOWERING OSCILLATOR FREQUENCY

Positive Voltage Doubling

The TJ7660 may be employed to achieve positive voltage doubling using the circuit shown in Figure19. In this application, the pump inverter switches of the TJ7660 are used to charge C_1 to a voltage level of V+ −VF (where V+ is the supply voltage and VF is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes (2V+) − (2VF) or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V+ = 5V and an output current of 10mA it will be approximately 60Ω.

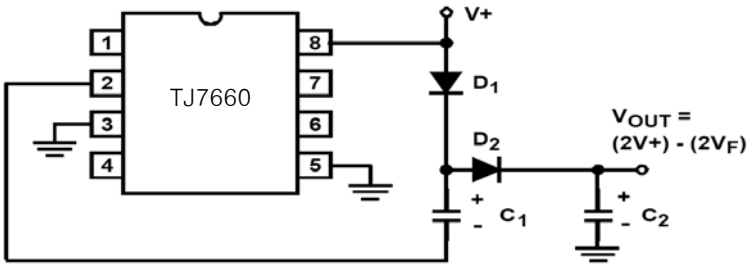


FIGURE 19. POSITIVE VOLT DOUBLER

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 20 combines the functions shown in Figures 13 and Figure 19 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9V and −5V from an existing +5V supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

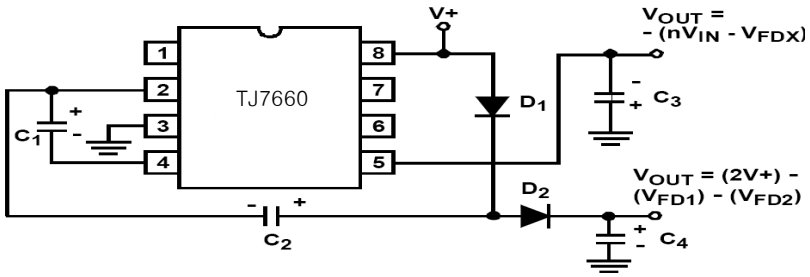


FIGURE 20. COMBINED NEGATIVE VOLTAGE CONVERTER AND POSITIVE DOUBLER

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 21. The combined load will be evenly shared between the two sides. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 16, +15V can be converted (via +7.5, and −7.5) to a nominal −15V, although with rather high series output resistance (~250Ω).

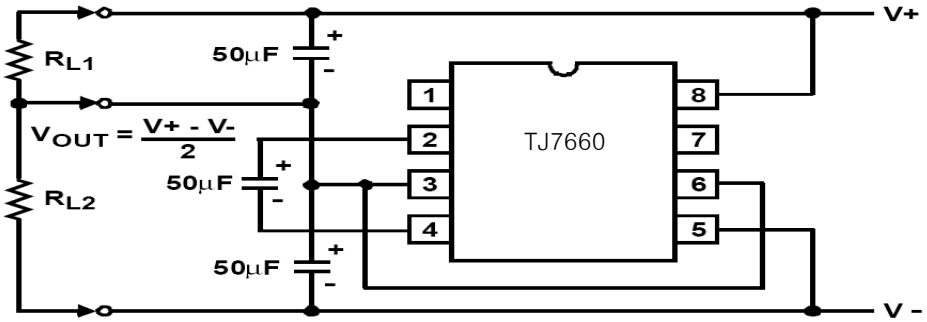


FIGURE 21. SPLITTING A SUPPLY IN HALF

Regulated Negative Voltage Supply

In some cases, the output impedance of the TJ7660 can be a problem, particularly if the load current

varies substantially. The circuit of Figure 22 can be used to overcome this by controlling the input voltage, via an TJ7611 low−power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the TJ7660s and TJ7660As output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the TJ7660, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

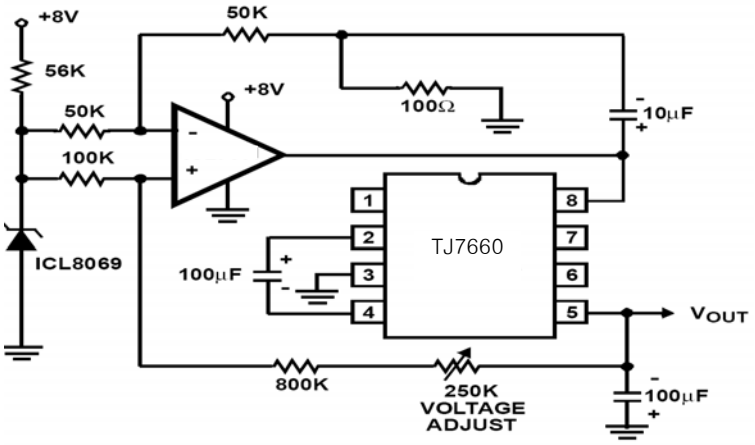


FIGURE 22. REGULATING THE OUTPUT VOLTAGE

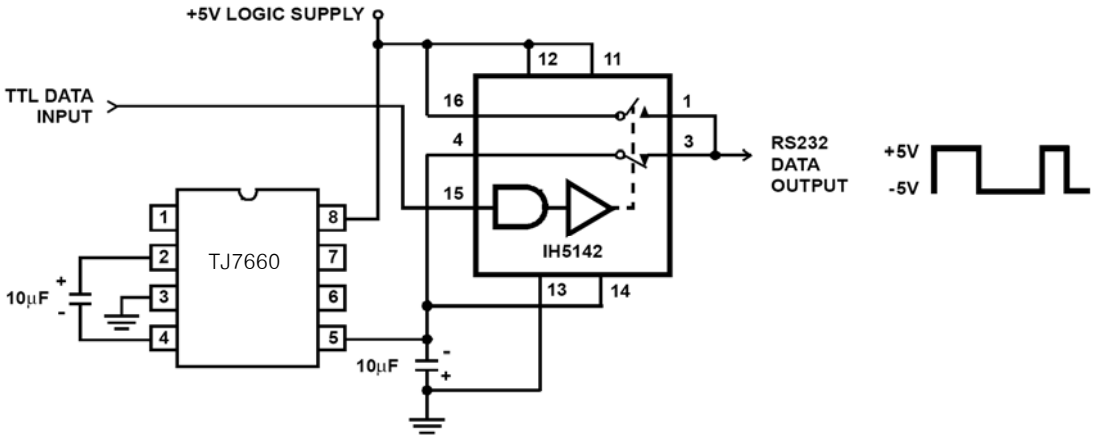


FIGURE 23. RS232 LEVELS FROM A SINGLE 5V SUPPLY

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