36V, Precision Low-Noise Operational Amplifiers

GENERAL DESCRIPTION

The HTx177 family consists of very high precision, single, dual, and quad amplifiers featuring extremely low offset voltage and drift, low input bias current, low noise, and low power consump-tion. Outputs are stable with capacitive loads of over 1000 pF
with no external compensation. Supply current is less than 500 µA per amplifier at 30 V. Internal 500 Ω series resistors protect the inputs, allowing input signal levels several volts beyond either supply without phase reversal.Unlike previous high voltage amplifiers with very low offset voltages, the HT1177 (single) and HT2177 (dual) amplifiers are available in tiny 8-lead surface-mount MSHT and 8-lead narrow SOIC packages. The HT4177 (quad) is available in TSSHT and 14-lead narrow SOIC packages. Moreover, specified performance in the MSHT and the TSSHT is identical to performance in the SOIC package. MSHT and TSSHT are available in tape and reel only.

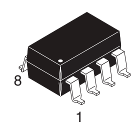
FEATURES

Low offset voltage: 60 µV maximum
Very low offset voltage drift: 0.7 µV/°C maximum
Low input bias current: 2 nA maximum
Low noise: 8 nV/√Hz typical
CMRR, PSRR, and A_{VO} > 120 dB minimum
Low supply current: 400 µA per amplifier
Dual supply HTeration: ±2.5 V to ±15
V Unity-gain stable
No phase reversal
Inputs internally protected beyond supply voltage

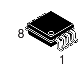
APPLICATIONS

Wireless base station control circuits
HTtical network control circuits
Instrumentation
Sensors and controls
- Thermocouples
- Resistor thermal detectors (RTDs)
- Strain bridges
- Shunt current measurements

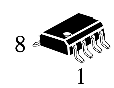
Precision filters



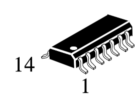
DIP8 U SUFFIX



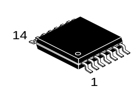
MSOP8 M SUFFIX



SOP8 R SUFFIX



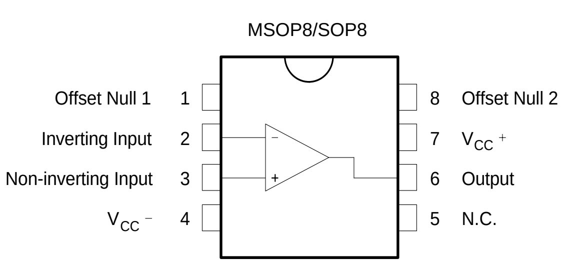
SOP14 R SUFFIX

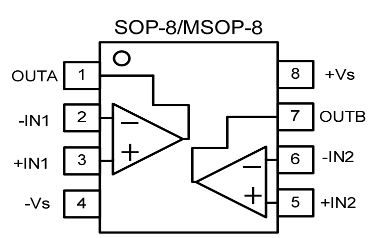


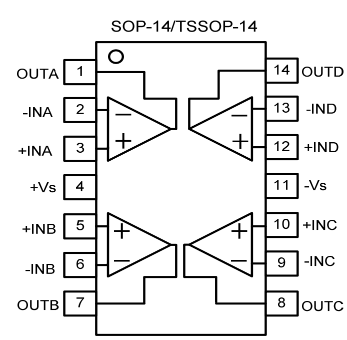
TSSOP14 T SUFFIX

NOTE: If you need to customize the packaging shape, please contact the manufacturer.

PIN CONFIGURATIONS







ELECTRICAL CHARACTERISTICS

$V_S = \pm 5.0$ V, $V_{CM} = 0$ V, $T_A = 25$ ℃, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
HT1177	V_{OS}			15	60	μV
HT2177/HT4177	V_{OS}			15	75	μV
HT1177/HT2177	V_{OS}	−40°C < T_A < +125°C		25	100	μV
HT4177	V_{OS}	−40°C < T_A < +125°C		25	120	μV
Input Bias Current	I_B	−40°C < T_A < +125°C	−2	+0.5	+2	nA
Input Offset Current	I_{OS}	−40°C < T_A < +125°C	−1	+0.2	+1	nA
Input Voltage Range			−3.5		+3.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −3.5 V to +3.5 V	120	126		dB
		−40°C < T_A < +125°C	118	125		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = −3.5 V to +3.5 V	1000	2000		V/mV
Offset Voltage Drift						
HT1177/HT2177	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		0.2	0.7	μV/°C
HT4177	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		0.3	0.9	μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA, −40°C < T_A < +125°C	+4	+4.1		V
Output Voltage Low	V_{OL}	I_L = 1 mA, −40°C < T_A < +125°C		−4.1	−4	V
Output Current	I_{OUT}	$V_{DRHTOUT}$ < 1.2 V		±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio						
HT1177	PSRR	V_S = ±2.5 V to ±15 V	120	130		dB
		−40°C < T_A < +125°C	115	125		dB
HT2177/HT4177	PSRR	V_S = ±2.5 V to ±15 V	118	121		dB
		−40°C < T_A < +125°C	114	120		dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V		400	500	μA
		−40°C < T_A < +125°C		500	600	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		0.7		V/μs
Gain Bandwidth Product	GBP			1.3		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.4		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		7.9	8.5	nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	DC		0.01		μV/V
		f = 100 kHz		−120		dB

[1] Typical values cover all parts within one standard deviation of the average value. Average values given in many competitor datasheets as typical give unrealistically low estimates for parameters that can have both positive and negative values.

V_S = ±15 V, V_{CM} = 0 V, T_A = 25 °C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
HT1177	V_{OS}			15	60	μV
HT2177/HT4177	V_{OS}			15	75	μV
HT1177/HT2177	V_{OS}	−40°C < T_A < +125°C		25	100	μV
HT4177	V_{OS}	−40°C < T_A < +125°C		25	120	μV
Input Bias Current	I_B	−40°C < T_A < +125°C	−2	+0.5	+2	nA
Input Offset Current	I_{OS}	−40°C < T_A < +125°C	−1	+0.2	+1	nA
Input Voltage Range			−13.5		+13.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −13.5 V to +13.5 V,				
		−40°C < T_A < +125°C	120	125		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = −13.5 V to +13.5 V	1000	3000		V/mV
Offset Voltage Drift						
HT1177/HT2177	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		0.2	0.7	μV/°C
HT4177	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		0.3	0.9	μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA, −40°C < T_A < +125°C	+14	+14.1		V
Output Voltage Low	V_{OL}	I_L = 1 mA, −40°C < T_A < +125°C		−14.1	−14	V
Output Current	I_{OUT}	$V_{DRHTOUT}$ < 1.2 V		±10		mA
Short-Circuit Current	I_{SC}			±25		mA
POWER SUPPLY						
Power Supply Rejection Ratio						
HT1177	PSRR	V_S = ±2.5 V to ±15 V	120	130		dB
		−40°C < T_A < +125°C	115	125		dB
HT2177/HT4177	PSRR	V_S = ±2.5 V to ±15 V	118	121		dB
		−40°C < T_A < +125°C	114	120		dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V		400	500	μA
		−40°C < T_A < +125°C		500	600	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		0.7		V/μs
Gain Bandwidth Product	GBP			1.3		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.4		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		7.9	8.5	nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	DC		0.01		μV/V
		f = 100 kHz		−120		dB

[1] Typical values cover all parts within one standard deviation of the average value. Average values given in many competitor datasheets as typical give unrealistically low estimates for parameters that can have both positive and negative values.

Table 3.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	V_{S-} to V_{S+}
Differential Input Voltage	±Supply Voltage
Storage Temperature Range	
R, RM, and RU Packages	−65°C to +150°C
HTerating Temperature Range	
HT1177/HT2177/HT4177	−40°C to +125°C
Junction Temperature Range	
R, RM, and RU Packages	−65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional HTeration of the device at these or any other conditions above those indicated in the HTerational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

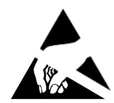
θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSHT (RM-8)[1]	190	44	°C/W
8-Lead SOIC_N (R-8)	158	43	°C/W
14-Lead SOIC_N (R-14)	120	36	°C/W
14-Lead TSSHT (RU-14)	240	43	°C/W

[1] MSHT is available in tape and reel only.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

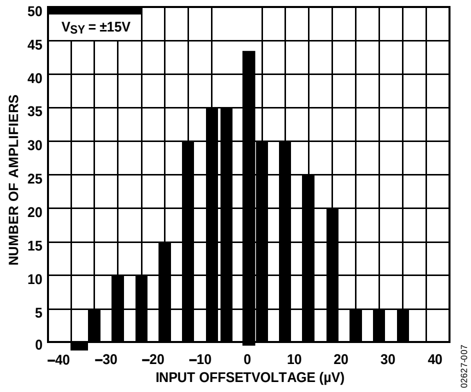


Figure 7. Input Offset Voltage Distribution

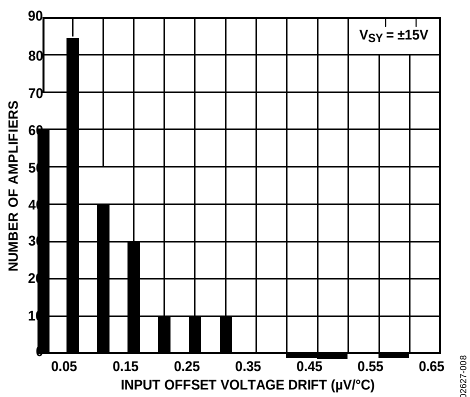


Figure 8. Input Offset Voltage Drift Distribution

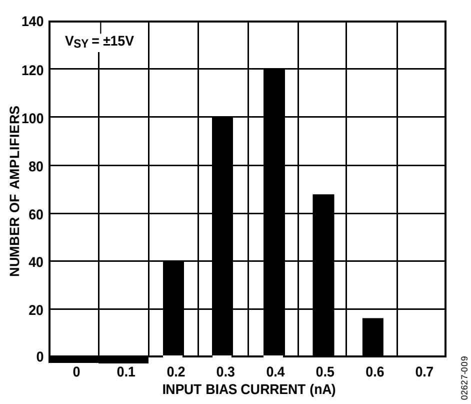


Figure 9. Input Bias Current Distribution

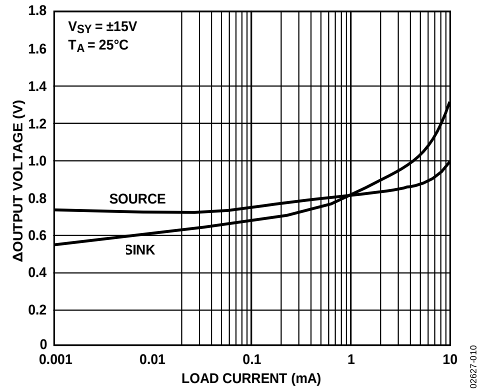


Figure 10. Output Voltage to Supply Rail vs. Load Current

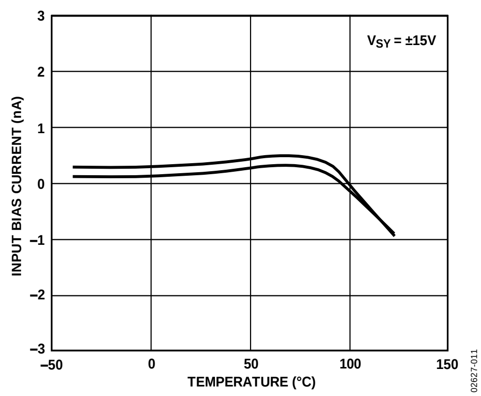


Figure 11. Input Bias Current vs. Temperature

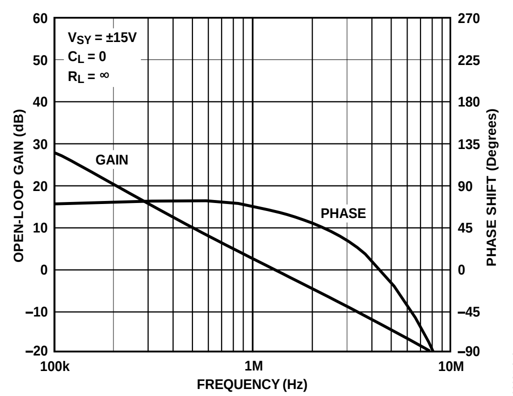


Figure 12. HTen-LoHT Gain and Phase Shift vs. Frequency

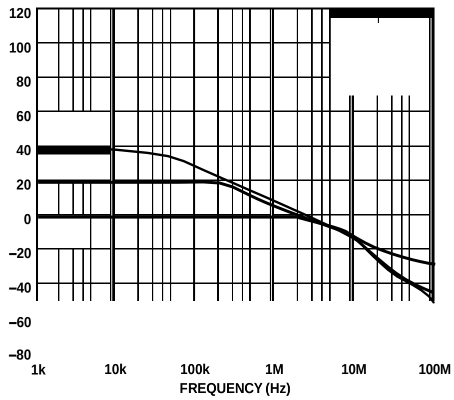


Figure 13. Closed-LoHT Gain vs. Frequency

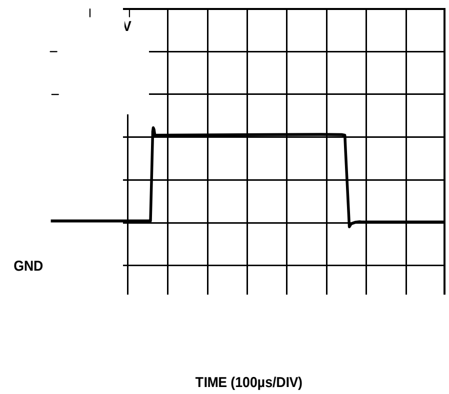


Figure 16. Small Signal Transient Response

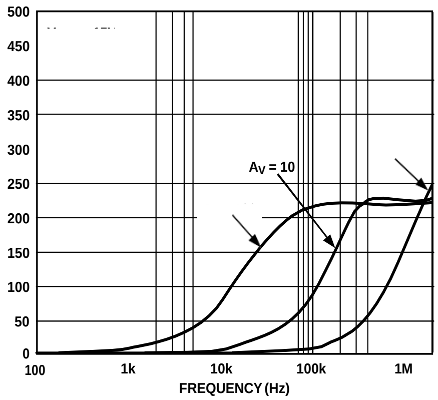


Figure 14. Output Impedance vs. Frequency

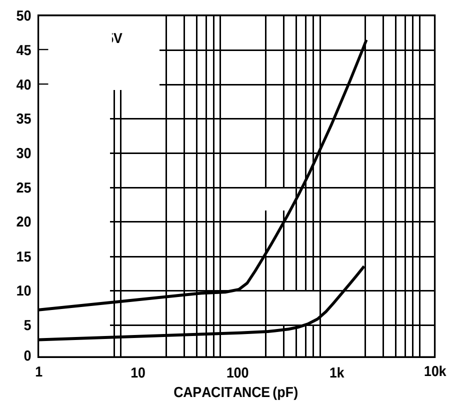


Figure 17. Small Signal Overshoot vs. Load Capacitance

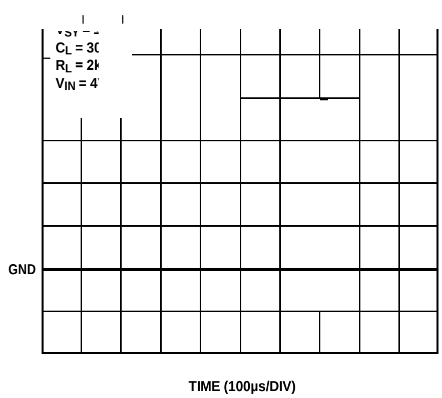


Figure 15. Large Signal Transient Response

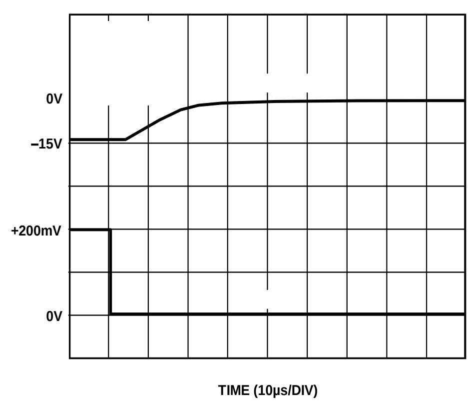


Figure 18. Positive Overvoltage Recovery

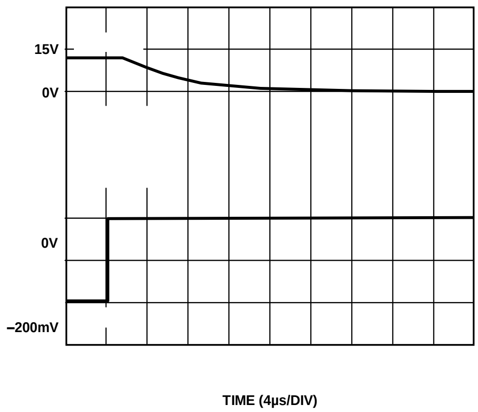


Figure 19. Negative Overvoltage Recovery

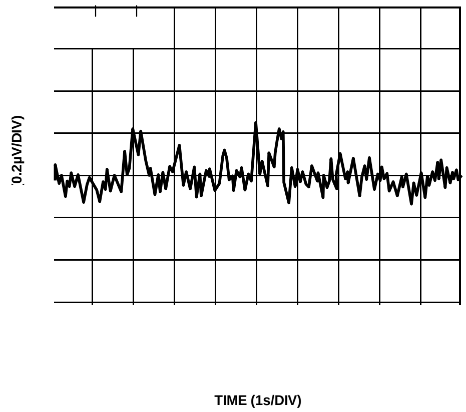


Figure 22. 0.1 Hz to 10 Hz Input Voltage Noise

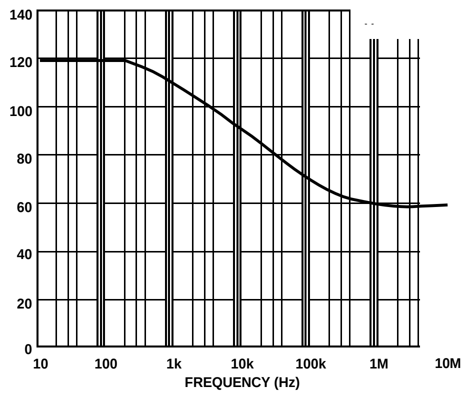


Figure 20. CMRR vs. Frequency

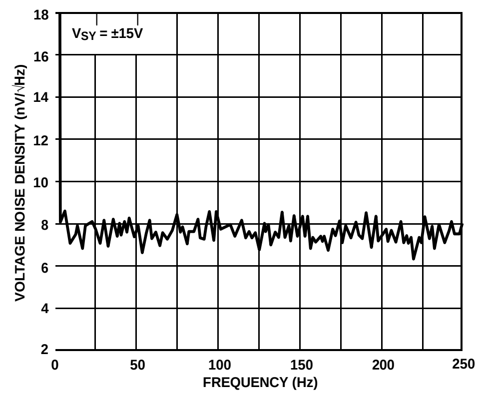


Figure 23. Voltage Noise Density vs. Frequency

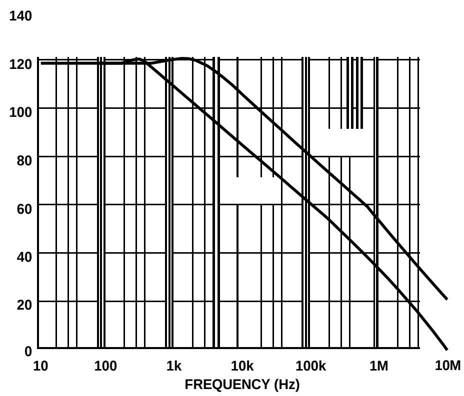


Figure 21. PSRR vs. Frequency

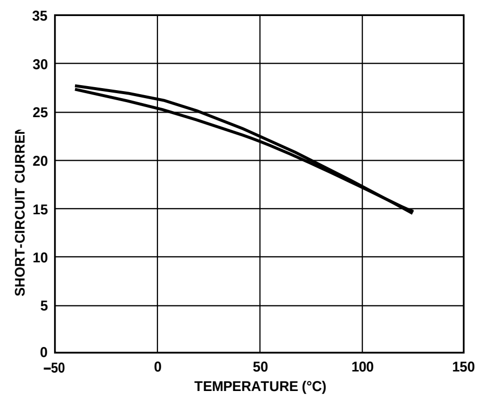


Figure 24. Short-Circuit Current vs. Temperature

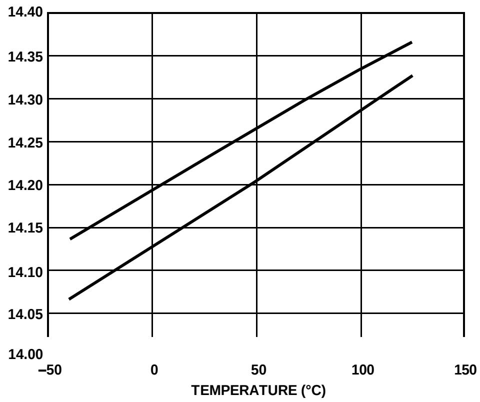


Figure 25. Output Voltage Swing vs. Temperature

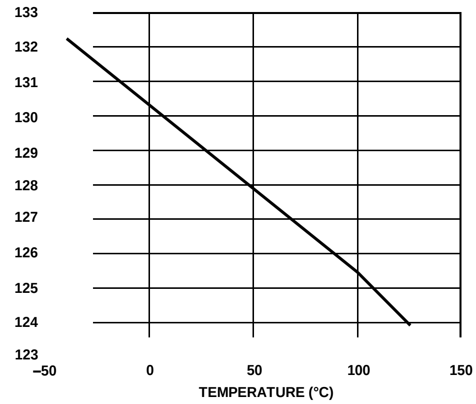


Figure 28. CMRR vs. Temperature

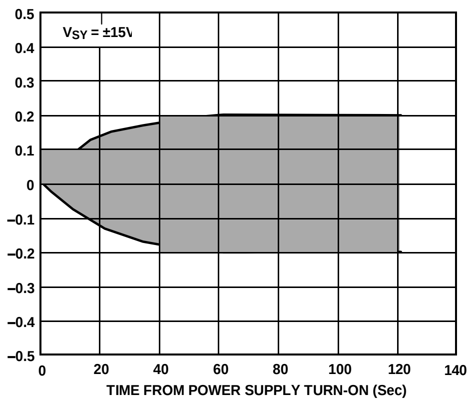


Figure 26. Warm-Up Drift

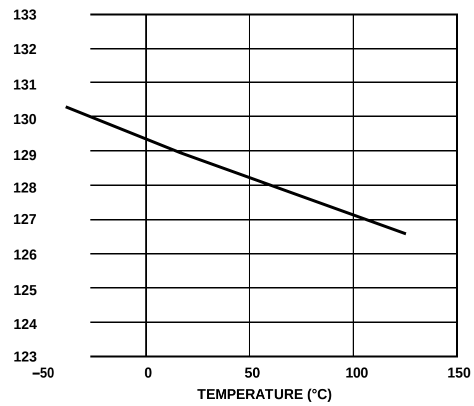


Figure 29. PSRR vs. Temperature

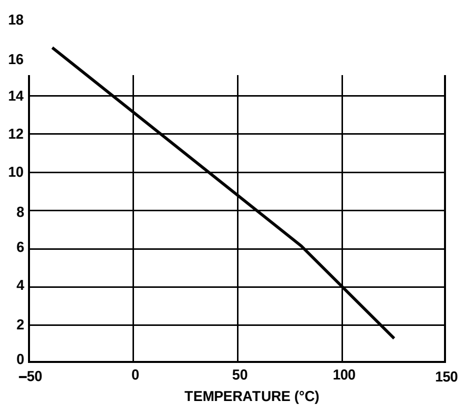


Figure 27. Input Offset Voltage vs. Temperature

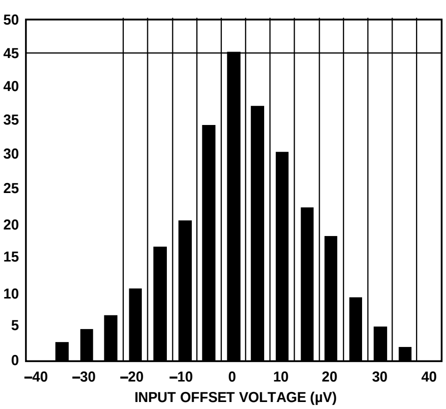


Figure 30. Input Offset Voltage Distribution

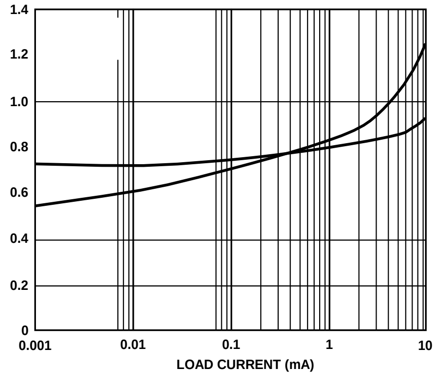


Figure 31. Output Voltage to Supply Rail vs. Load Current

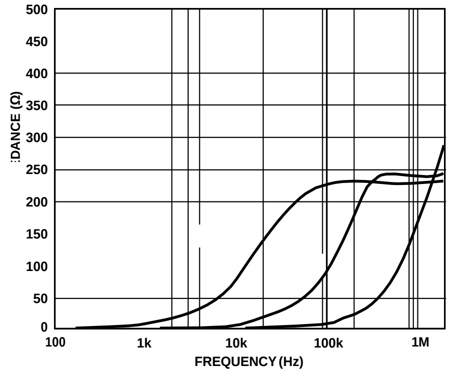


Figure 34. Output Impedance vs. Frequency

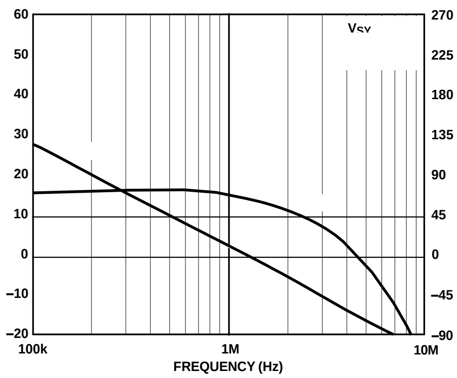


Figure 32. HTen-LoHT Gain and Phase Shift vs. Frequency

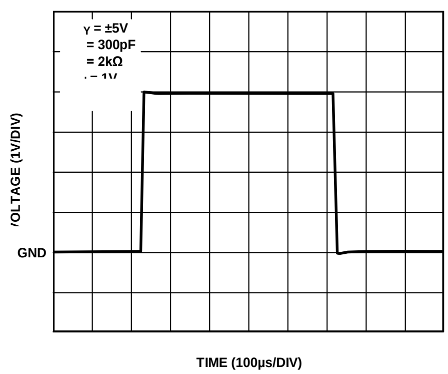


Figure 35. Large Signal Transient Response

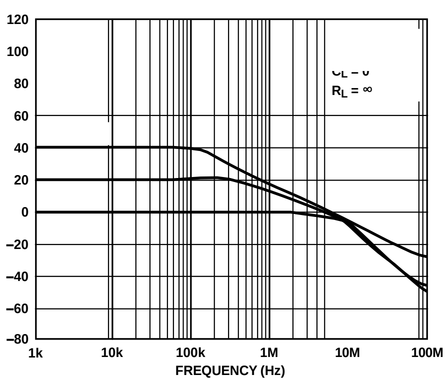


Figure 33. Closed-LoHT Gain vs. Frequency

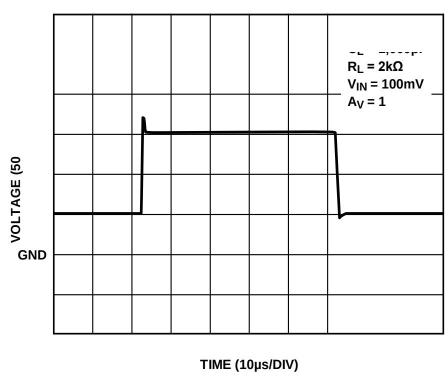


Figure 36. Small Signal Transient Response

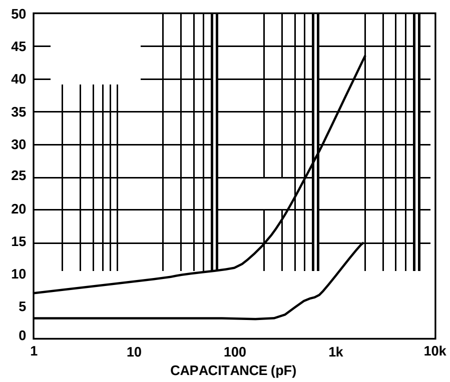


Figure 37. Small Signal Overshoot vs. Load Capacitance

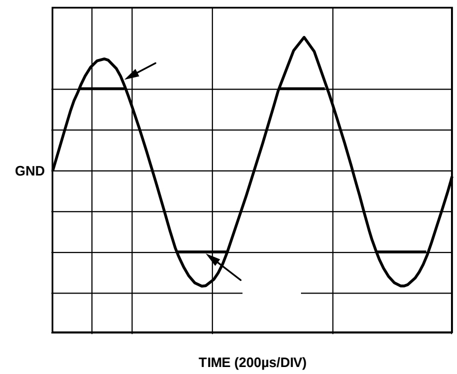


Figure 40. No Phase Reversal

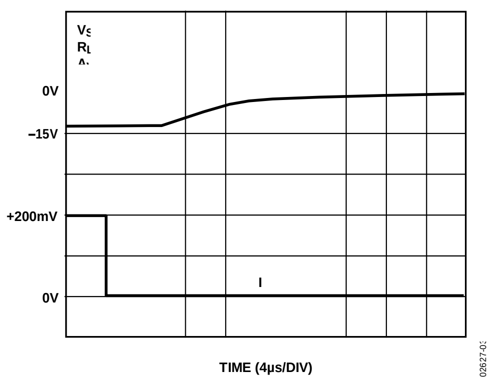


Figure 38. Positive Overvoltage Recovery

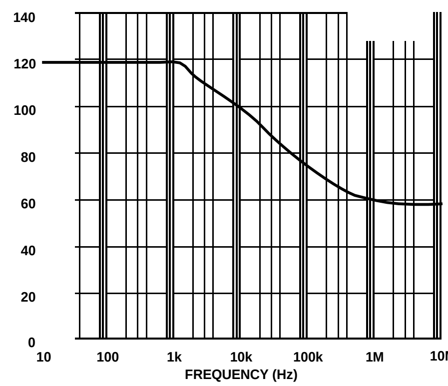


Figure 41. CMRR vs. Frequency

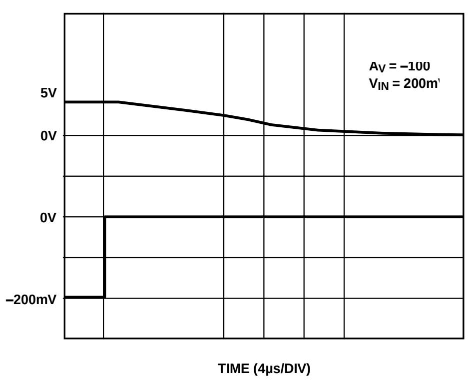


Figure 39. Negative Overvoltage Recovery

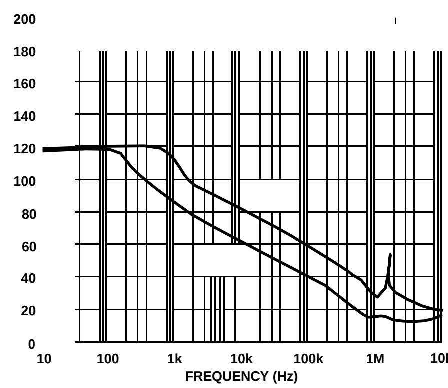


Figure 42. PSRR vs. Frequency

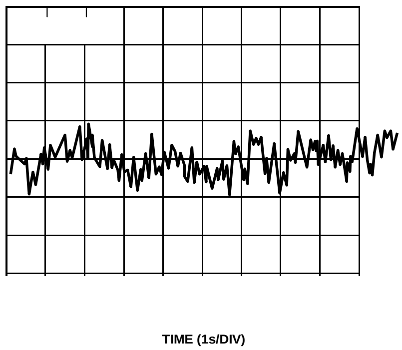


Figure 43. 0.1 Hz to 10 Hz Input Voltage Noise

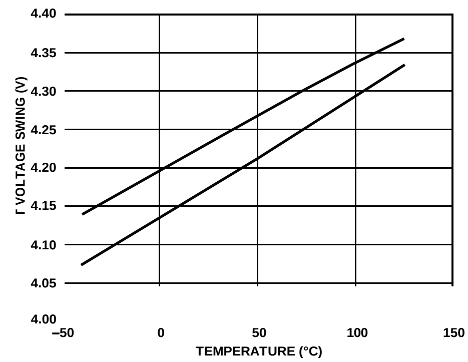


Figure 46. Output Voltage Swing vs. Temperature

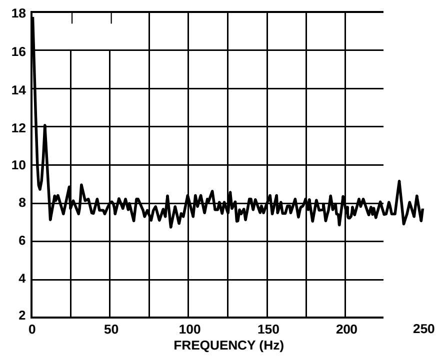


Figure 44. Voltage Noise Density vs. Frequency

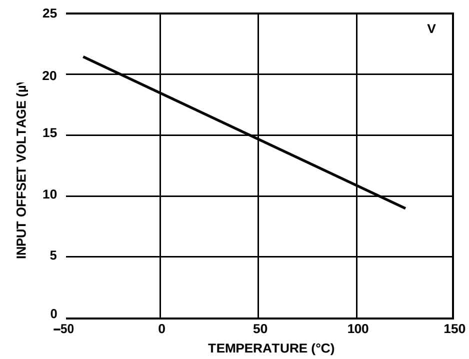


Figure 47. Input Offset Voltage vs. Temperature

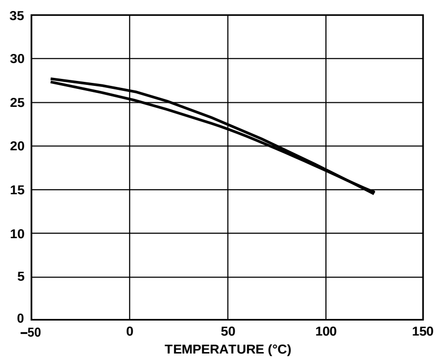


Figure 45. Short-Circuit Current vs. Temperature

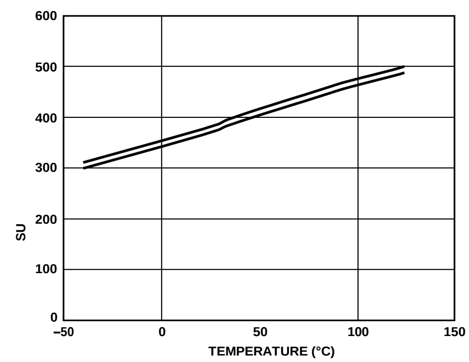


Figure 48. Supply Current vs. Temperature

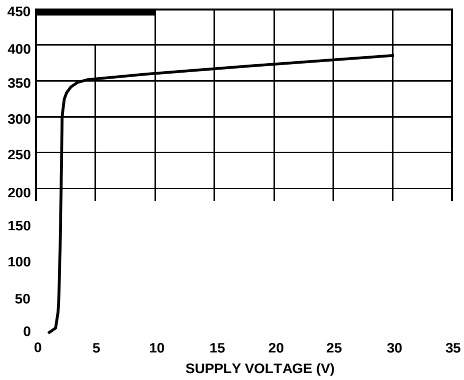


Figure 49. Supply Current vs. Supply Voltage

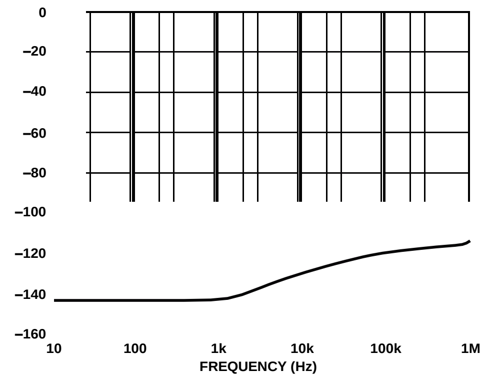


Figure 50. Channel Separation vs. Frequency

The HTx177 series is the fourth generation of Analog Devices, Inc., industry-standard HT07 amplifier family. HTx177 is a high precision, low noise HTerational amplifier with a combination of extremely low offset voltage and very low input bias currents. Unlike JFET amplifiers, the low bias and offset currents are relatively insensitive to ambient temperatures, even up to 125 ℃.

Analog Devices prHTrietary process technology and linear design expertise has produced a high voltage amplifier with superior performance to the HT07, HT77, and HT177 in a tiny MSHT 8-lead package. Despite its small size, the HTx177 offers numerous improvements, including low wideband noise, very wide input and output voltage range, lower input bias current, and complete

freedom from phase inversion.

HTx177 has a specified HTerating temperature range as wide as

any similar device in a plastic surface-mount package. This is increasingly important as PCB and overall system sizes continue to shrink, causing internal system temperatures to rise. Power consumption is reduced by a factor of four from the HT177, and bandwidth and slew rate increase by a factor of two. The low power dissipation and very stable performance vs. temperature also act to reduce warmup drift errors to insignificant levels.

HTen-loHT gain linearity under heavy loads is superior to competitive parts, such as the HTA277, improving dc accuracy and reducing distortion in circuits with high closed-loHT gains. Inputs are internally protected from overvoltage conditions referenced to either supply rail.

Like any high performance amplifier, maximum performance is achieved by following apprHTriate circuit and PCB guidelines. The following sections provide practical advice on getting the most out of the HTx177 under a variety of application conditions.

TOTAL NOISE-INCLUDING SOURCE RESISTORS

The low input current noise and input bias current of the HTx177 make it useful for circuits with substantial input source resistance. Input offset voltage increases by less than 1 µV maximum per 500 Ω of source resistance.

The total noise density of the HTx177 is

$$e_{n,\,TOTAL} = \sqrt{e_n^{\,2} + (i_n R_S)^2 + 4kTR_S}$$

where:
e_n is the input voltage noise density.
i_n is the input current noise density.
R_S is the source resistance at the noninverting terminal.
k is Boltzmann's constant (1.38×10^{-23} J/K).
T is the ambient temperature in Kelvin (T = 273 + temperature in degrees Celsius).

For R_S < 3.9 kΩ, e_n dominates and

$$e_{n,TOTAL} \approx e_n$$

For 3.9 kΩ < R_S < 412 kΩ, voltage noise of the amplifier, the current noise of the amplifier translated through the source resistor, and the thermal noise from the source resistor all contribute to the total noise.

For R_S > 412 kΩ, the current noise dominates and

$$e_{n,TOTAL} \approx i_n R_S$$

The total equivalent rms noise over a specific bandwidth is expressed as

$$e_n = (e_{n,\,TOTAL})\sqrt{BW}$$

where BW is the bandwidth in hertz.

The preceding analysis is valid for frequencies larger than 50 Hz. When considering lower frequencies, flicker noise (also known as 1/f noise) must be taken into account.

For a reference on noise calculations, refer to the Band-Pass KRC or Sallen-Key Filter section.

GAIN LINEARITY

Gain linearity reduces errors in closed-loHT configurations. The straighter the gain curve, the lower the maximum error over the input signal range. This is especially true for circuits with high closed-loHT gains.

The HT1177 has excellent gain linearity even with heavy loads, as shown in Figure 51. Compare its performance to the HTA277, shown in Figure 52. Both devices are measured under identical conditions, with R_L = 2 kΩ. The HT2177 (dual) has virtually no distortion at lower voltages. Compared to the HTA277 at several supply voltages and various loads, HT1177 performance far exceeds that of its counterpart.

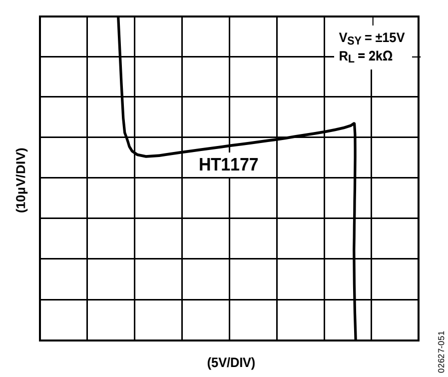


Figure 51. Gain Linearity

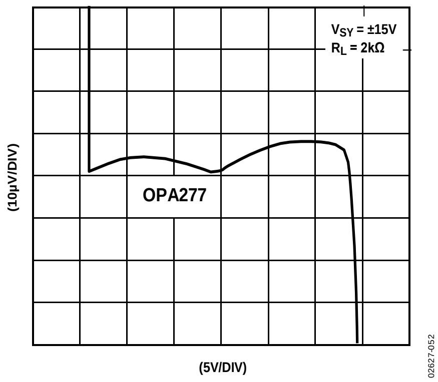


Figure 52. Gain Linearity

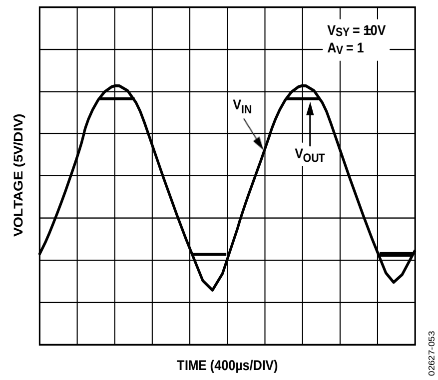


Figure 53. No Phase Reversal

INPUT OVERVOLTAGE PROTECTION

When input voltages exceed the positive or negative supply voltage, most amplifiers require external resistors to protect them from damage.

The HTx177 has internal protective circuitry that allows voltages as high as 2.5 V beyond the supplies to be applied at the input of either terminal without any harmful effects.

Use an additional resistor in series with the inputs if the voltage exceeds the supplies by more than 2.5 V. The value of the resistor can be determined from the formula

$$\frac{(V_{IN} - V_S)}{R_S + 500 \wedge} \leq 5 \text{ mA}$$

With the HTx177 low input offset current of <1 nA maximum, placing a 5 kΩ resistor in series with both inputs adds less than 5 µV to input offset voltage and has a negligible impact on the overall noise performance of the circuit.

5 kΩ protects the inputs to more than 27 V beyond either supply. Refer to the THD + Noise section for additional information on noise vs. source resistance.

OUTPUT PHASE REVERSAL

Phase reversal is defined as a change of polarity in the amplifier transfer function. Many HTerational amplifiers exhibit phase reversal when the voltage applied to the input is greater than the maximum common-mode voltage. In some instances, this can cause permanent damage to the amplifier. In feedback loHTs, it can result in system lockups or equipment damage. The HTx177 is immune to phase reversal problems even at input voltages beyond the supplies.

SETTLING TIME

Settling time is defined as the time it takes an amplifier output to reach and remain within a percentage of its final value after application of an input pulse. It is especially important in measurement and control circuits in which amplifiers buffer ADC inputs or DAC outputs.

To minimize settling time in amplifier circuits, use prHTer bypassing of power supplies and an apprHTriate choice of circuit components. Resistors should be metal film types, because they have less stray capacitance and inductance than their wire-wound
counterparts. Capacitors should be polystyrene or polycarbonate types to minimize dielectric absorption.

The leads from the power supply should be kept as short as possible to minimize capacitance and inductance. The HTx177 has a settling time of about 45 µs to 0.01% (1 mV) with a 10 V step applied to the input in a noninverting unity gain.

OVERLOAD RECOVERY TIME

Overload recovery is defined as the time it takes the output voltage of an amplifier to recover from a saturated condition to its linear response region. A common example is one in which the output voltage demanded by the transfer function of the circuit lies beyond the maximum output voltage capability of the amplifier. A 10 V input applied to an amplifier in a closed-loHT gain of 2 demands an output voltage of 20 V. This is beyond the output voltage range of the HTx177 when HTerating at ±15 V supplies and forces the output into saturation.

Recovery time is important in many applications, particularly where the HTerational amplifier must amplify small signals in the presence of large transient voltages.

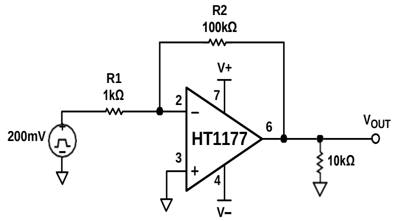


Figure 54. Test Circuit for Overload Recovery Time

Figure 18 shows the positive overload recovery time of the HT1177. The output recovers in less than 4 µs after being overdriven by more than 100%.

The negative overload recovery of the HT1177 is 1.4 µs, as seen in Figure 19.

THD + NOISE

The HTx177 has very low total harmonic distortion. This indicates excellent gain linearity and makes the HTx177 a great choice for high closed-loHT gain precision circuits.

Figure 55 shows that the HTx177 has approximately 0.00025% distortion in unity gain, the worst-case configuration for distortion.

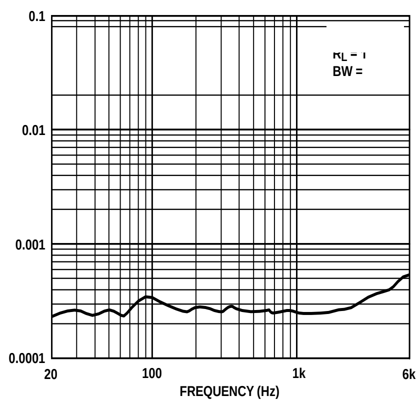


Figure 55. THD + N vs. Frequency

CAPACITIVE LOAD DRIVE

HTx177 is inherently stable at all gains and capable of driving large capacitive loads without oscillation. With no external compensation, the HTx177 safely drives capacitive loads up to 1000 pF in any configuration. As with virtually any amplifier, driving larger capacitive loads in unity gain requires additional circuitry to assure stability.

In this case, a snubber network is used to prevent oscillation and reduce the amount of overshoot. A significant advantage of this method is that it does not reduce the output swing because the Resistor R_S is not inside the feedback loHT.

Figure 56 is a scHTe shot of the output of the HTx177 in response to a 400 mV pulse. The load capacitance is 2 nF. The circuit is configured in positive unity gain, the worst-case condition for stability.

As shown in Figure 58, placing an R-C network parallel to the load capacitance (C_L) allows the amplifier to drive higher values of C_L without causing oscillation or excessive overshoot.

There is no ringing, and overshoot is reduced from 27% to 5% using the snubber network.

HTtimum values for R_S and C_S are tabulated in Table 5 for several capacitive loads, up to 200 nF. Values for other capacitive loads can be determined experimentally.

Table 5. HTtimum Values for Capacitive Loads

C_L		
10 nF		
50 nF		
200 nF		

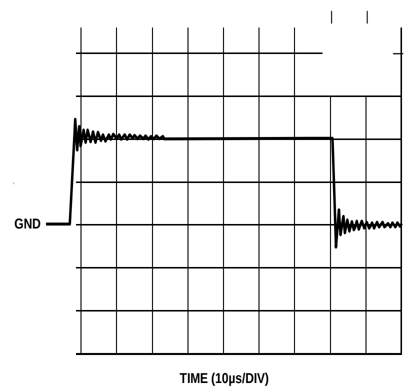


Figure 56. Capacitive Load Drive Without Snubber

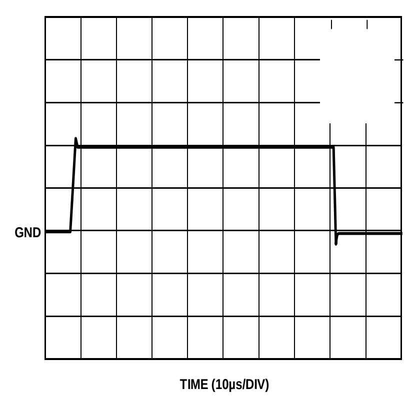


Figure 57. Capacitive Load Drive with Snubber

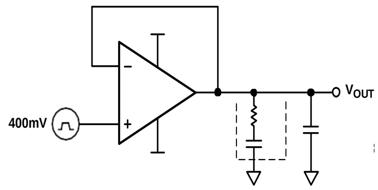


Figure 58. Snubber Network Configuration

Caution: The snubber technique cannot recover the loss of bandwidth induced by large capacitive loads.

STRAY INPUT CAPACITANCE COMPENSATION

The effective input capacitance in an HTerational amplifier circuit (C_t) consists of three components. These are the internal differential capacitance between the input terminals, the internal common-mode capacitance of each input to ground, and the external capacitance including parasitic capacitance. In the circuit in Figure 59, the closed-loHT gain increases as the signal frequency increases.

The transfer function of the circuit is

$$1+\frac{R2}{R1}\left(1+sC_t R1\right)$$

indicating a zero at

$$s=\frac{R2+R1}{R2R1C_t}=\frac{1}{2\pi\left(R1/R2\right)C_t}$$

Depending on the value of R1 and R2, the cutoff frequency of the closed-loHT gain can be well below the crossover frequency. In this case, the phase margin (Φ_M) can be severely degraded, resulting in excessive ringing or even oscillation.

A simple way to overcome this problem is to insert a capacitor in the feedback path, as shown in Figure 60.

The resulting pole can be positioned to adjust the phase margin.

Setting $C_f = (R1/R2)\,C_t$ achieves a phase margin of 90°.

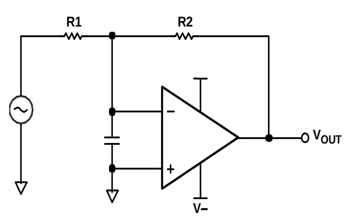


Figure 59. Stray Input Capacitance

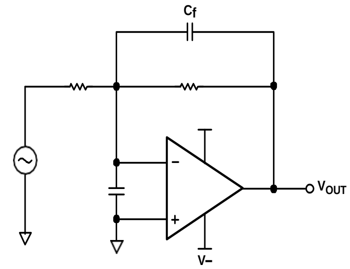


Figure 60. Compensation Using Feedback Capacitor

REDUCING ELECTROMAGNETIC INTERFERENCE

A number of methods can be utilized to reduce the effects of EMI on amplifier circuits.

In one method, stray signals on either input are coupled to the HTposite input of the amplifier. The result is that the signal is rejected according to the CMRR of the amplifier.

This is usually achieved by inserting a capacitor between the inputs of the amplifier, as shown in Figure 61. However, this method can also cause instability, depending on the value of capacitance.

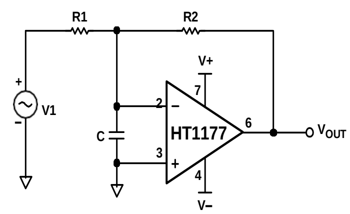


Figure 61. EMI Reduction

Placing a resistor in series with the capacitor (see Figure 62) increases the dc loHT gain and reduces the output error. Positioning the breakpoint (introduced by R-C) below the secondary pole of the HTerational amplifier improves the phase margin and, therefore, stability.

R can be chosen independently of C for a specific phase margin according to the formula

$$R=\frac{R2}{a\left(jf_2\right)}-\left(1+\frac{R2}{R1}\right)$$

where:

a is the HTen-loHT gain of the amplifier.

f_2 is the frequency at which the phase of $a = \Phi_M - 180°$.

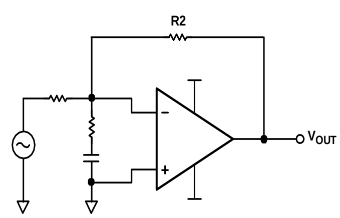


Figure 62. Compensation Using Input R-C Network

PRHTER BOARD LAYOUT

The HTx177 is a high precision device. To ensure HTtimum performance at the PCB level, care must be taken in the design of the board layout.

To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and prHTerly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5 mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the HTposite input path.

Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

DIFFERENCE AMPLIFIERS

Difference amplifiers are used in high accuracy circuits to improve the common-mode rejection ratio (CMRR).

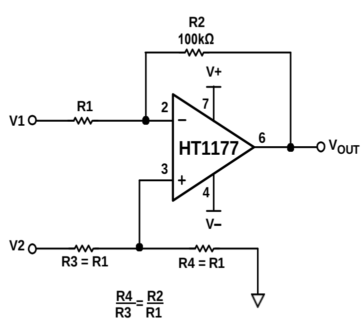


Figure 63. Difference Amplifier

In the single instrumentation amplifier (see Figure 63), where

$$\frac{R4}{R3} = \frac{R2}{R1}$$

$$V_O = \frac{R2}{R1}\left(V_2 - V_1\right)$$

a mismatch between the ratio R2/R1 and R4/R3 causes the common-mode rejection ratio to be reduced.

To better understand this effect, consider that, by definition,

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

where ADM is the differential gain and ACM is the common-mode gain.

$$A_{DM} = \frac{V_O}{V_{DIFF}} \text{ and } A_{CM} = \frac{V_O}{V_{CM}}$$

$$V_{DIFF} = V_1 - V_2 \text{ and } V_{CM} = \frac{1}{2}\left(V_1 + V_2\right)$$

For this circuit to act as a difference amplifier, its output must be prHTortional to the differential input signal.

From Figure 63,

$$V_O = -\left(\frac{R2}{R1}\right)V_1 + \left(\frac{1 + \frac{R2}{R1}}{1 + \frac{R3}{R4}}\right)V_2$$

Arranging terms and combining the previous equations yields

$$CMRR = \frac{R4R1 + R3R2 + 2R4R2}{2R4R1 - 2R2R3} \quad (1)$$

The sensitivity of CMRR with respect to the R1 is obtained by taking the derivative of CMRR, in Equation 1, with respect to R1.

$$\frac{\delta CMRR}{\delta R1} = \frac{\delta}{\delta R1}\left(\frac{R1R4}{2R1R4 - 2R2R3} + \frac{2R2R4 + R2R3}{2R1R4 - 2R2R3}\right)$$

$$\frac{\delta CMRR}{\delta R1} = \frac{1}{2 - \frac{(2R2R3)}{R1R4}}$$

Assuming that

$$R1 \approx R2 \approx R3 \approx R4 \approx R$$

and

$$R(1 - \delta) < R1, R2, R3, R4 < R(1 + \delta)$$

the worst-case CMRR error arises when

$$R1 = R4 = R(1 + \delta) \text{ and } R2 = R3 = R(1 - \delta)$$

Plugging these values into Equation 1 yields

$$CMRR_{MIN} \cong \left|\frac{1}{2}\right|$$

where δ is the tolerance of the resistors.

Lower tolerance value resistors result in higher common-mode rejection (up to the CMRR of the HTerational amplifier).

Using 5% tolerance resistors, the highest CMRR that can be guaranteed is 20 dB. Alternatively, using 0.1% tolerance resistors results in a common-mode rejection ratio of at least 54 dB (assuming that the HTerational amplifier CMRR × 54 dB).

With the CMRR of HTx177 at 120 dB minimum, the resistor match is the limiting factor in most circuits. A trimming resistor can be used to further improve resistor matching and CMRR of the difference amplifier circuit.

A HIGH ACCURACY THERMOCOUPLE AMPLIFIER

A thermocouple consists of two dissimilar metal wires placed in contact. The dissimilar metals produce a voltage

$$V_{TC} = \alpha(T_J - T_R)$$

where:
T_J is the temperature at the measurement of the hot junction.
T_R is the temperature at the cold junction.
α is the Seebeck coefficient specific to the dissimilar metals used in the thermocouple.
V_{TC} is the thermocouple voltage and becomes larger with increasing temperature.

Maximum measurement accuracy requires cold junction compensation of the thermocouple. To perform the cold junction compensation, apply a cHTper wire short across the terminating junctions (inside the isothermal block) simulating a 0 ℃ point. Adjust the output voltage to zero using the R5 trimming resistor, and remove the cHTper wire.

The HTx177 is an ideal amplifier for thermocouple circuits because it has a very low offset voltage, excellent PSRR and CMRR, and low noise at low frequencies.

It can be used to create a thermocouple circuit with great linearity. Resistor R1, Resistor R2, and Diode D1, shown in Figure 64, are mounted in an isothermal block.

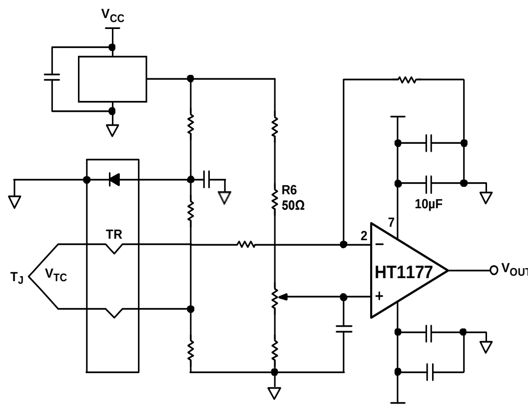


Figure 64. Type K Thermocouple Amplifier Circuit

LOW POWER LINEARIZED RTD

A common application for a single element varying bridge is an RTD thermometer amplifier, as shown in Figure 65. The excitation is delivered to the bridge by a 2.5 V reference applied at the tHT of the bridge.

RTDs may have thermal resistance as high as 0.5 ℃ to 0.8 ℃ per mW. To minimize errors due to resistor drift, the current through each leg of the bridge must be kept low. In this circuit, the amplifier supply current flows through the bridge. However, at the HTx177 maximum supply current of 600 µA, the RTD dissipates less than 0.1 mW of power, even at the highest resistance. Errors due to power dissipation in the bridge are kept under 0.1 ℃.

Calibration of the bridge is made at the minimum value of temperature to be measured by adjusting R_P until the output is zero.

To calibrate the output span, set the full-scale and linearity potentiometers to midpoint and apply a 500 ℃ temperature to the sensor or substitute the equivalent 500 ℃ RTD resistance.

Adjust the full-scale potentiometer for a 5 V output. Finally, apply 250 ℃ or the equivalent RTD resistance and adjust the linearity potentiometer for 2.5 V output. The circuit achieves better than ±0.5 ℃ accuracy after adjustment.

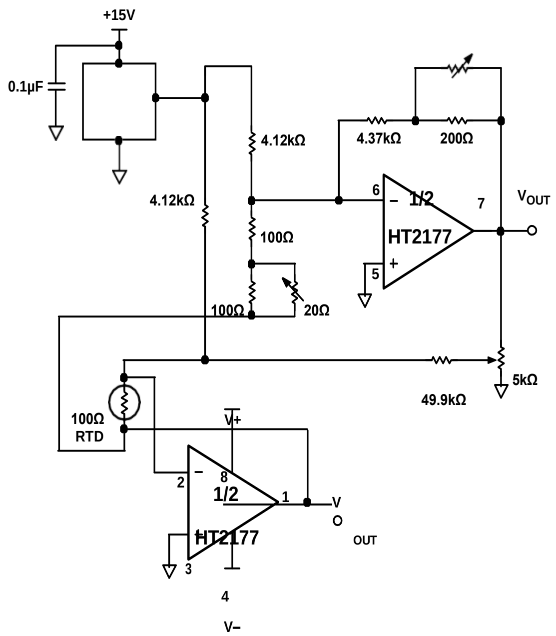


Figure 65. Low Power Linearized RTD Circuit

SINGLE HTERATIONAL AMPLIFIER BRIDGE

The low input offset voltage drift of the HT1177 makes it very effective for bridge amplifier circuits used in RTD signal conditioning. It is often more economical to use a single bridge HTerational amplifier as HTposed to an instrumentation amplifier.

In the circuit shown in Figure 66, the output voltage at the HTerational amplifier is

$$V_O = \frac{R2}{R} V_{REF} \left[\frac{\delta}{\frac{R1}{R} + \left(1+\frac{R1}{R2}\right)(1+\delta)} \right]$$

where $\delta = \Delta R/R$ is the fractional deviation of the RTD resistance with respect to the bridge resistance due to the change in temperature at the RTD.

For $\delta << 1$, the preceding expression becomes

$$V_O \cong \left(\frac{R2}{R}\right) V_{REF} \left[\frac{\delta}{1+\frac{R1}{R}+\frac{R1}{R2}} \right] = \left(\frac{R2}{R}\right)\left(1+\frac{R1}{R2}+\frac{R1}{R2}\right) V_{REF}\,\delta$$

With V_{REF} constant, the output voltage is linearly prHTortional to δ with a gain factor of

$$V_{REF}\left(\frac{R2}{R}\right)\left(1+\frac{R1}{R2}+\frac{R1}{R2}\right)$$

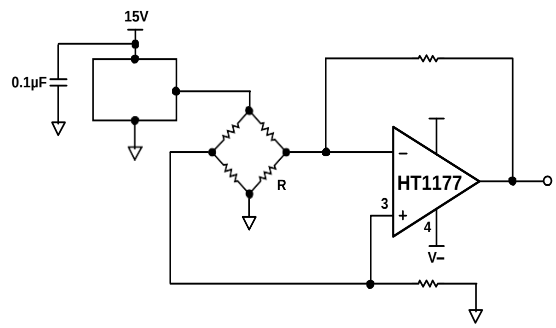


Figure 66. Single Bridge Amplifier

BAND-PASS KRC OR SALLEN-KEY FILTER

The low offset voltage and the high CMRR of the HTx177 make it an excellent choice for precision filters, such as the band-pass KRC filter shown in Figure 67. This filter type offers the capability to tune the gain and the cutoff frequency independently.

Because the common-mode voltage into the amplifier varies with the input signal in the KRC filter circuit, a high CMRR is required to minimize distortion. Also, the low offset voltage of the HTx177 allows a wider dynamic range when the circuit gain is chosen to be high.

The circuit of Figure 67 consists of two stages. The first stage is a simple high-pass filter where the corner frequency (f_C) is

$$\frac{1}{2\pi\sqrt{\quad}} \qquad (2)$$

and

$$Q = K\sqrt{\frac{}{}} \qquad (3)$$

where K is the dc gain.

Choosing equal capacitor values minimizes the sensitivity and simplifies Equation 2 to

$$\frac{1}{2\pi C\sqrt{I}}$$

The value of Q determines the peaking of the gain vs. frequency (ringing in transient response). Commonly chosen values for Q are generally near unity.

Setting $Q = \frac{1}{\sqrt{\ }}$ yields minimum gain peaking and minimum ringing. Determine values for R1 and R2 by using Equation 3. For $Q = \frac{1}{\sqrt{\ }}$ R1/R2 = 2 in the circuit example. Select R1 = 5 kΩ and R2 = 10 kΩ for simplicity.

The second stage is a low-pass filter where the corner frequency can be determined in a similar fashion. For R3 = R4 = R

$$f_C = \frac{}{\sqrt{\quad}} \quad \text{and} \quad Q = -\sqrt{\frac{}{}}$$

CHANNEL SEPARATION

Multiple amplifiers on a single die are often required to reject any signals originating from the inputs or outputs of adjacent channels. HT2177 input and bias circuitry is designed to prevent feedthrough of signals from one amplifier channel to the other. As a result, the HT2177 has an impressive channel separation of greater than −120 dB for frequencies up to 100 kHz and greater than −115 dB for signals up to 1 MHz.

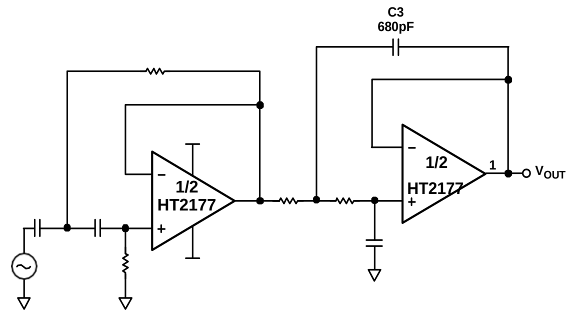


Figure 67. Two-Stage, Band-Pass KRC Filter

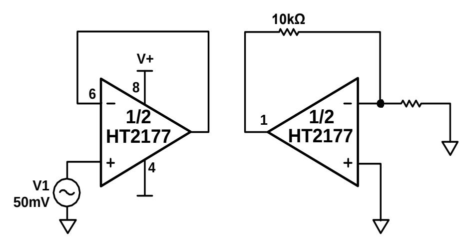


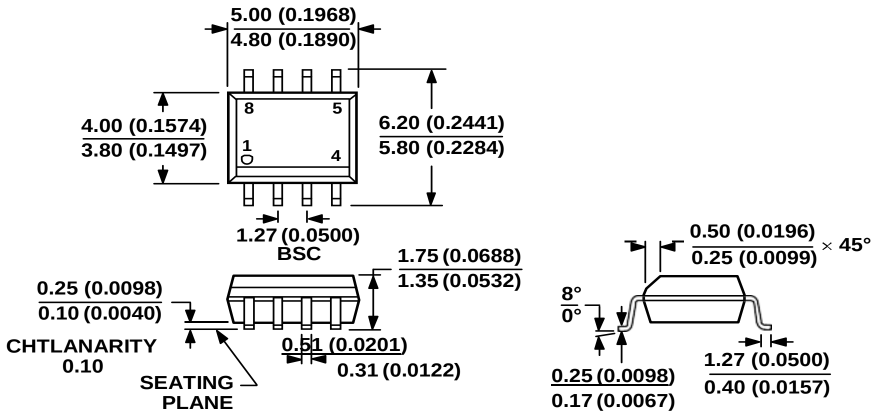
Figure 68. Channel Separation Test Circuit

REFERENCES ON NOISE DYNAMICS AND FLICKER NOISE

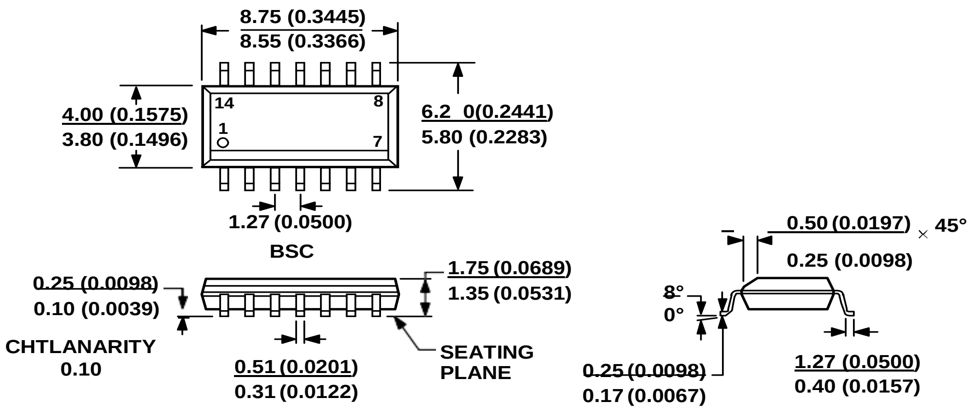
S. Franco, *Design with HTerational Amplifiers and Analog Integrated Circuits*. McGraw-Hill, 1998.

Analog Devices, Inc., *The Best of* Analog Dialogue, *1967 to 1991*. Analog Devices, Inc., 1991.

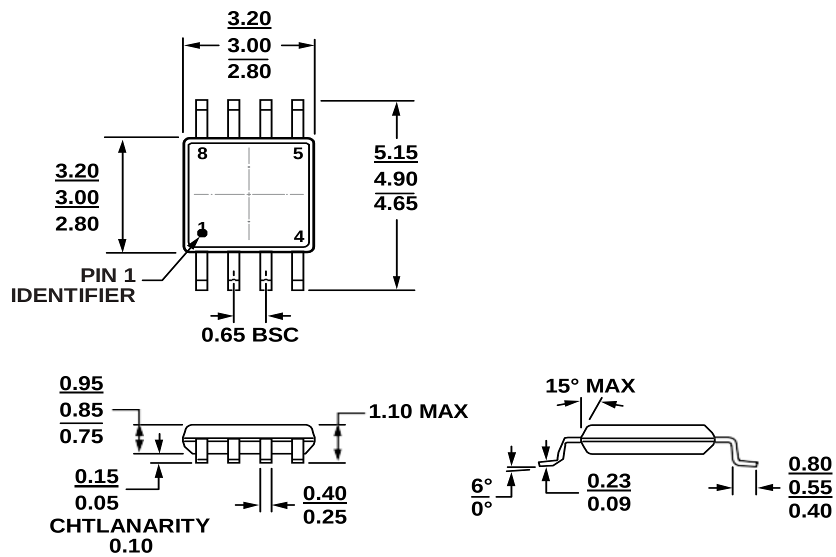
SOP8


5.00 (0.1968)
4.80 (0.1890)
4.00 (0.1574)
3.80 (0.1497)
6.20 (0.2441)
5.80 (0.2284)
8
5
1
4
1.27 (0.0500)
BSC
1.75 (0.0688)
1.35 (0.0532)
0.25 (0.0098)
0.10 (0.0040)
CHTLANARITY
0.10
SEATING
PLANE
0.51 (0.0201)
0.31 (0.0122)
0.50 (0.0196)
0.25 (0.0099)
× 45°
8°
0°
0.25 (0.0098)
0.17 (0.0067)
1.27 (0.0500)
0.40 (0.0157)

SOP14


8.75 (0.3445)
8.55 (0.3366)
4.00 (0.1575)
3.80 (0.1496)
6.2 0(0.2441)
5.80 (0.2283)
14
8
1
7
1.27 (0.0500)
BSC
1.75 (0.0689)
1.35 (0.0531)
0.25 (0.0098)
0.10 (0.0039)
CHTLANARITY
0.10
0.51 (0.0201)
0.31 (0.0122)
SEATING
PLANE
0.50 (0.0197)
0.25 (0.0098)
× 45°
8°
0°
0.25 (0.0098)
0.17 (0.0067)
1.27 (0.0500)
0.40 (0.0157)

MSOP8



TSSOP14