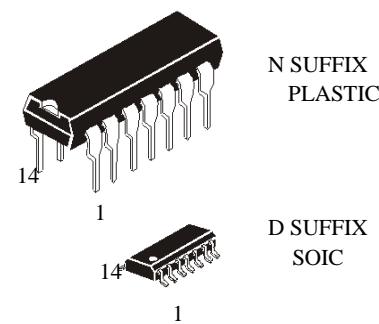




Low Power Quad Operational Amplifier

The HT324A contains four independent high gain operational amplifiers with internal frequency compensation. The op-amps operate over a wide voltage range. The device has low power supply current drain, regardless of the power supply voltage. The low power drain makes the HT324A a good choice for battery operation.

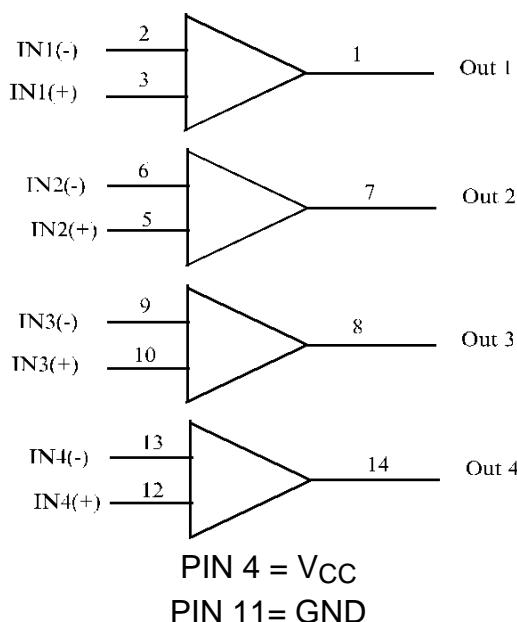
- Internally frequency compensated for unity gain
- Large DC voltage gain
- Single or split supply operation
- Input common-mode voltage range to ground
- Large output voltage swing: 0V DC to V_{CC}-1.5V DC
- Power drain suitable for battery operation
- Low input offset voltage and offset current
- Differential input voltage range equal to the power supply voltage



ORDERING INFORMATION

HT324AN	Plastic
HT324AR	SOIC
HT324AG	Chip

BLOCK DIAGRAM



PIN ASSIGNMENT

OUT 1	1	OUT 4	14
IN1(-)	2	IN4(-)	13
IN1(+)	3	IN4(+)	12
CC	4	GND	11
IN2 (+)	5	IN3(+)	10
IN2 (-)	6	IN3(-)	9
OUT 2	7	OUT 3	8

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltages Single Supply Split Supplies	32 ± 16	V
V_{IDR}	Input Differential Voltage Range (1)	± 32	V
V_{ICR}	Input Common Mode Voltage Range	-0.3 to 32	V
t_s	Short-Circuit duration of Output	100	ms
T_J	Junction Temperature Plastic Packages	150	°C
T_{STG}	Storage Temperature Plastic Packages	-55 to +125	°C
I_{IN}	Input Current, per pin (2)	50	mA
T_L	Lead Temperature, 1mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
 Functional operation should be restricted to the Recommended Operating Conditions.

Notes:

1. Split Power Supplies.
2. $V_{IN} < -0.3V$.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	± 2.5 or 5.0	± 15 or 30	V
T_A	Operating Temperature, All Package Types	0	+70	°C

DC ELECTRICAL CHARACTERISTICS (T_A=0 to +70°C)

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
V _{IO}	Maximum Input Offset Voltage	V _{CC} =5.0-30V; R _S =0Ω V _O =1.4V V _{ICR} =0V - (V _{CC} -1.5V)* V _{ICR} =0V - (V _{CC} -2.0V)		7.0* 9.0	mV
I _{IO}	Maximum Input Offset Current	V _{CC} =5.0-30V, V _O =1.4V		±50* ±150	nA
I _{IB}	Maximum Input Bias Current	V _{CC} =5.0-30V, V _O =1.4V		-250* -500	nA
V _{ICR}	Input Common Mode Voltage Range	V _{CC} =30V	0	V _{CC} -1.5V V _{CC} -2.0V	V
I _{CC}	Maximum Power Supply Current	R _L =∞,V _{CC} =5V, V _O =2.5V R _L =∞,V _{CC} =30V, V _O =15V		1.2 3.0	mA
A _{VOL}	Minimum Large Signal Open-Loop Voltage Gain	V _{CC} =15V, R _L ≥2KΩ	25* 15		V/mV
V _{OH}	Minimum Output High-Level Voltage Swing	V _{CC} =5V,R _L =2KΩ V _{CC} =30V,R _L =2KΩ V _{CC} =30V,R _L =10KΩ	3.3 26 27		V
V _{OL}	Maximum Output Low-Level Voltage Swing	V _{CC} =5V,R _L =10KΩ		20	mV
CMR	Common Mode Rejection	Ω V _{CC} =5-30V, R _S =10K	65*		dB
PSR	Power Supply Rejection	V _{CC} =5-30V	65*		dB
I _{SC}	Maximum Output Short Circuit to GND	V _{CC} =5.0V, V _O =0V		60*	mA
I _{O+}	Minimum Output Source Current	V _{CC} =15V, V _{ID} =-1.0V,	20*		mA
I _{O-}	Minimum Output Sink Current	V _{ID} =-1.0V, V _{CC} =15V, V _O =15V V _{ID} =-1.0V, V _{CC} =15V, V _O =0.2V	10* 5 12*		mA μA
V _{IDR}	Differential Input Voltage Range (if used)	All V _{IN} ≥GND or V-Supply		V _{CC} *	V

 * T_A = +25°C

NOTE: Guaranteed Limits of DC Electrical Characteristics are given for T_A=0, +70°C as the information for chips.

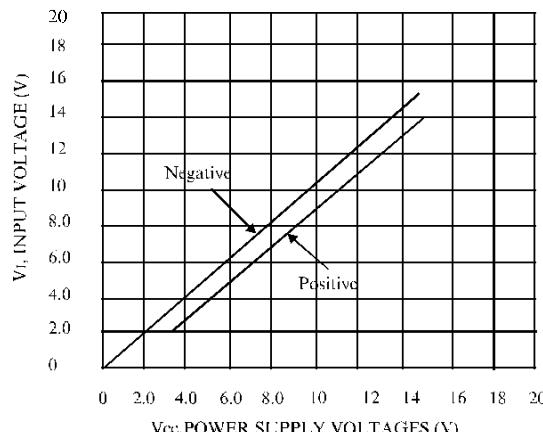
TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$)

Figure 1. Input Voltage Range

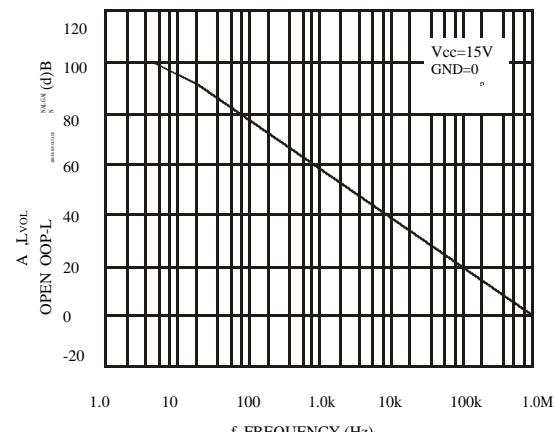


Figure 2. Open-Loop Frequency

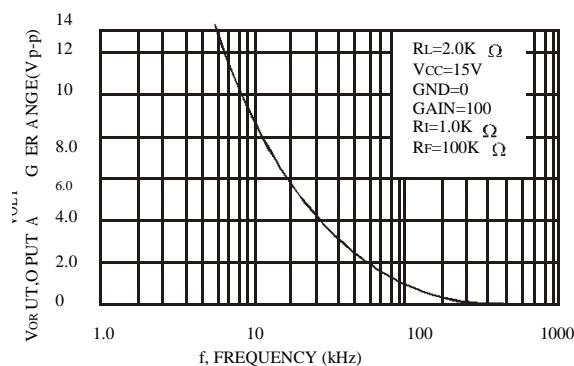


Figure 3. Large-Signal Frequency Response

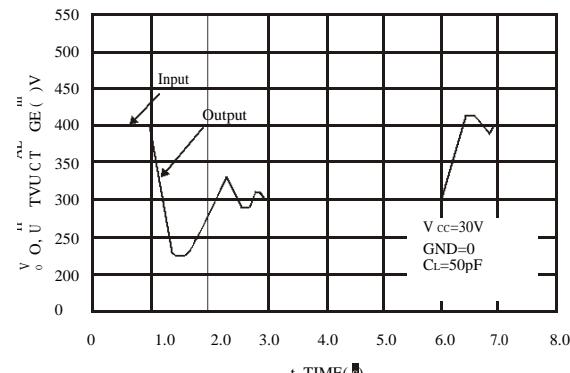


Figure 4. Small-Signal Voltage Follower Pulse Response (Noninverting)

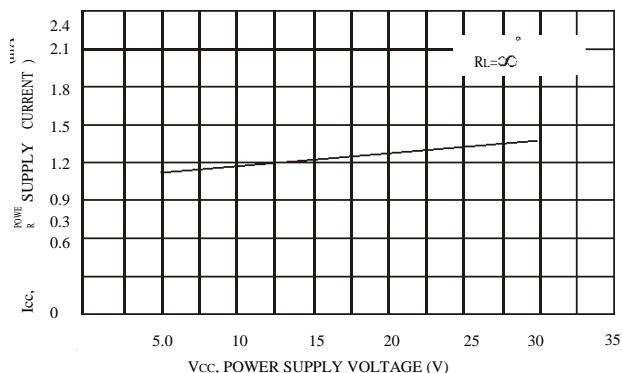


Figure 5. Power Supply Current versus Power Supply Voltage

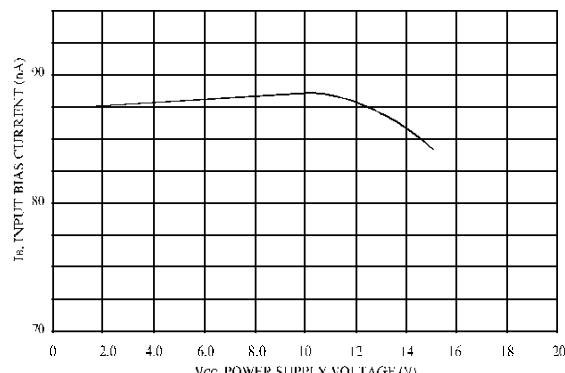
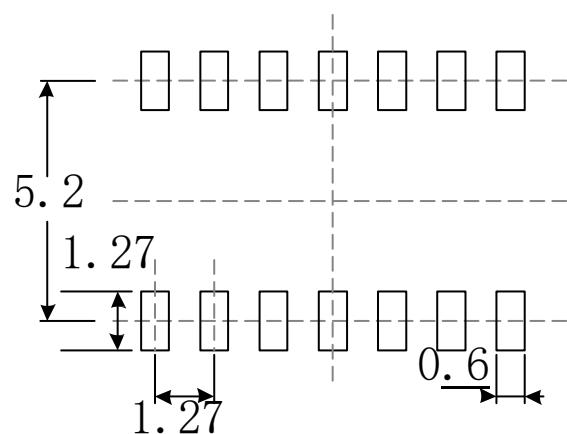
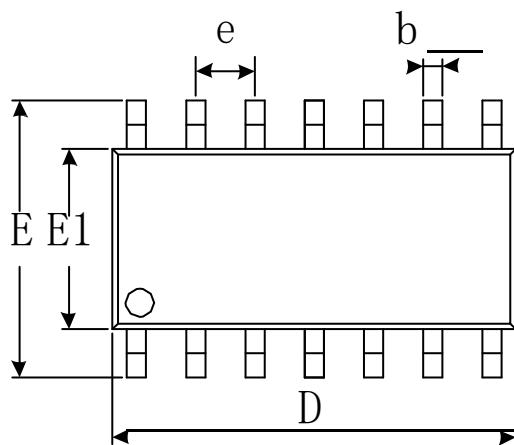


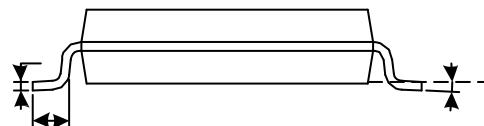
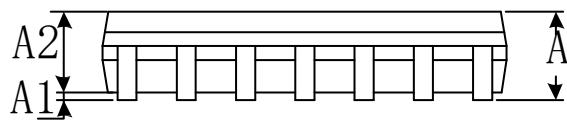
Figure 6. Input Bias Current versus Power Supply Voltage



SOP-14



RECOMMENDED LAND PATTERN (Unit: mm)

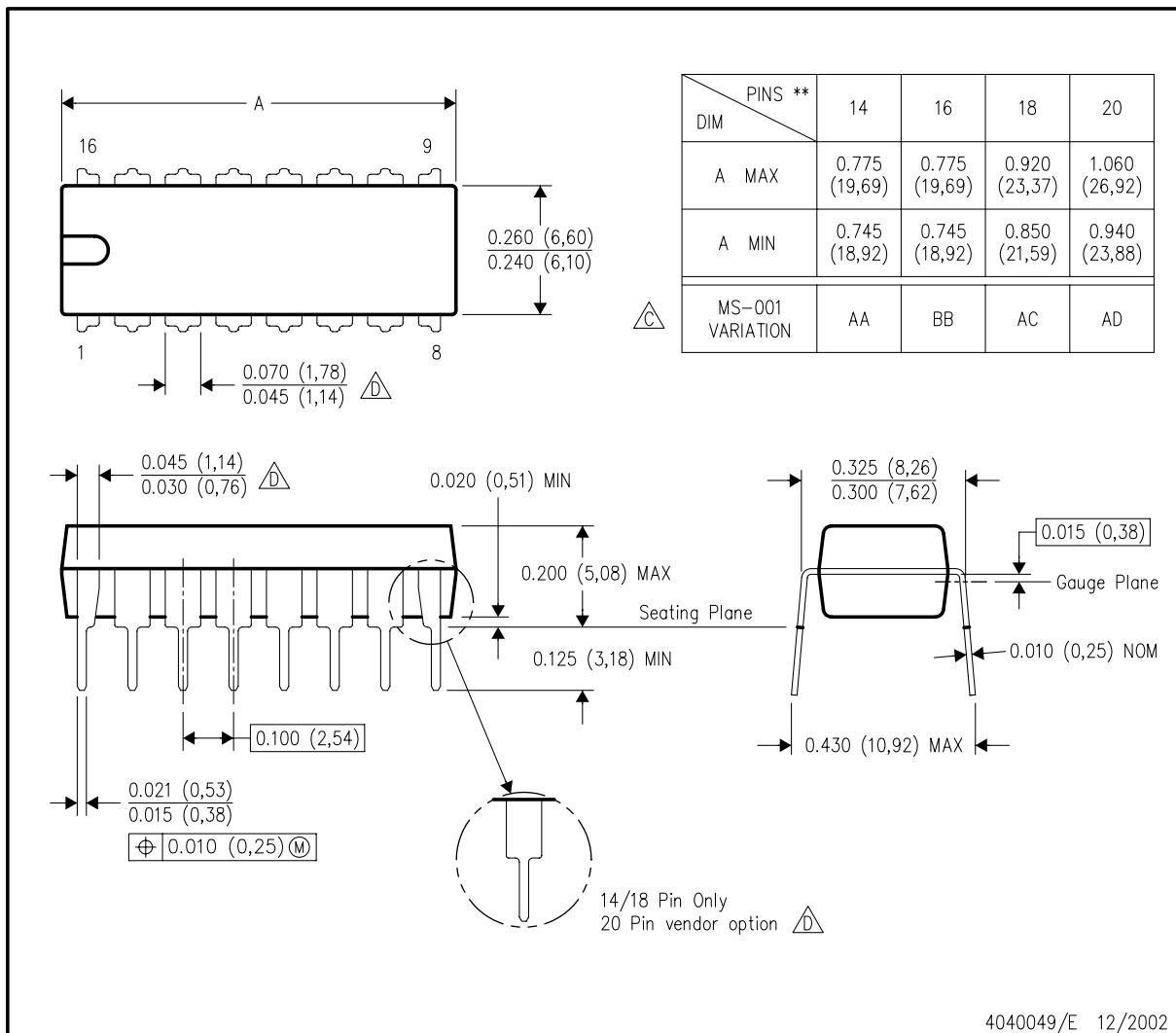


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
e	1.270(BSC)		0.050(BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



DIP-14

16 PINS SHOWN



- NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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[TLV2455IDR](#) [TLV2461IDR](#)