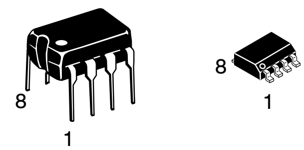
Single Supply 3.0 V to 36V Operational Amplifiers

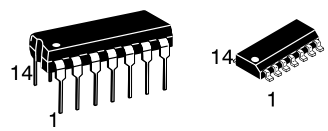
Quality bipolar fabrication with innovative design concepts are employed for the HT33071/72/74, HT34071/72/74, A series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, 13 V/ms slew rate and fast settling time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With a Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The HT33071/72/74, HT34071/72/74, ,A series of devices are available in standard or prime performance (A Suffix) grades and are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic DIP, SOIC, QFN and TSSOP surface mount packages.

DUAL



QUAD



ORDERING INFORMATION

HT34072ANZ DIP8

HT34072ARZ SOP8

HT34074ANZ DIP14

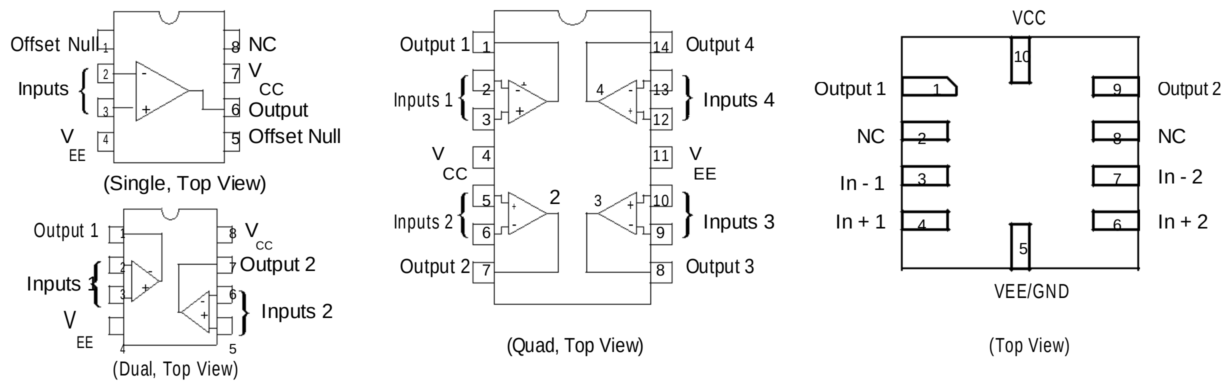
HT34074ARZ SOP14

T_A = 0° to 70°C for all packages.

Features

- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/ms
- Fast Settling Time: 1.1 ms to 0.1%
- Wide Single Supply Operation: 3.0 V to 36 V
- Wide Input Common Mode Voltage Range: Includes Ground (V_{EE})
- Low Input Offset Voltage: 3.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: −14.7 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 10,000 pF
- Low Total Harmonic Distortion: 0.02%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 12 dB
- Output Short Circuit Protection
- ESD Diodes/Clamps Provide Input Protection for Dual and Quad
- HTV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

CASE 626/CASE 751	CASE 646/CASE 751A/CASE 948G	CASE 510AJ



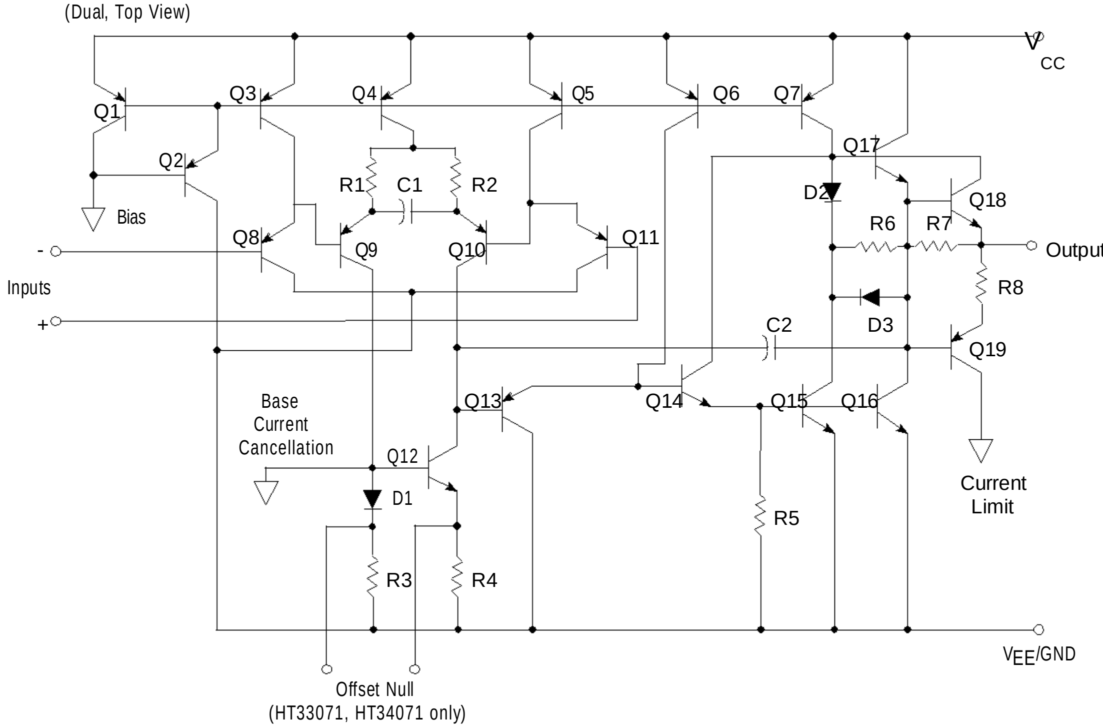


Figure 1. Representative Schematic Diagram

(Each Amplifier)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{EE} to V_{CC})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	Sec
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
ESD Capability, Dual and Quad (Note 3) Human Body Model Machine Model	 ESD_{HBM} ESD_{MM}	 2000 200	V

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground, unless otherwise noted. See Note 4 for $T_A = T_{low}$ to T_{high})

Characteristics	Symbol	A Suffix Min	A Suffix Typ	A Suffix Max	Non−Suffix Min	Non−Suffix Typ	Non−Suffix Max	Unit
Input Offset Voltage (R_S = 100 W, V_{CM} = 0 V, V_O = 0 V) V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, $T_A = T_{low}$ to T_{high}	V_{IO}	 – – –	 0.5 0.5 –	 3.0 3.0 5.0	 – – –	 1.0 1.5 –	 5.0 5.0 7.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 W, V_{CM} = 0 V, V_O = 0 V, $T_A = T_{low}$ to T_{high}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	mV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C $T_A = T_{low}$ to T_{high}	I_{IB}	 – –	 100 –	 500 700	 – –	 100 –	 500 700	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0V) T_A = +25°C $T_A = T_{low}$ to T_{high}	I_{IO}	 – –	 6.0 –	 50 300	 – –	 6.0 –	 75 300	nA
Input Common Mode Voltage Range T_A = +25°C $T_A = T_{low}$ to T_{high}	V_{ICR}		 V_{EE} to (V_{CC} −1.8) V_{EE} to (V_{CC} −2.2)			 V_{EE} to (V_{CC} −1.8) V_{EE} to (V_{CC} −2.2)		V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kW) T_A = +25°C $T_A = T_{low}$ to T_{high}	A_{VOL}	 50 25	 100 –	 – –	 25 20	 100 –	 – –	V/mV
Output Voltage Swing (V_{ID} = ±1.0 V) V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kW, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kW, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kW, $T_A = T_{low}$ to T_{high}	V_{OH}	 3.7 13.6 13.4	 4.0 14 –	 – – –	 3.7 13.6 13.4	 4.0 14 –	 – – –	V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kW, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kW, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kW, $T_A = T_{low}$ to T_{high}	V_{OL}	– – –	0.1 −14.7 –	0.3 −14.3 −13.5	– – –	0.1 −14.7 –	0.3 −14.3 −13.5	V
Output Short Circuit Current (V_{ID} = 1.0 V, V_O = 0 V, T_A = 25°C) Source Sink	I_{SC}	 10 20	 30 30	 – –	 10 20	 30 30	 – –	mA
Common Mode Rejection R_S ≤ 10 kW, V_{CM} = V_{ICR}, T_A = 25°C	CMR	80	97	–	70	97	–	dB
Power Supply Rejection (R_S = 100 W) V_{CC}/V_{EE} = +16.5 V/−16.5 V to +13.5 V/−13.5 V, T_A = 25°C	PSR	80	97	–	70	97	–	dB
Power Supply Current (Per Amplifier, No Load) V_{CC} = +5.0 V, V_{EE} = 0 V, V_O = +2.5 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, $T_A = T_{low}$ to T_{high}	I_D	 – – –	 1.6 1.9 –	 2.0 2.5 2.8	 – – –	 1.6 1.9 –	 2.0 2.5 2.8	mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground. T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	A Suffix			Non−Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kW, C_L = 500 pF)	SR							V/ms
A_V = +1.0		8.0	10	−	8.0	10	−	
A_V = −1.0		−	13	−	−	13	−	
Setting Time (10 V Step, A_V = −1.0)	t_s							ms
To 0.1% (+1/2 LSB of 9−Bits)		−	1.1	−	−	1.1	−	
To 0.01% (+1/2 LSB of 12−Bits)		−	2.2	−	−	2.2	−	
Gain Bandwidth Product (f = 100 kHz)	GBW	3.5	4.5	−	3.5	4.5	−	MHz
Power Bandwidth A_V = +1.0, R_L = 2.0 kW, V_O = 20 V_{pp}, THD = 5.0%	BW	−	160	−	−	160	−	kHz
Phase margin	f_m							Deg
R_L = 2.0 kW		−	60	−	−	60	−	
R_L = 2.0 kW, C_L = 300 pF		−	40	−	−	40	−	
Gain Margin	A_m							dB
R_L = 2.0 kW		−	12	−	−	12	−	
R_L = 2.0 kW, C_L = 300 pF		−	4.0	−	−	4.0	−	
Equivalent Input Noise Voltage R_S = 100 W, f = 1.0 kHz	e_n	−	32	−	−	32	−	nV/ √Hz
Equivalent Input Noise Current f = 1.0 kHz	i_n	−	0.22	−	−	0.22	−	pA/ √Hz
Differential Input Resistance V_{CM} = 0 V	R_{in}	−	150	−	−	150	−	MW
Differential Input Capacitance V_{CM} = 0 V	C_{in}	−	2.5	−	−	2.5	−	pF
Total Harmonic Distortion A_V = +10, R_L = 2.0 kW, 2.0 V_{pp} ≤ V_O ≤ 20 V_{pp}, f = 10 kHz	THD	−	0.02	−	−	0.02	−	%
Channel Separation (f = 10 kHz)	−	−	120	−	−	120	−	dB
Open Loop Output Impedance (f = 1.0 MHz)	$\|Z_O\|$	−	30	−	−	30	−	W

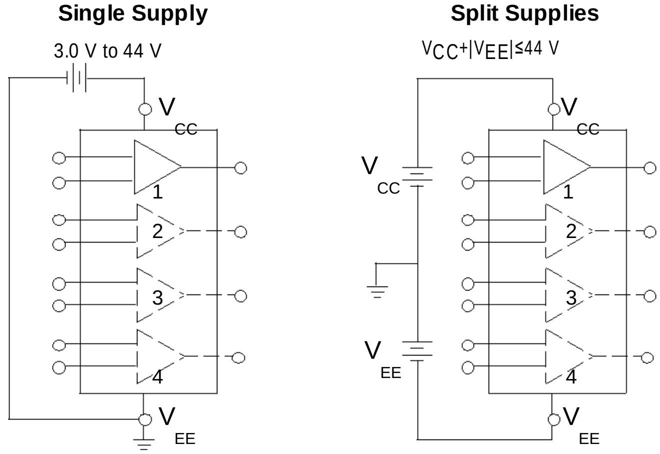
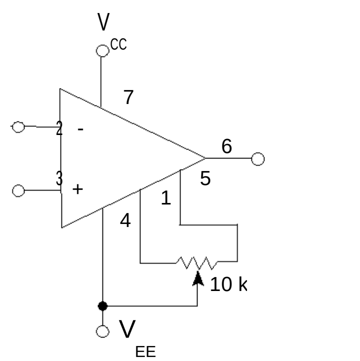


Figure 2. Power Supply Configurations



Offset nulling range is approximately ± 80 mV with a 10 k potentiometer (HT33071, HT34071 only).

Figure 3. Offset Null Circuit

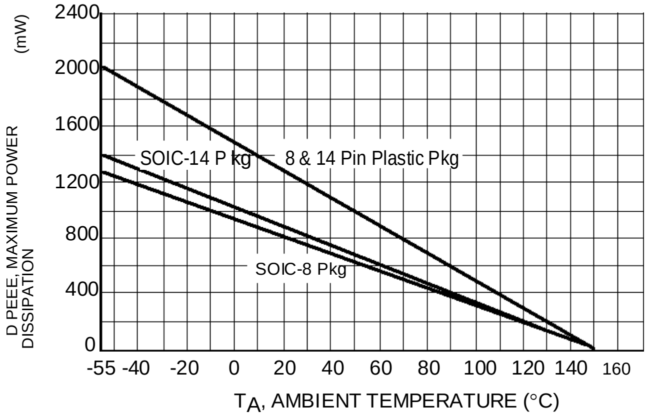


Figure 4. Maximum Power Dissipation versus Temperature for Package Types

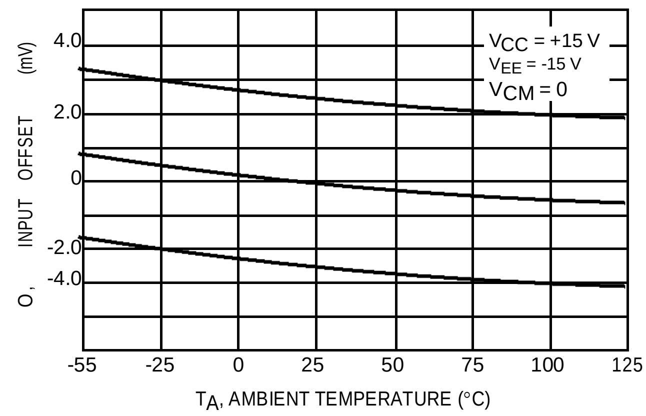


Figure 5. Input Offset Voltage versus Temperature for Representative Units

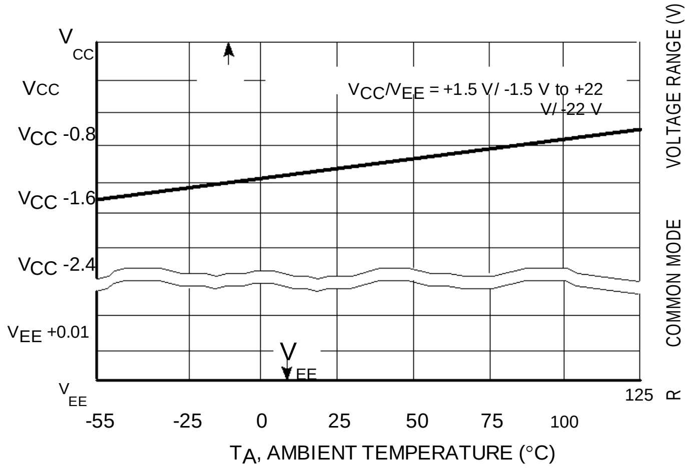


Figure 6. Input Common Mode Voltage Range versus Temperature

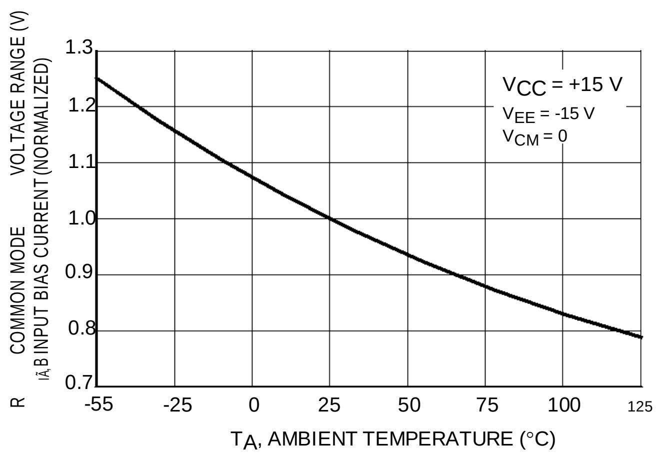


Figure 7. Normalized Input Bias Current versus Temperature

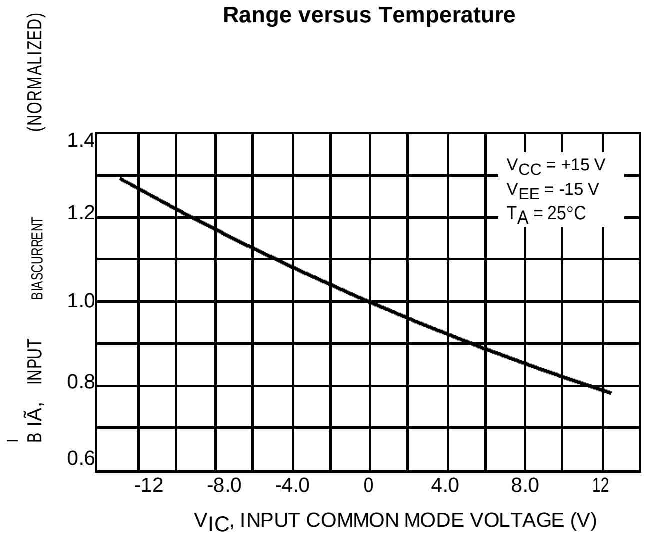


Figure 8. Normalized Input Bias Current versus Input Common Mode Voltage

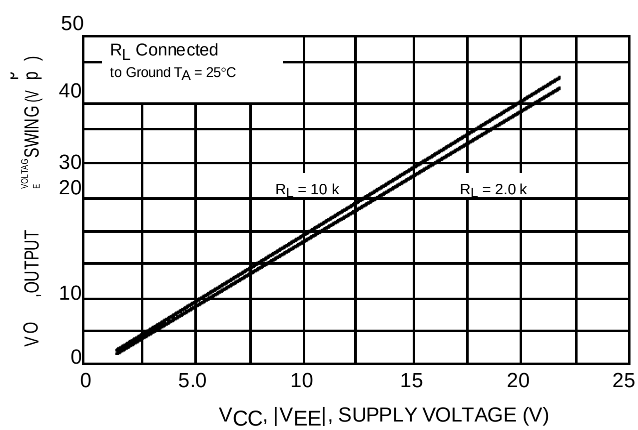


Figure 9. Split Supply Output Voltage Swing versus Supply Voltage

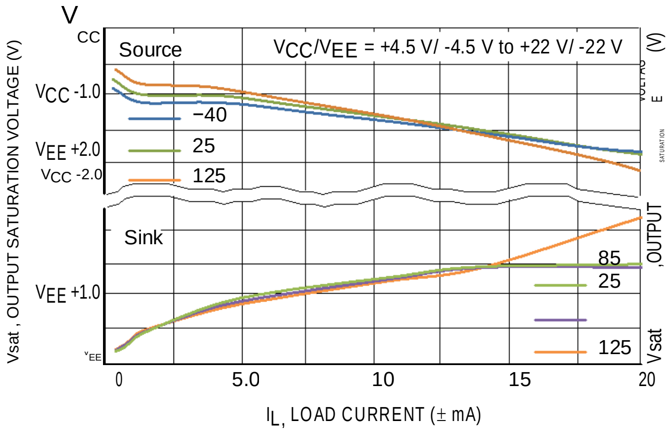


Figure 10. Split Supply Output Saturation versus Load Current

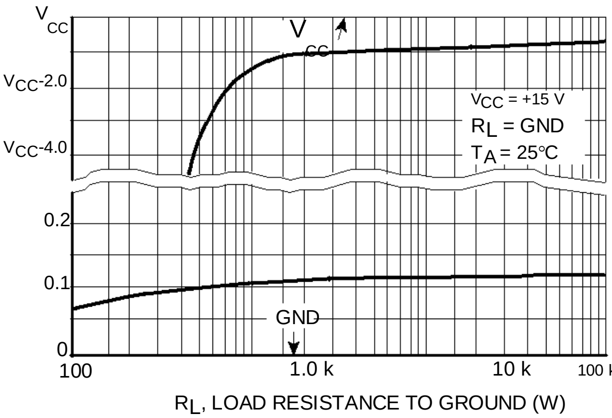


Figure 11. Single Supply Output Saturation versus Load Resistance to Ground

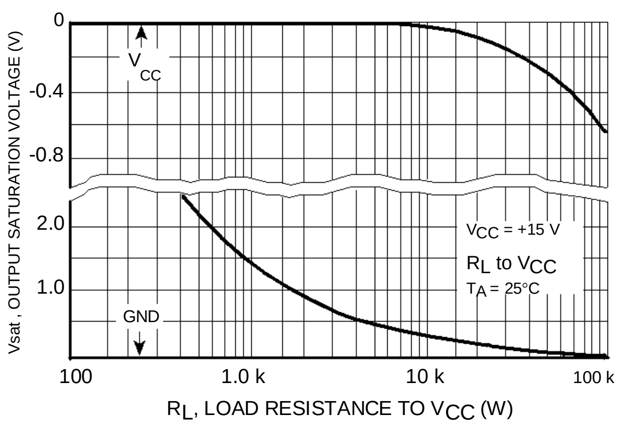


Figure 12. Single Supply Output Saturation versus Load Resistance to VCC

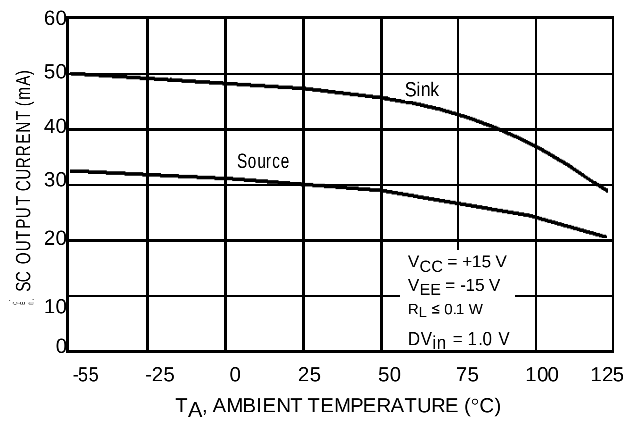


Figure 13. Output Short Circuit Current versus Temperature

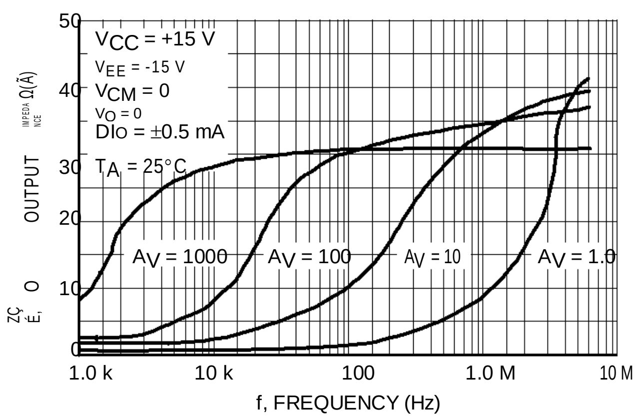


Figure 14. Output Impedance versus Frequency

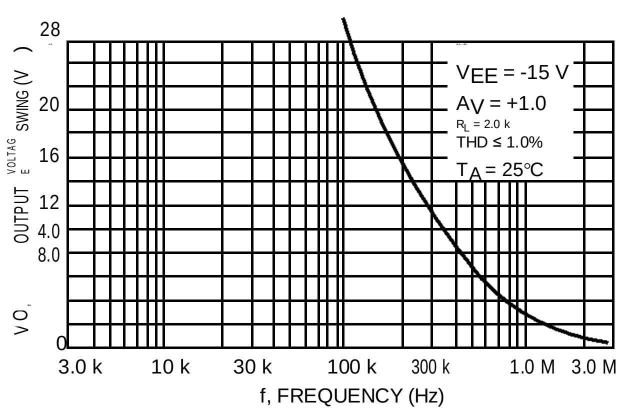


Figure 15. Output Voltage Swing versus Frequency

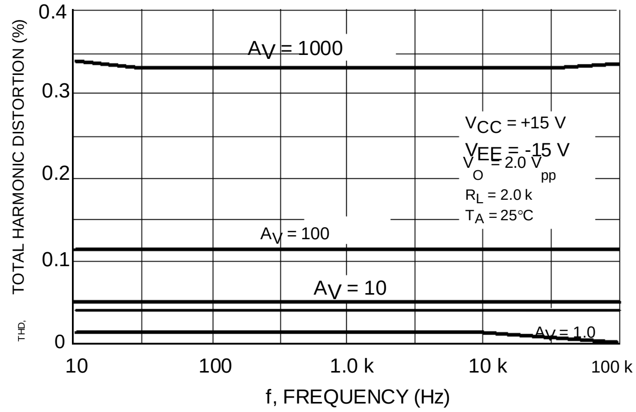


Figure 16. Total Harmonic Distortion versus Frequency

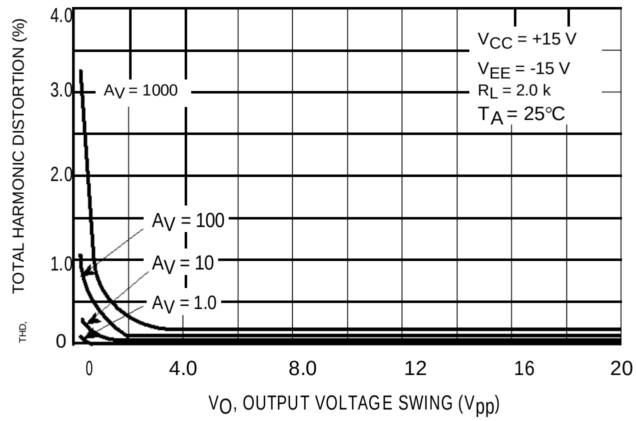


Figure 17. Total Harmonic Distortion versus Output Voltage Swing

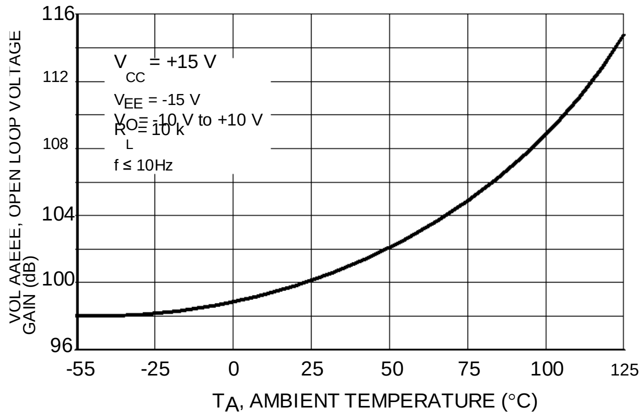


Figure 18. Open Loop Voltage Gain versus Temperature

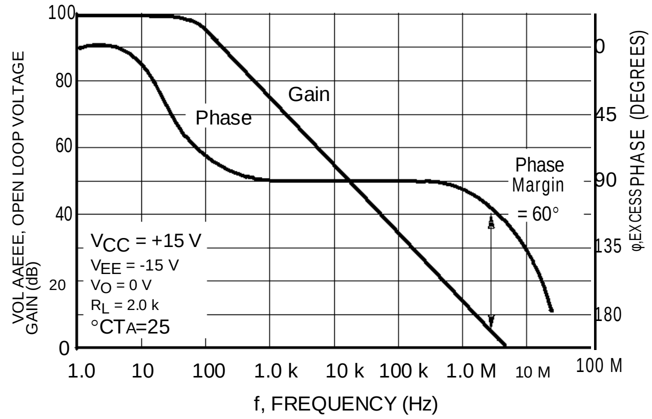


Figure 19. Open Loop Voltage Gain and Phase versus Frequency

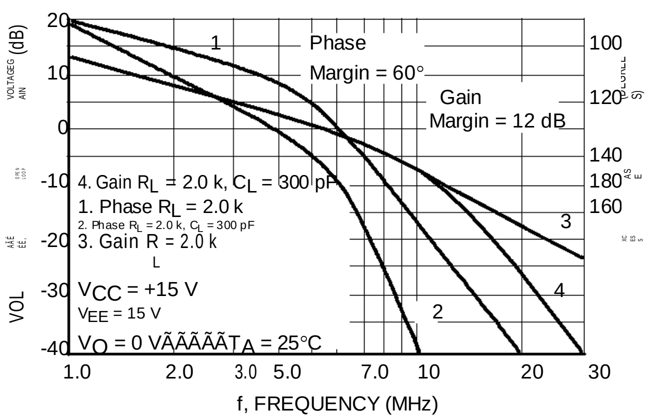


Figure 20. Open Loop Voltage Gain and Phase versus Frequency

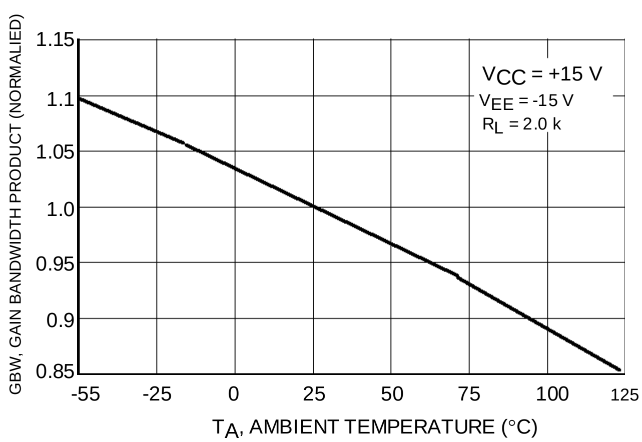


Figure 21. Normalized Gain Bandwidth Product versus Temperature

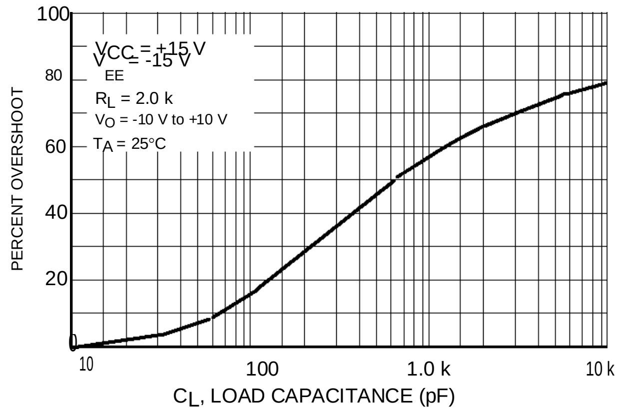


Figure 22. Percent Overshoot versus Load Capacitance

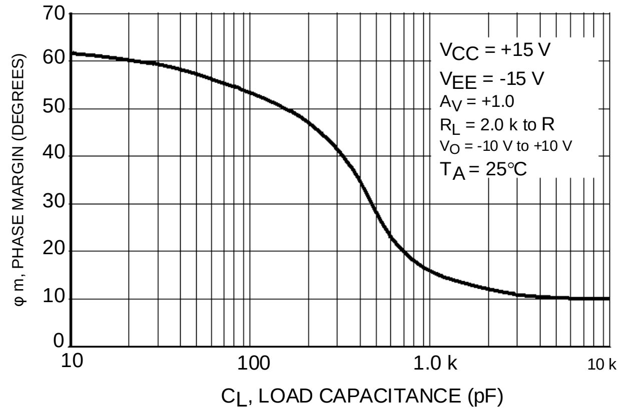


Figure 23. Phase Margin versus Load Capacitance

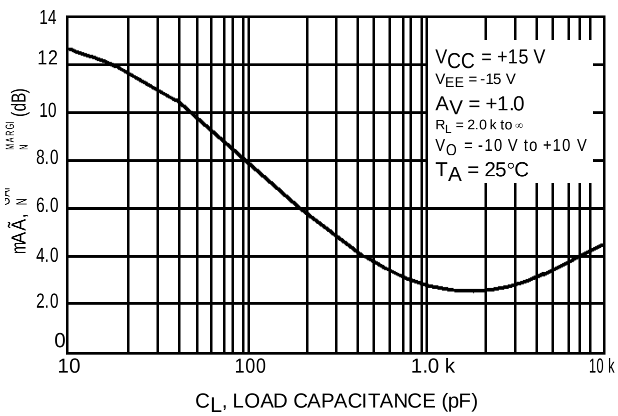


Figure 24. Gain Margin versus Load Capacitance

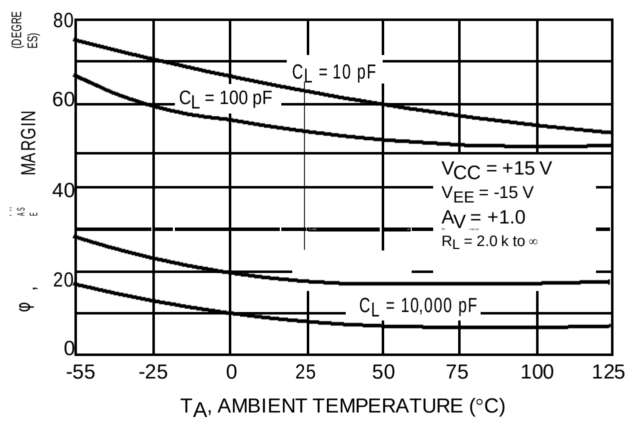


Figure 25. Phase Margin versus Temperature

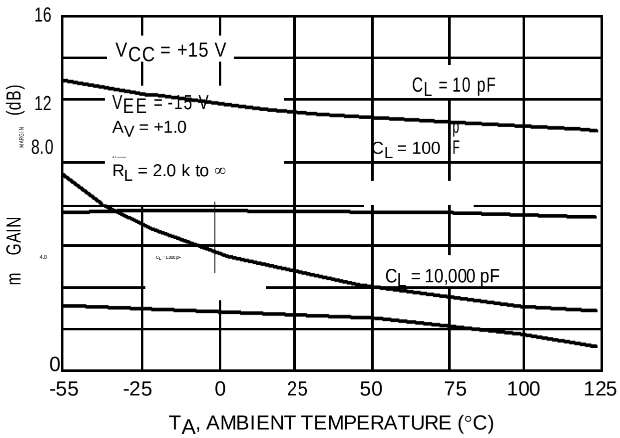


Figure 26. Gain Margin versus Temperature

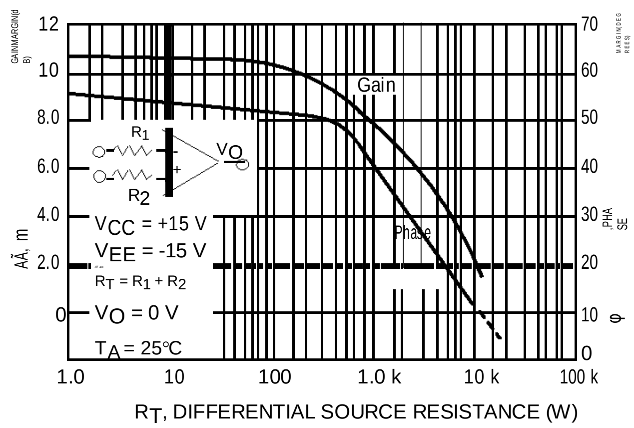


Figure 27. Phase Margin and Gain Margin versus Differential Source Resistance

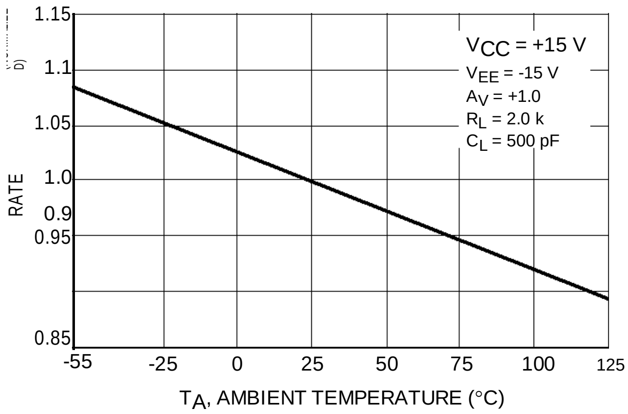


Figure 28. Normalized Slew Rate versus Temperature

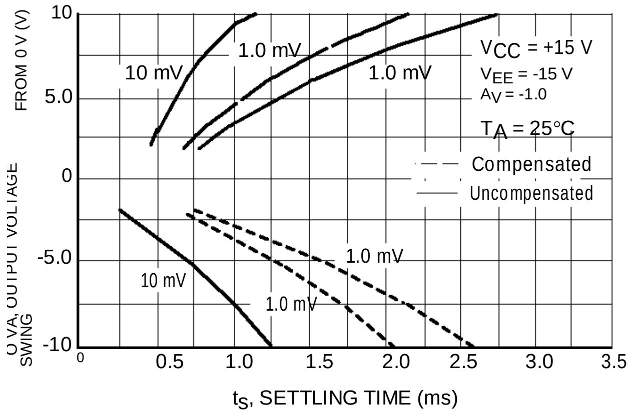


Figure 29. Output Settling Time

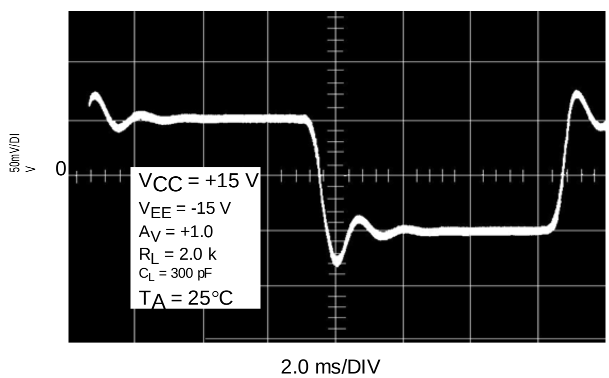


Figure 30. Small Signal Transient Response

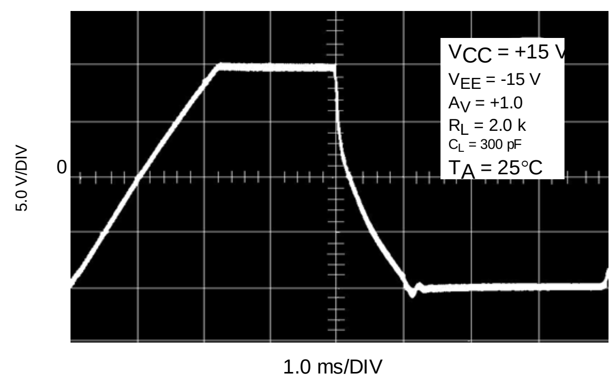


Figure 31. Large Signal Transient Response

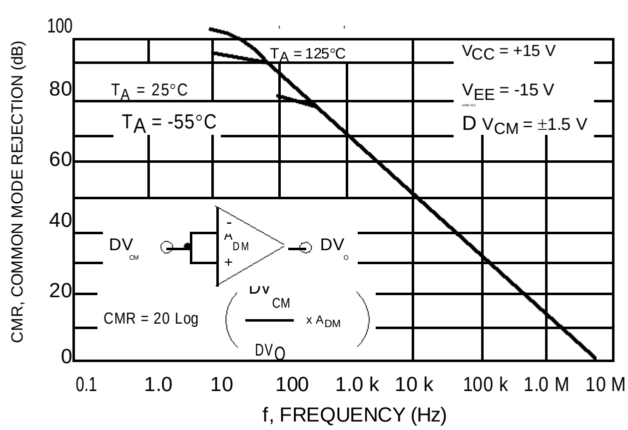


Figure 32. Common Mode Rejection versus Frequency

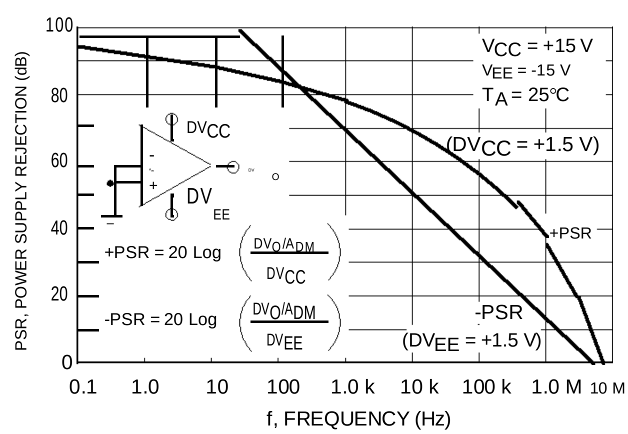


Figure 33. Power Supply Rejection versus Frequency

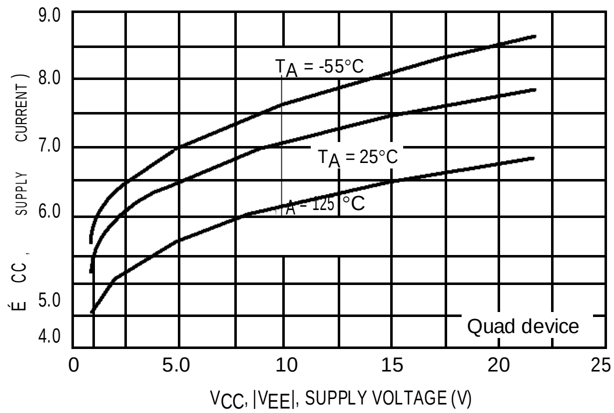


Figure 34. Supply Current versus Supply Voltage

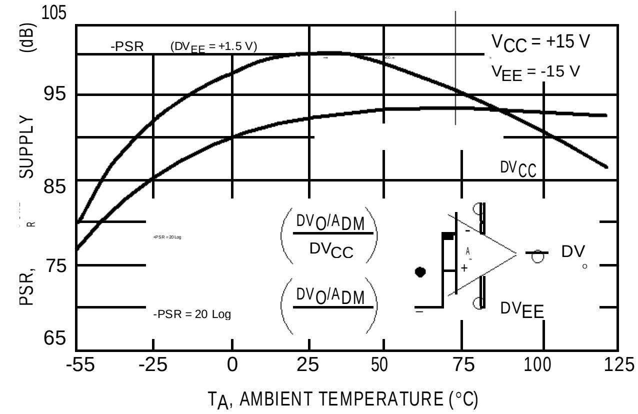


Figure 35. Power Supply Rejection versus Temperature

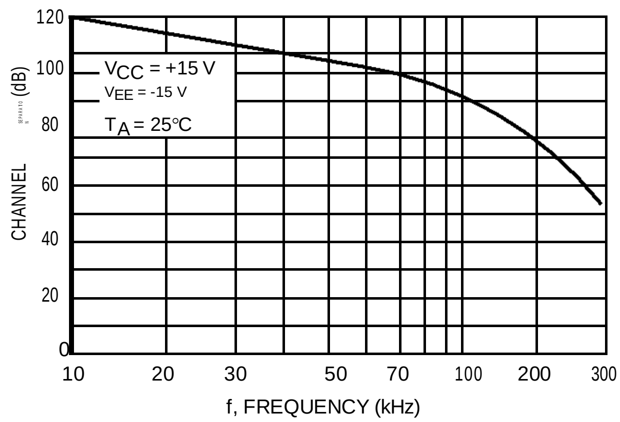


Figure 36. Channel Separation versus Frequency

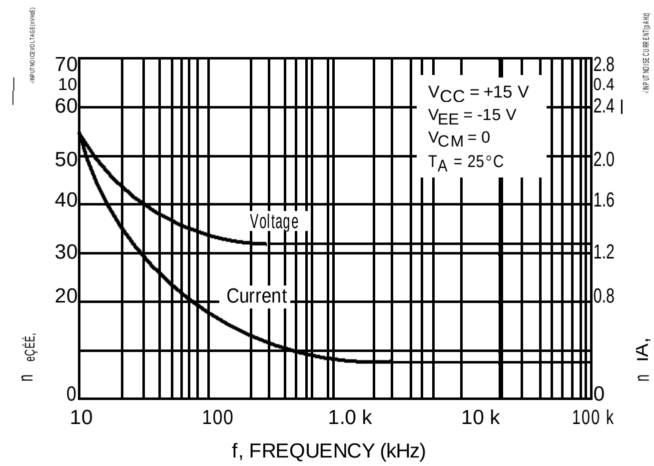


Figure 37. Input Noise versus Frequency

APPLICATIONS INFORMATION
CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the HT34071 amplifier series are similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{EE} and V_{CC} supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the V_{CC} voltage by approximately 3.0 V and decrease below the V_{EE} voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to approximately 5.0 mA of current from V_{EE} through either inputs clamping diode without damage or latching, although phase reversal may again occur.

If one or both inputs exceed the upper common mode voltage limit, the amplifier output is readily predictable and may be in a low or high state depending on the existing input bias conditions.

Since the input capacitance associated with the small geometry input device is substantially lower (2.5 pF) than the typical JFET input gate capacitance (5.0 pF), better frequency response for a given input source resistance can be achieved using the HT34071 series of amplifiers. This performance feature becomes evident, for example, in fast settling D−to−A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 2.0 kW of feedback resistance, the HT34071 series can settle to within 1/2 LSB of 8−bits in 1.0 ms, and within 1/2 LSB of 12−bits in 2.2 ms for a 10 V step. In a inverting unity gain fast settling configuration, the symmetrical slew rate is ±13 V/ms. In the classic noninverting unity gain configuration, the output positive slew rate is +10 V/ms, and the corresponding negative slew rate will exceed the positive slew rate as a function of the fall time of the input waveform.

Since the bipolar input device matching characteristics are superior to that of JFETs, a low untrimmed maximum offset voltage of 3.0 mV prime and 5.0 mV downgrade can be economically offered with high frequency performance characteristics. This combination is ideal for low cost precision, high speed quad op amp applications.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kW load resistance can swing within 1.0 V of the positive rail (V_{CC}), and within 0.3 V of the negative rail (V_{EE}), providing a 28.7 V_{pp} swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q_7, and V_{BE} of the NPN pull up transistor Q_{17}, and the voltage drop associated with the short circuit resistance, R_7. The negative swing is limited by the saturation voltage of the pull−down transistor Q_{16}, the voltage drop $I_L R_6$, and the voltage drop associated with resistance R_7, where I_L is the sink load current. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE}. For large valued sink currents (>5.0 mA), diode D3 clamps the voltage across R_6, thus limiting the negative swing to the saturation voltage of Q_{16}, plus the forward diode drop of D3 (≈V_{EE} +1.0 V). Thus for a given supply voltage, unprecedented peak−to−peak output voltage swing is possible as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter−follower transistor has been eliminated, the HT34071 series offers a 20 mA minimum current sink capability, typically to an output voltage of (V_{EE} +1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for fast high current switching applications.

In addition, the all NPN transistor output stage is inherently fast, contributing to the bipolar amplifier's high gain bandwidth product and fast settling capability. The associated high frequency low output impedance (30 W typ @ 1.0 MHz) allows capacitive drive capability from 0 pF to 10,000 pF without oscillation in the unity closed loop gain configuration. The 60° phase margin and 12 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The high frequency characteristics of the HT34071 series also allow excellent high frequency active filter capability, especially for low voltage single supply applications.

Although the single supply specifications is defined at 5.0 V, these amplifiers are functional to 3.0 V @ 25°C although slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

Special static precautions are not necessary for these bipolar amplifiers since there are no MOS transistors on the die.

As with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input−output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

(Typical Single Supply Applications V_{CC} = 5.0 V)

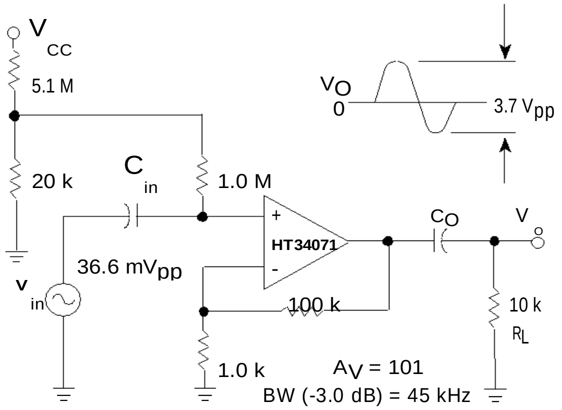


Figure 38. AC Coupled Noninverting Amplifier

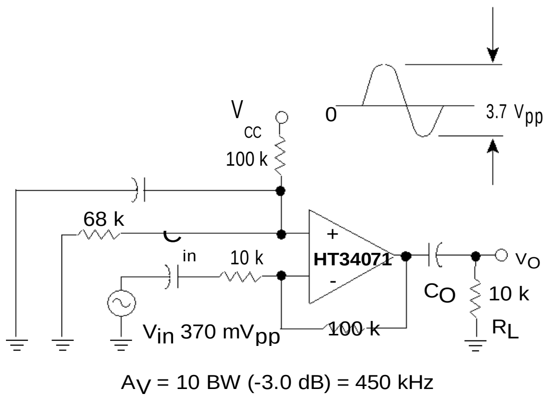


Figure 39. AC Coupled Inverting Amplifier

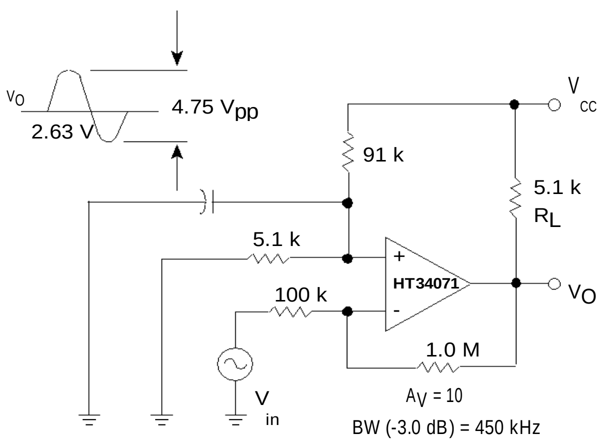


Figure 40. DC Coupled Inverting Amplifier Maximum Output Swing

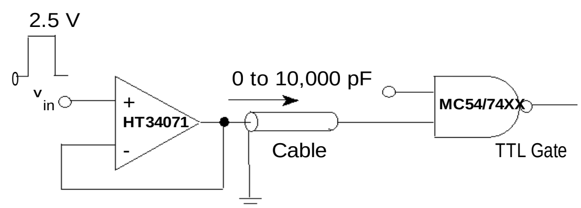


Figure 41. Unity Gain Buffer TTL Driver

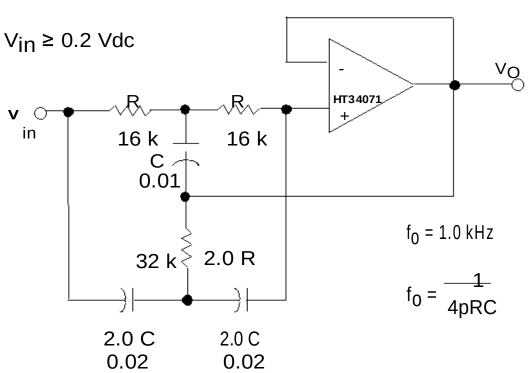
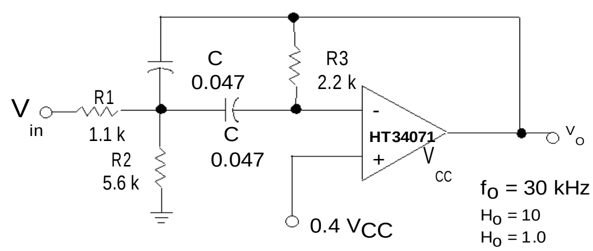


Figure 42. Active High−Q Notch Filter



Given f_O = Center Frequency

A_O = Gain at Center Frequency

Choose Value f_O, Q, A_O, C

Then: $R3 = \frac{Q}{\pi f_O C}$ $R1 = \frac{R3}{2 A_O}$ $R2 = \frac{R1\ R3}{4Q^2 R1 - R3}$

For less than 10% error from operational amplifier $\frac{Q_O f_O}{GBW} < 0.1$

where f_O and GBW are expressed in Hz.

GBW = 4.5 MHz Typ.

Figure 43. Active Bandpass Filter

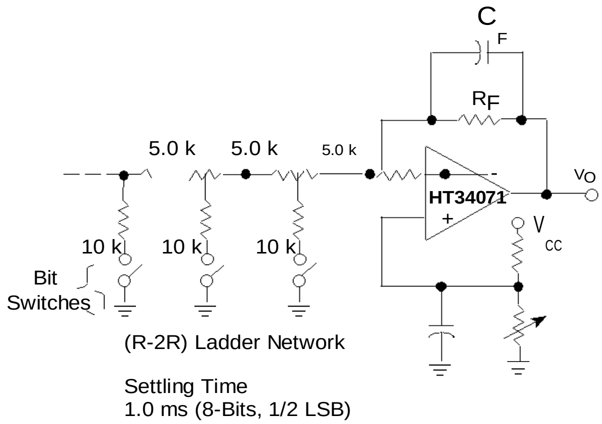


Figure 44. Low Voltage Fast D/A Converter

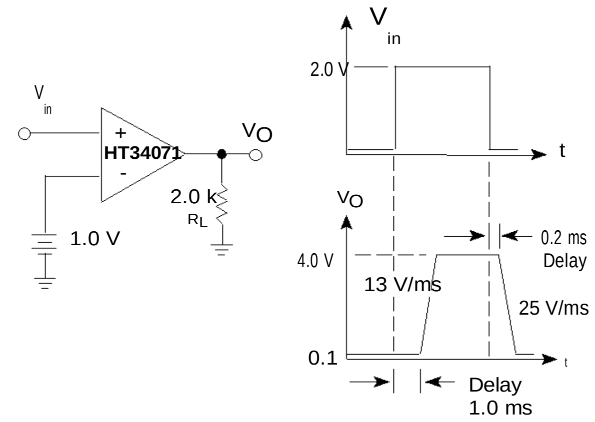


Figure 45. High Speed Low Voltage Comparator

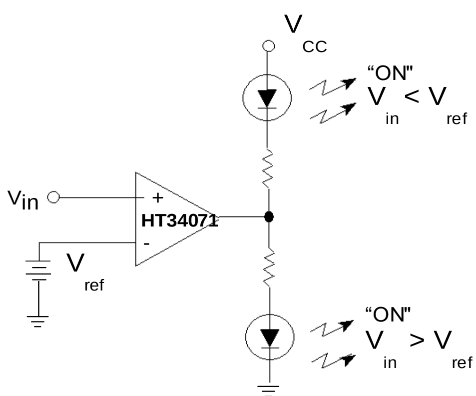


Figure 46. LED Driver

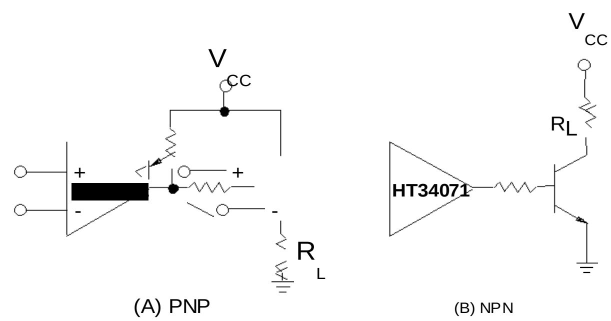


Figure 47. Transistor Driver

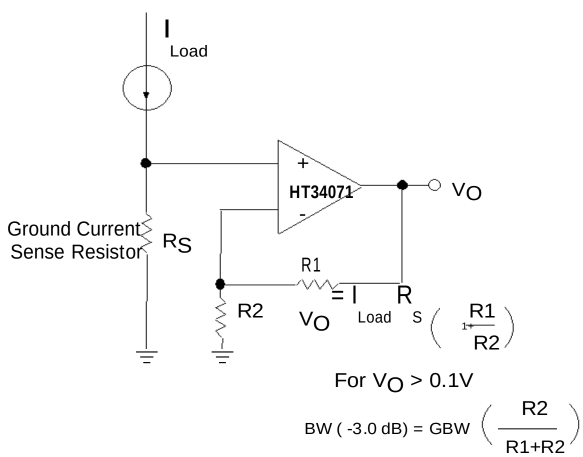


Figure 48. AC/DC Ground Current Monitor

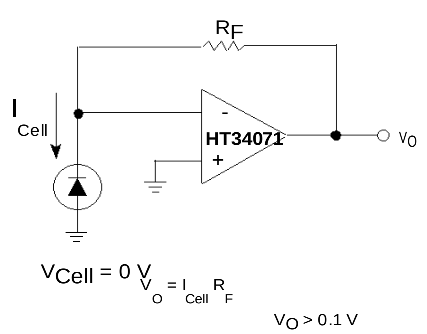


Figure 49. Photovoltaic Cell Amplifier

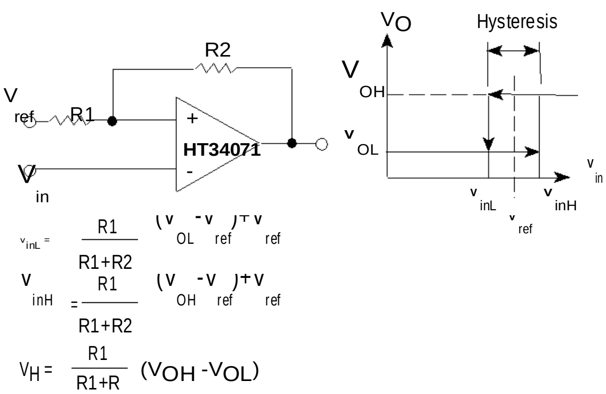


Figure 50. Low Input Voltage Comparator with Hysteresis

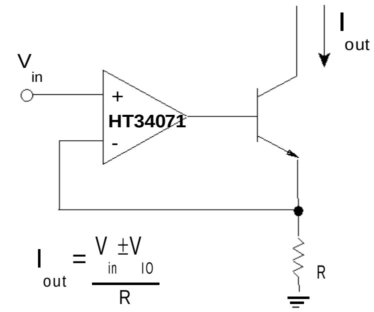


Figure 51. High Compliance Voltage to Sink Current Converter

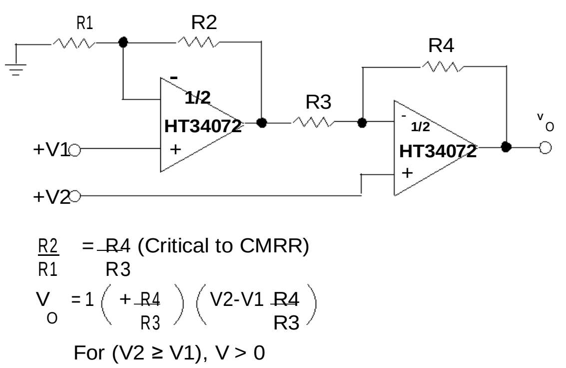


Figure 52. High Input Impedance Differential Amplifier

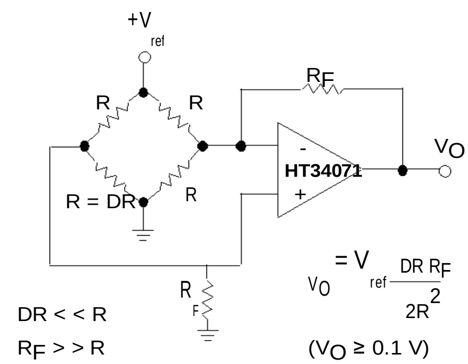


Figure 53. Bridge Current Amplifier

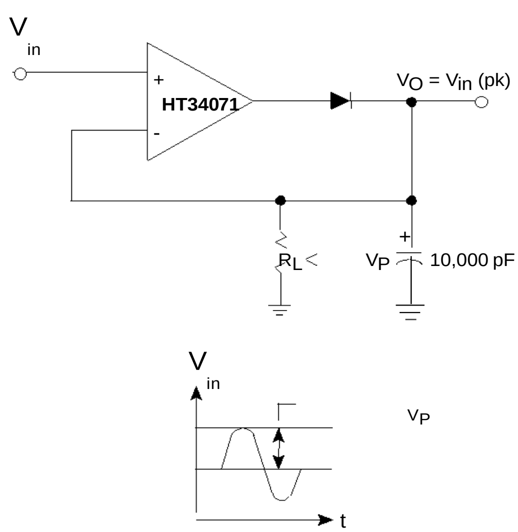


Figure 54. Low Voltage Peak Detector

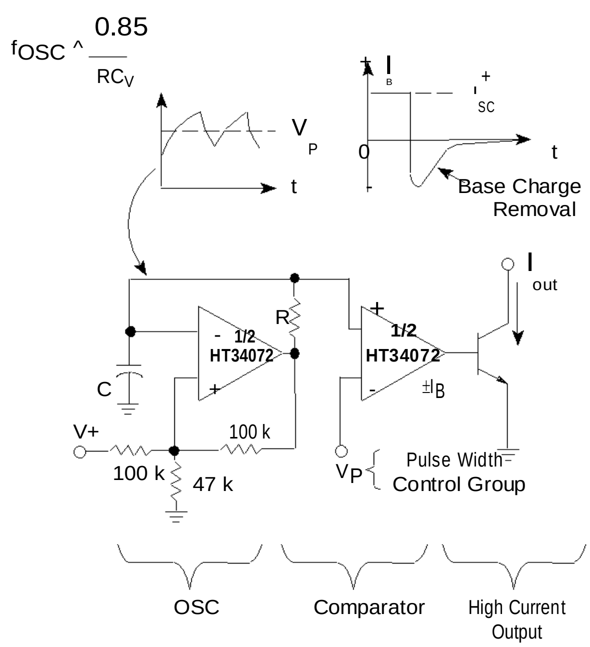


Figure 55. High Frequency Pulse Width Modulation

GENERAL ADDITIONAL APPLICATIONS INFORMATION $V_S = \pm 15.0$ V

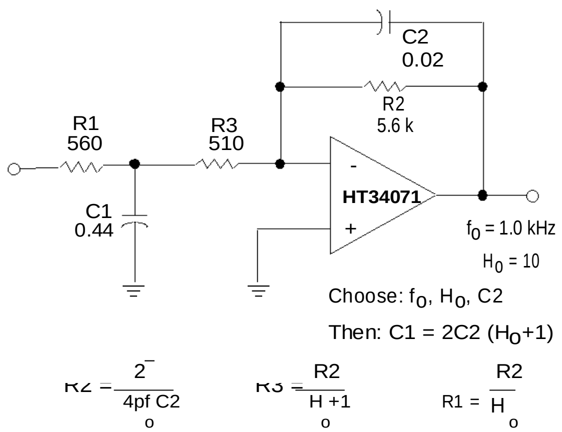


Figure 56. Second Order Low−Pass Active Filter

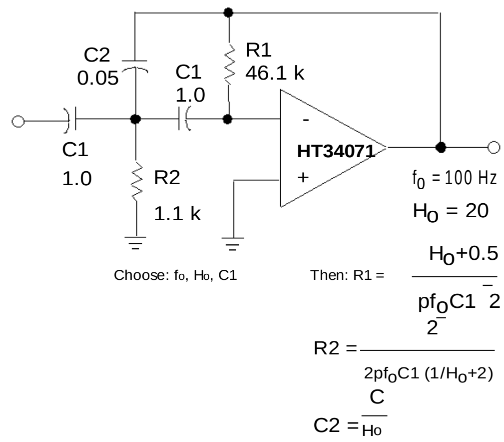


Figure 57. Second Order High−Pass Active Filter

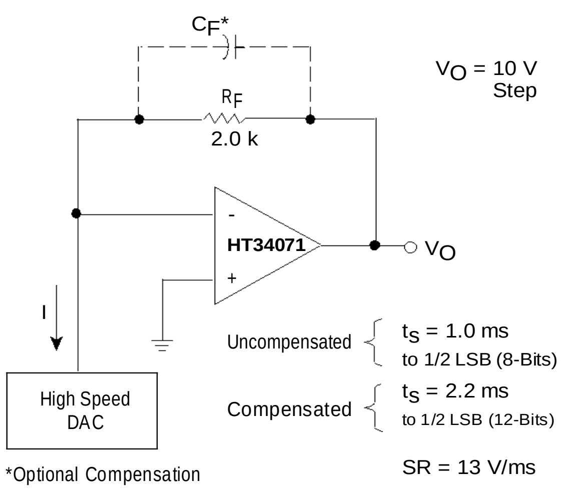


Figure 58. Fast Settling Inverter

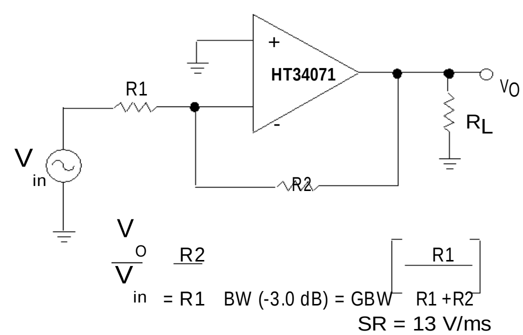


Figure 59. Basic Inverting Amplifier

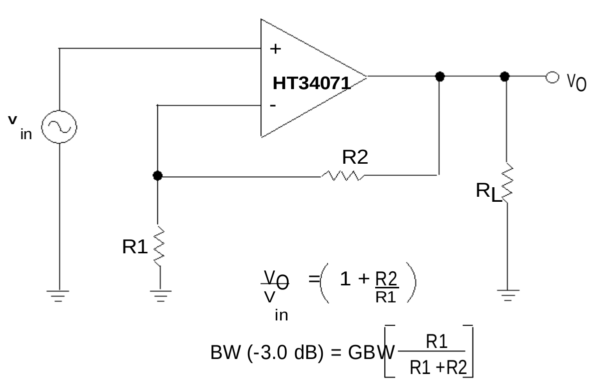


Figure 60. Basic Noninverting Amplifier

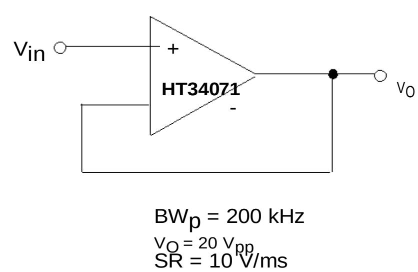


Figure 61. Unity Gain Buffer (A_V = +1.0)

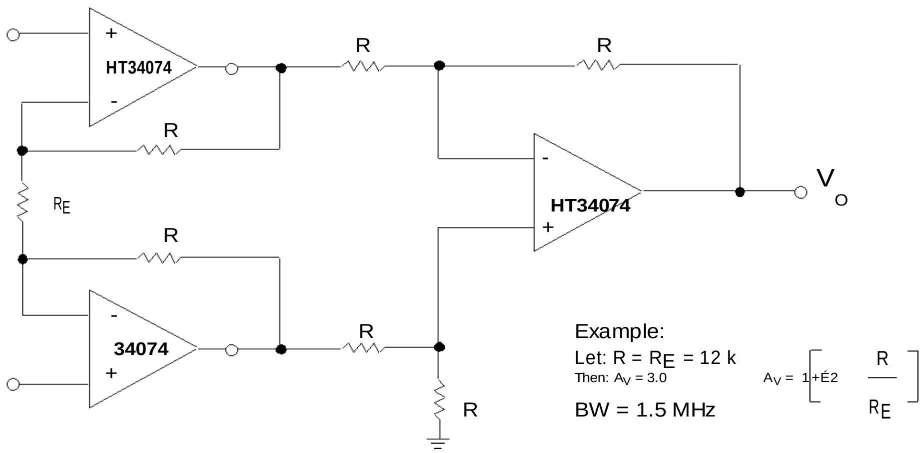
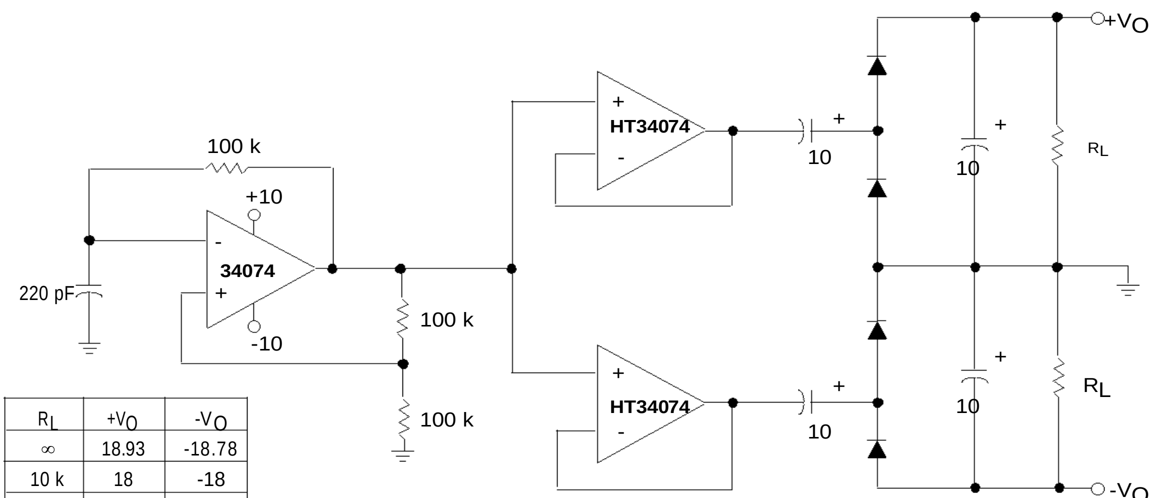


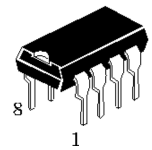
Figure 62. High Impedance Differential Amplifier

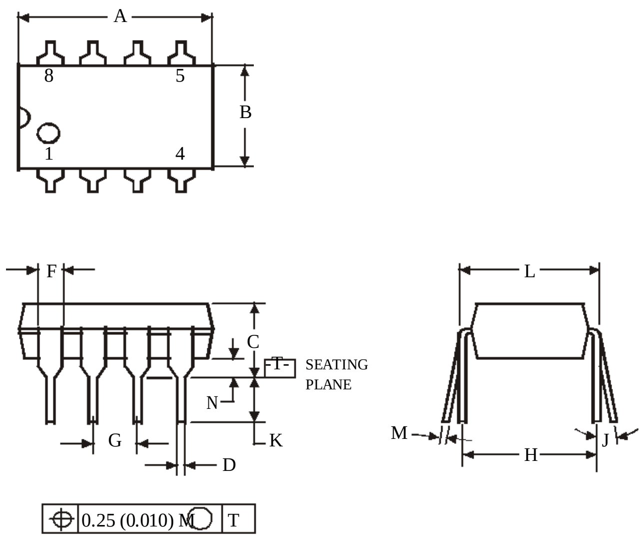


R_L	$+V_O$	$-V_O$
∞	18.93	-18.78
10 k	18	-18
5.0 k	15.4	-15.4

Figure 63. Dual Voltage Doubler

N SUFFIX PLASTIC DIP
(MS – 001BA)



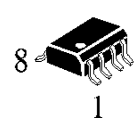


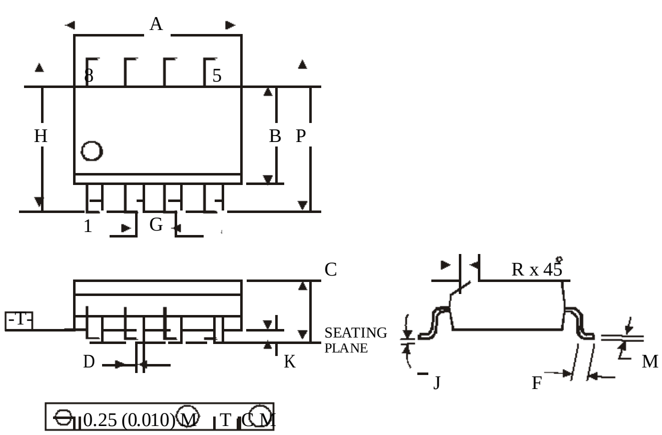
	Dimension, mm	
Symbol	MIN	MAX
A	8.51	10.16
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0 °	10 °
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions "A", "B" do not include mold flash or protrusions. Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 012AA)



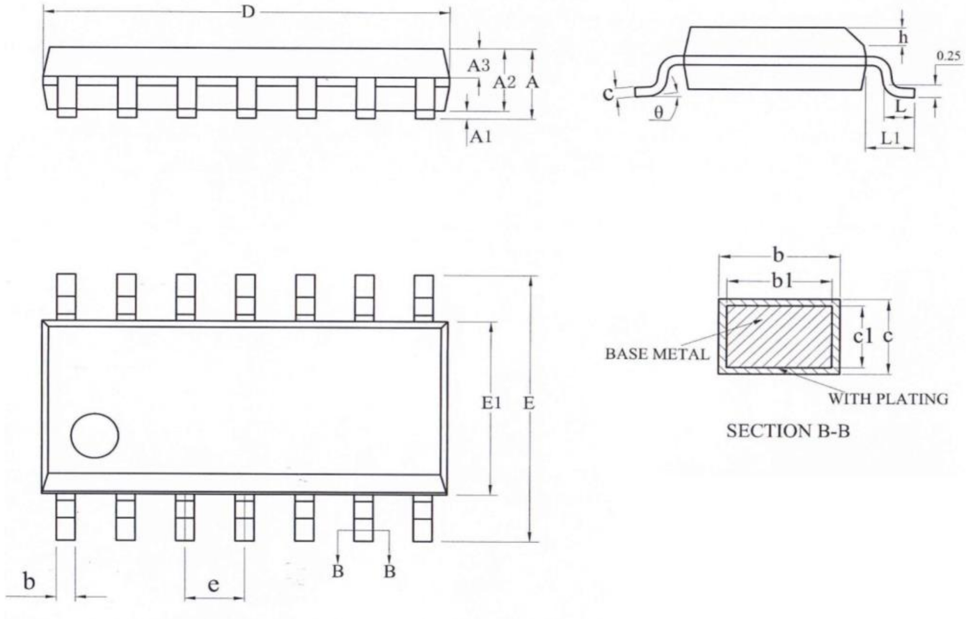


	Dimension, mm	
Symbol	MIN	MAX
A	4.8	5
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0 °	8 °
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5

NOTES:

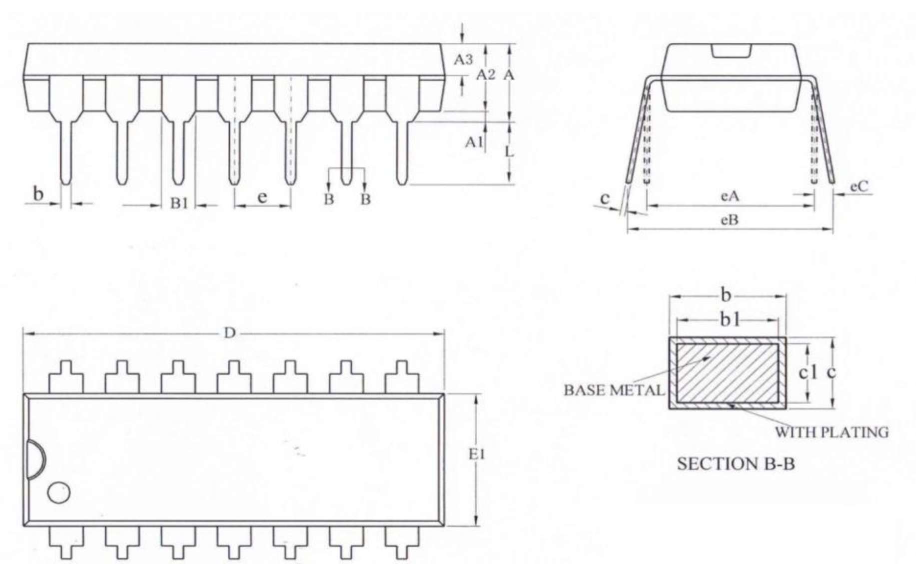
1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B ‐ 0.25 mm (0.010) per side.

SOP14



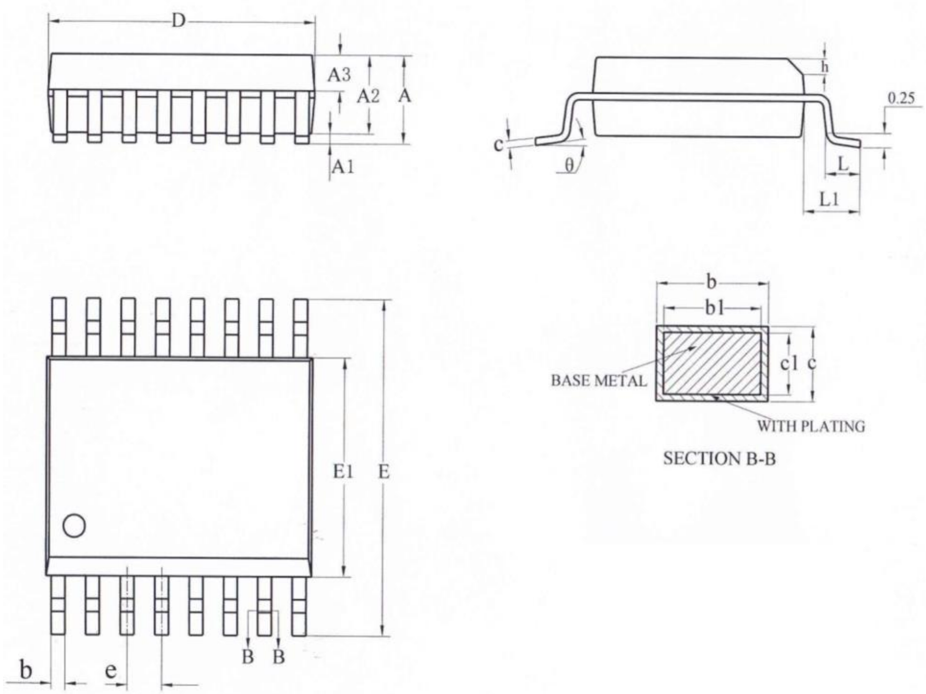
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
⚠ b	0.39	—	0.47
⚠ b1	0.38	0.41	0.44
⚠ c	0.20	—	0.24
c1	0.19	0.20	0.21
⚠ D	8.55	8.65	8.75
E	5.80	6.00	6.20
⚠ E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

DIP14



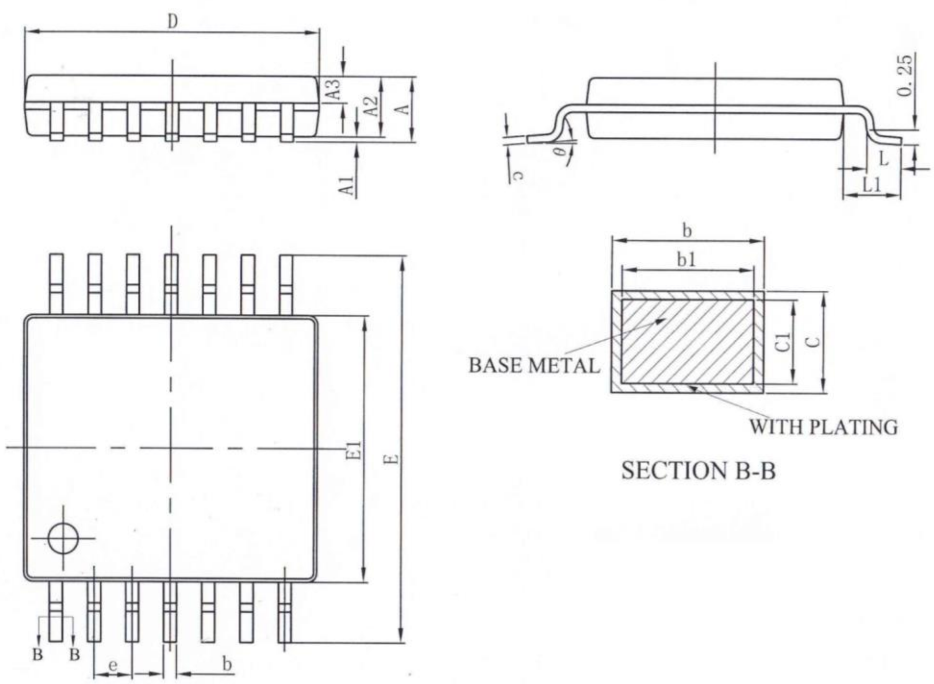
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	—	—
A2	3.20	3.30	3.40
A3	1.47	1.52	1.57
b	0.44	—	0.52
b1	0.43	0.46	0.49
B1	1.52REF		
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	19.00	19.10	19.20
E1	6.25	6.35	6.45
e	2.54BSC		
eA	7.62REF		
eB	7.62	—	9.30
eC	0	—	0.84
L	3.00	—	—

SSOP14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.55	0.60	0.65
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.25	—	0.50
L	0.50	0.65	0.80
L1	1.05REF		
θ	0	—	8°

TSSOP14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°