High Performance Current Mode Controllers

The HT3844B, HT3845B series are high performance fixed frequency current mode controllers. They are specifically designed for Off−Line
and dc−dc converter applications offering the designer a cost−effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle−by−cycle current limiting, a latch for single pulse metering, and a flip−flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed from 50% to 70%.

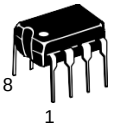
These devices are available in an 8−pin dual−in−line and surface mount (SOIC−8) plastic package as well as the 14−pin plastic surface mount (SOIC−14). The SOIC−14 package has separate power and ground pins for the totem pole output stage.

The UCX844B has UVLO thresholds of 16V (on) and 10V (off), ideally suited for off−line converters. The UCX845B is tailored for lower voltage applications having UVLO thresholds of 8.5V (on) and 7.6V (off).

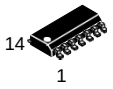
Features

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50% to 70%

- Automatic Feed Forward Compensation
- Latching PWM for Cycle−By−Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- These Devices are Pb−Free and are RoHS Compliant
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

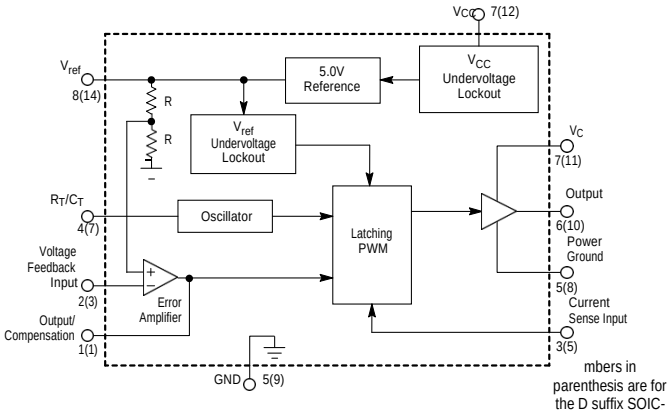


PDIP−8
N SUFFIX
CASE 626

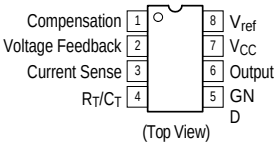


SOIC−14
R SUFFIX
CASE 751A

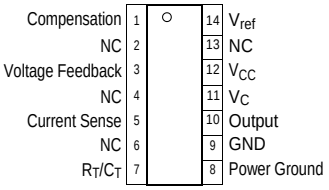
SOIC−8
R SUFFIX
CASE 751



PIN CONNECTIONS



(Top View)



(Top View)

Rating	Symbol	Value	Unit
Bias and Driver Voltages (Zero Series Impedance, see also Total Device spec) (Note 1)	V_{CC}, V_C	36	V
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 2)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	− 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package, SOIC−14 Case 751A			
Maximum Power Dissipation @ T_A = 25°C	P_D	862	mW
Thermal Resistance, Junction−to−Air	R_{SJA}	145	°C/W
D1 Suffix, Plastic Package, SOIC−8 Case 751			
Maximum Power Dissipation @ T_A = 25°C	P_D	702	mW
Thermal Resistance, Junction−to−Air	R_{SJA}	178	°C/W
N Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A = 25°C	P_D	1.25	W
Thermal Resistance, Junction−to−Air	R_{SJA}	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature HT3844B, HT3845B HT2844B, HT2845B HT3844BV, HT3845BV	T_A	0 to +70 −25 to +85 −40 to +105	°C
Storage Temperature Range	T_{stg}	− 65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The voltage is clamped by a zener diode (see page 9 Under Voltage Lockout section). Therefore this voltage may be exceeded as long as the total power supply and zener current is not exceeded.
2. Maximum package power dissipation limits must be observed.
3. This device series contains ESD protection and exceeds the following tests: Human Body Model 4000 V per JEDEC Standard JESD22-A114B, Machine Model Method 200 V per JEDEC Standard JESD22-A115-A
4. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 5], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 6], unless otherwise noted.)

Characteristic	Symbol	HT284xB Min	HT284xB Typ	HT284xB Max	HT384xB, xBV, HTV384xBV Min	HT384xB, xBV, HTV384xBV Typ	HT384xB, xBV, HTV384xBV Max	Unit
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	−	2.0	20	−	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	−	3.0	25	−	3.0	25	mV
Temperature Stability	T_S	−	0.2	−	−	0.2	−	mV/°C
Total Output Variation over Line, Load, & Temperature	V_{ref}	4.9	−	5.1	4.82	−	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	−	50	−	−	50	−	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	−	5.0	−	−	5.0	−	mV
Output Short Circuit Current	I_{SC}	− 30	− 85	−180	− 30	− 85	−180	mA
OSCILLATOR SECTION								
Frequency T_J = 25°C T_A = T_{low} to T_{high} T_J = 25°C (R_T = 6.2 k, C_T = 1.0 nF)	f_{OSC}	49 48 225	52 − 250	55 56 275	49 48 225	52 − 250	55 56 275	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	Mf_{OSC}/MV	−	0.2	1.0	−	0.2	1.0	%
Frequency Change w/ Temperature (T_A = T_{low} to T_{high})	Mf_{OSC}/MT	−	1.0	−	−	0.5	−	%
Oscillator Voltage Swing (Peak−to−Peak)	V_{OSC}	−	1.6	−	−	1.6	−	V

5. Adjust V_{CC} above the Startup threshold before setting to 15 V.
6. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for HT3844B, HT3845B T_{high} = + 70°C for HT3844B, HT3845B
   = − 25°C for HT2844B, HT2845B = + 85°C for HT2844B, HT2845B

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 7], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 8], unless otherwise noted.)

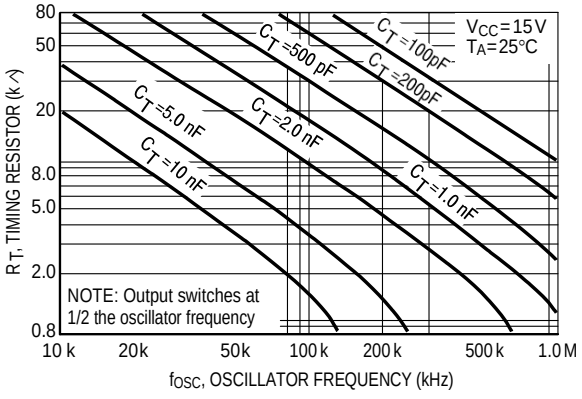
Characteristic	Symbol	HT284xB			HT384xB, xBV, HTV384xBV			Unit
		Min	Typ	Max	Min	Typ	Max	
OSCILLATOR SECTION								
Discharge Current (V_{OSC} = 2.0 V) T_J = 25°C	I_{dischg}	7.8	8.3	8.8	7.8	8.3	8.8	mA
T_A = T_{low} to T_{high} (HT284XB, HT384XB)		7.5	–	8.8	7.6	–	8.8	
(HT384XBV)		–	–	–	7.2	–	8.8	
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	– 0.1	–1.0	–	– 0.1	– 2.0	µA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB
Output Current – Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	–	2.0	12	–	mA
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	– 0.5	–1.0	–	– 0.5	–1.0	–	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	–	5.0	6.2	–	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}							
(HT284XB, HT384XB)		–	0.8	1.1	–	0.8	1.1	
(HT384XBV)		–	–	–	–	0.8	1.2	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 9 & 10)	A_V							V/V
(HT284XB, HT384XB)		2.85	3.0	3.15	2.85	3.0	3.15	
(HT384XBV)		–	–	–	2.85	3.0	3.25	
Maximum Current Sense Input Threshold (Note 9)	V_{th}							V
(HT284XB, HT384XB)		0.9	1.0	1.1	0.9	1.0	1.1	
(HT384XBV)		–	–	–	0.85	1.0	1.1	
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V) (Note 9)	PSRR	–	70	–	–	70	–	dB
Input Bias Current	I_{IB}	–	– 2.0	–10	–	– 2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(In/Out)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{Sink} = 200 mA, HT284XB, HT384XB)		–	1.6	2.2	–	1.6	2.2	
(I_{Sink} = 200 mA, HT384XBV)		–	–	–	–	1.6	2.3	
High State (I_{Source} = 20 mA, HT284XB, HT384XB)	V_{OH}	13	13.5	–	13	13.5	–	
(I_{Source} = 20 mA, HT384XBV)		–	–	–	12.9	–	–	
(I_{Source} = 200 mA)		12	13.4	–	12	13.4	–	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.1	1.1	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Startup Threshold UCX844B, BV	V_{th}	15	16	17	14.5	16	17.5	V
UCX845B, BV		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn–On UCX844B, BV	$V_{CC(min)}$	9.0	10	11	8.5	10	11.5	V
UCX845B, BV		7.0	7.6	8.2	7.0	7.6	8.2	

7. Adjust V_{CC} above the Startup threshold before setting to 15 V.
8. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for HT3844B, HT3845B; T_{high} = + 70°C for HT3844B, HT3845B
   = – 25°C for HT2844B, HT2845B; = + 85°C for HT2844B, HT2845B
   = – 40°C for HT384xBV, HTV384xBV; = +105°C for HT3844BV,HT3845BV
   = +125°C for HTV384xBV
9. This parameter is measured at the latch trip point with V_{FB} = 0 V.
10. Comparator gain is defined as: $A_V = \frac{\text{MV Output/Compensation}}{\text{MV Current Sense Input}}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 11], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 12], unless otherwise noted.)

Characteristic	Symbol	HT284xB			HT384xB, xBV, NCV384xBV			Unit
		Min	Typ	Max	Min	Typ	Max	
PWM SECTION								
Duty Cycle								%
Maximum (HT284XB, HT384XB)	$DC_{(max)}$	47	48	50	47	48	50	
(HT384XBV)		–	–	–	46	48	50	
Minimum	$DC_{(min)}$	–	–	0	–	–	0	
TOTAL DEVICE								
Power Supply Current	I_{CC}							mA
Startup (V_{CC} = 6.5 V for UCX845B, 14 V for UCX844B, BV)		–	0.3	0.5	–	0.3	0.5	
Operating (Note 11)		–	12	17	–	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

11. Adjust V_{CC} above the Startup threshold before setting to 15 V.
12. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
    T_{low} = 0°C for HT3844B, HT3845B; = –25°C for HT2844B, HT2845B; = –40°C for HT384xBV, HTV384xBV
    T_{high} = + 70°C for HT3844B, HT3845B; = + 85°C for HT2844B, HT2845B; = +105°C for HT3844BV,HT3845BV; =+125°C for HTV384xBV



For $R_T > 5$ Kf $\sim \frac{1.72}{R_T C_T}$

Figure 2. Timing Resistor versus Oscillator Frequency

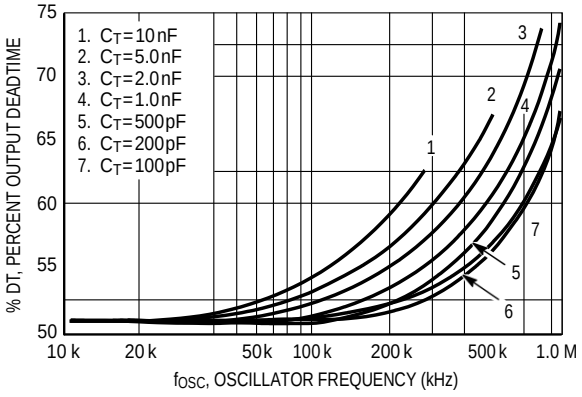


Figure 3. Output Deadtime versus Oscillator Frequency

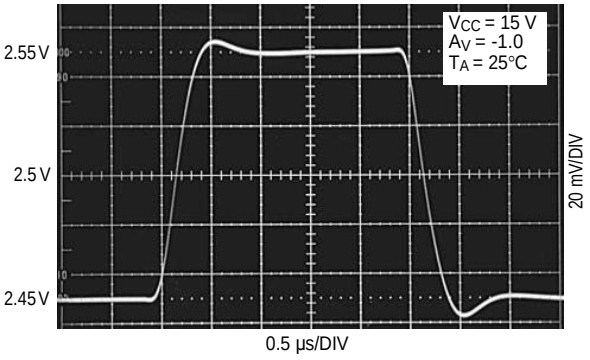


Figure 4. Error Amp Small Signal Transient Response

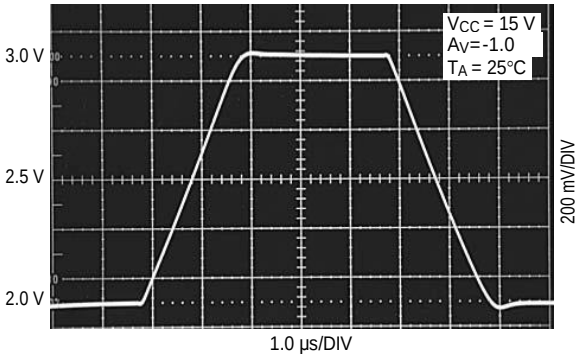


Figure 5. Error Amp Large Signal Transient Response

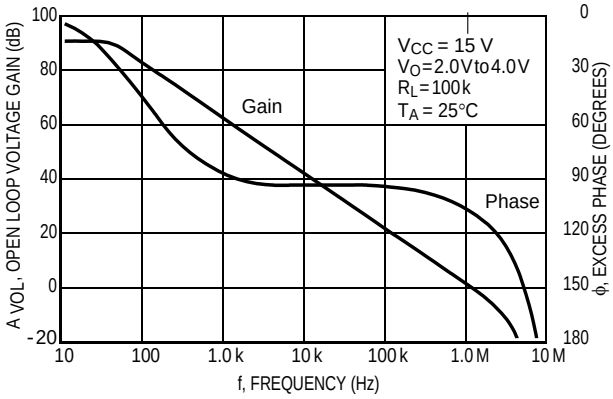


Figure 6. Error Amp Open Loop Gain and Phase versus Frequency

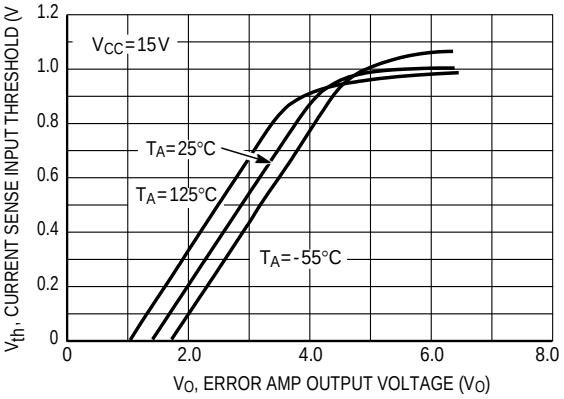


Figure 7. Current Sense Input Threshold versus Error Amp Output Voltage

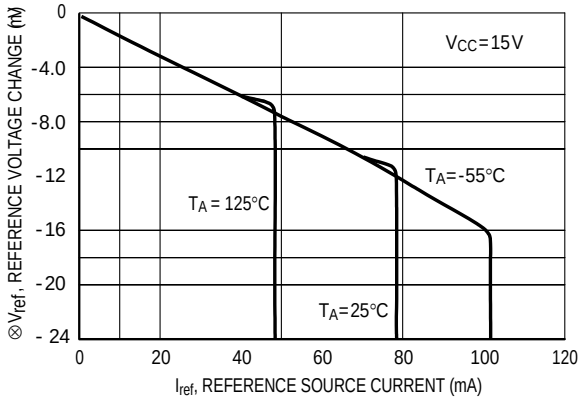


Figure 8. Reference Voltage Change versus Source Current

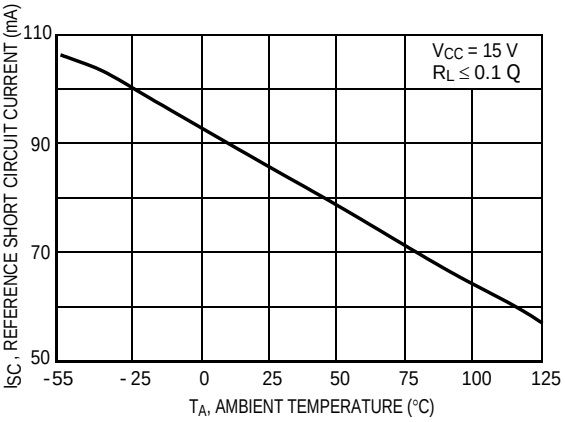


Figure 9. Reference Short Circuit Current versus Temperature

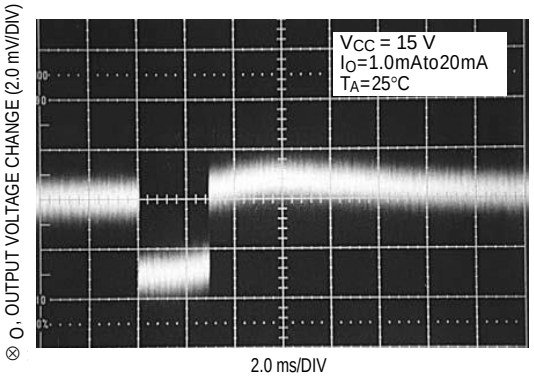


Figure 10. Reference Load Regulation

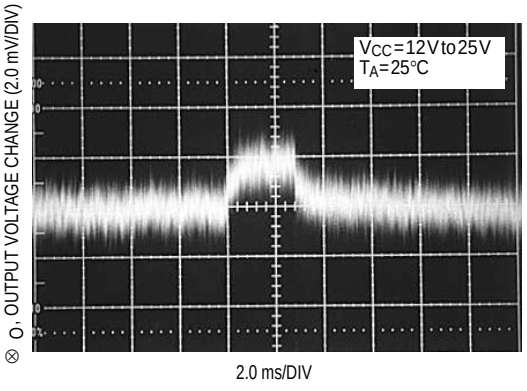


Figure 11. Reference Line Regulation

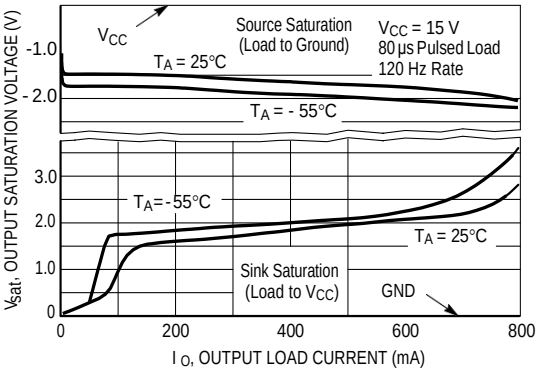


Figure 12. Output Saturation Voltage versus Load Current

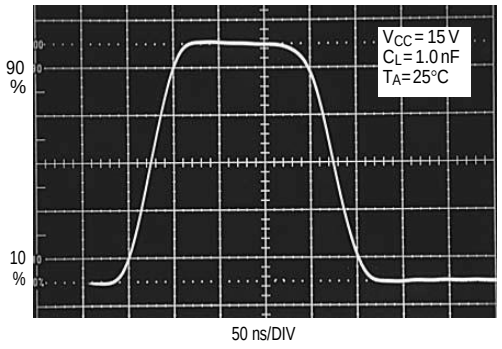


Figure 13. Output Waveform

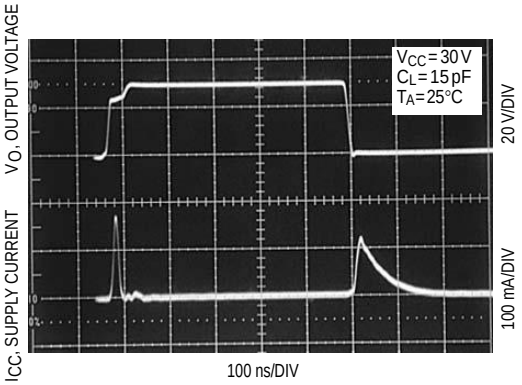


Figure 14. Output Cross Conduction

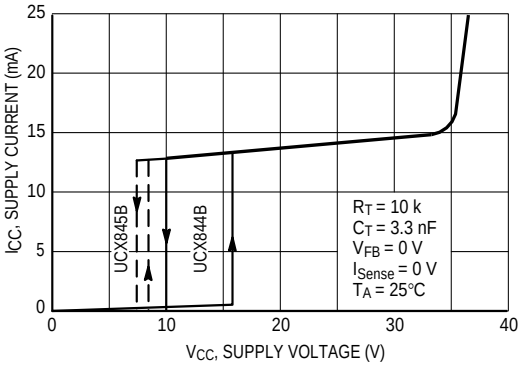


Figure 15. Supply Current versus Supply Voltage

PIN FUNCTION DESCRIPTION

Pin		Function	Description
8–Pin	14–Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Oscillator operation to 1.0 kHz is possible.
5		GND	This pin is the combined control circuitry and power ground.
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin. The output switches at one−half the oscillator frequency.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
	8	Power Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
	9	GND	This pin is the control circuitry ground return and is connected back to the powersource ground.
	2,4,6,13	NC	No connection. These pins are not internally connected.

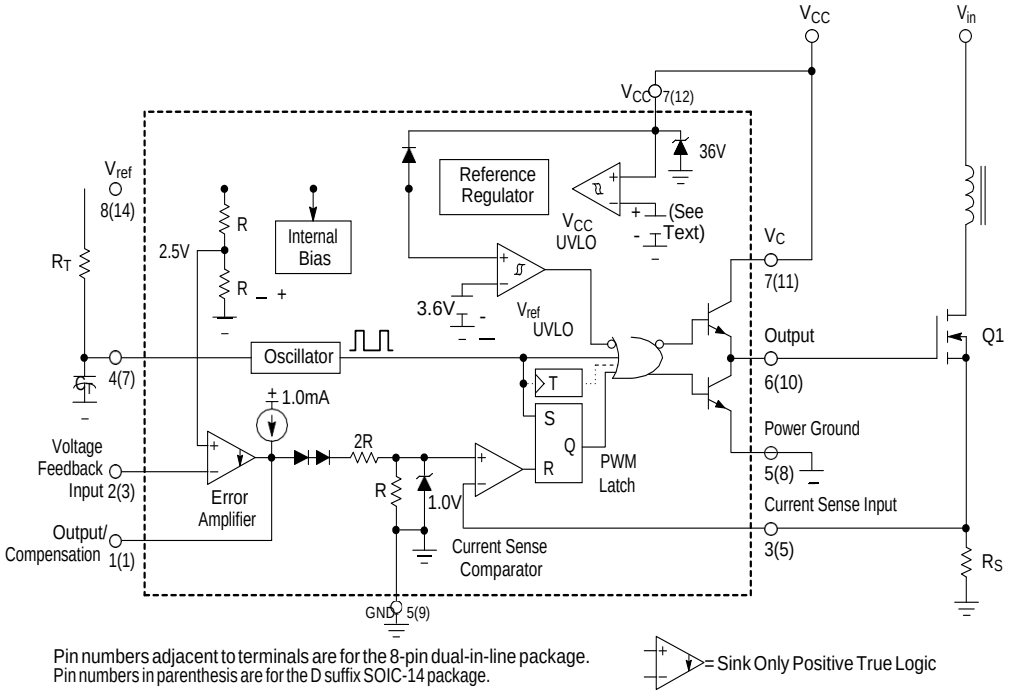


Figure 16. Representative Block Diagram

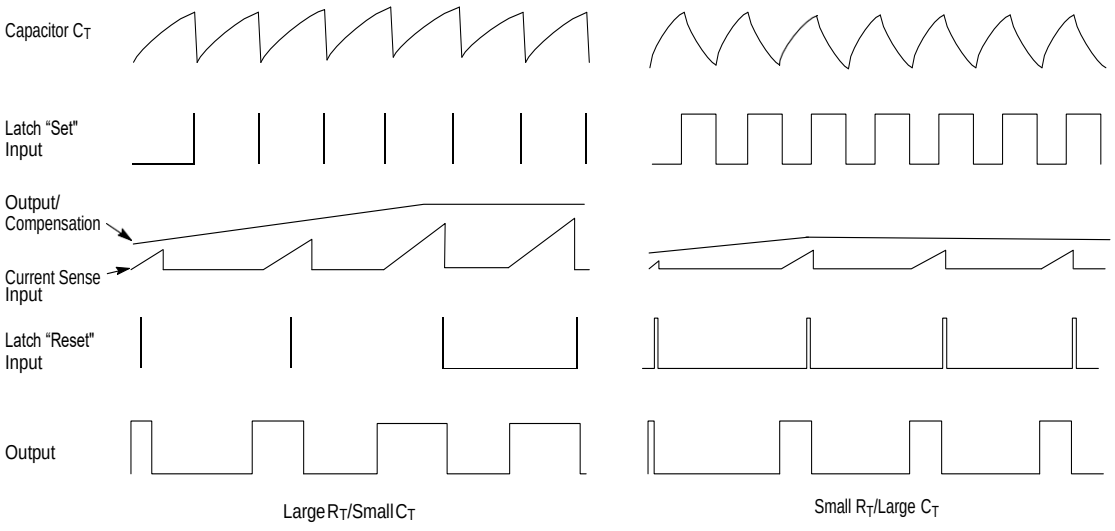


Figure 17. Timing Diagram

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built−in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX844B, and 8.4 V/7.6 V for the UCX845B. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low startup current of the UCX844B makes it ideally suited in off−line converter applications where efficient bootstrap startup techniques are required (Figure 30). The UCX845B is intended for lower voltage dc−dc converter applications. A 36 V Zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage for the UCX844B is 11 V and 8.2 V for the UCX845B.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pulldown resistor.

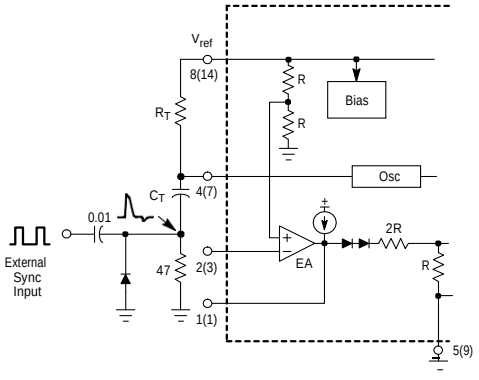
The SOIC−14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A Zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 23 shows proper power and control ground connections in a current−sensing power MOSFET application.

Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the HT284XB, and ±2.0% on the HT384XB. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short−circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

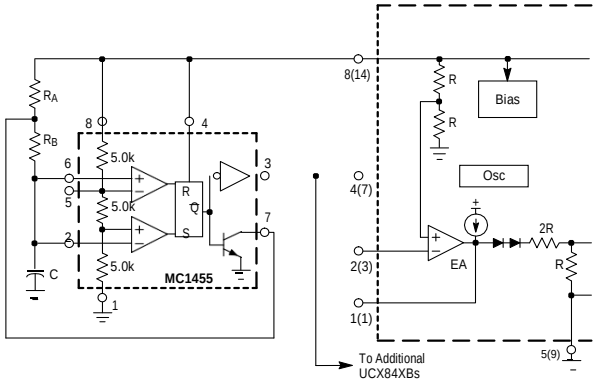
Design Considerations

Do not attempt to construct the converter on wire−wrap or plug−in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse−width jitter. This is usually caused by excessive noise pick−up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low−current signal and high−current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise−generating components.



The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Figure 18. External Clock Synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D(max) = \frac{R_A}{R_A + 2R_B}$$

Figure 19. External Duty Cycle Clamp and Multi−Unit Synchronization

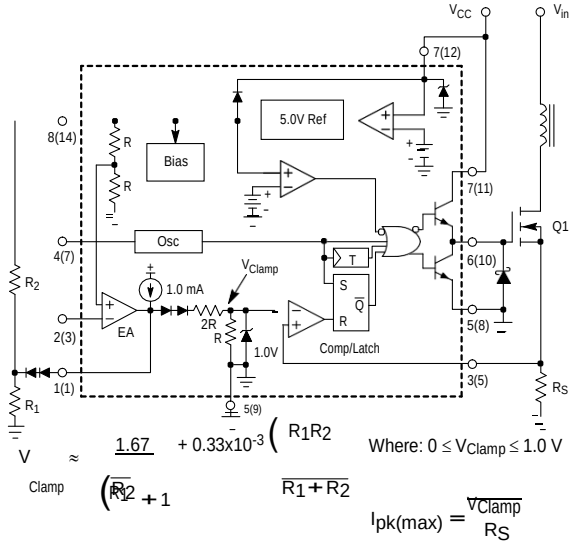


Figure 20. Adjustable Reduction of Clamp Level

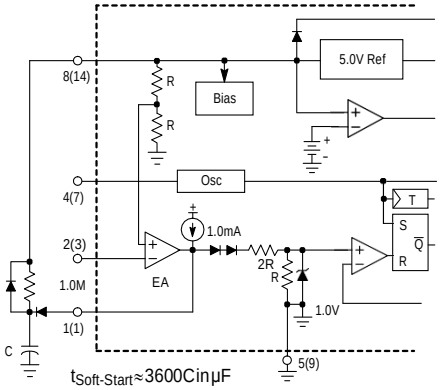


Figure 21. Soft−Start Circuit

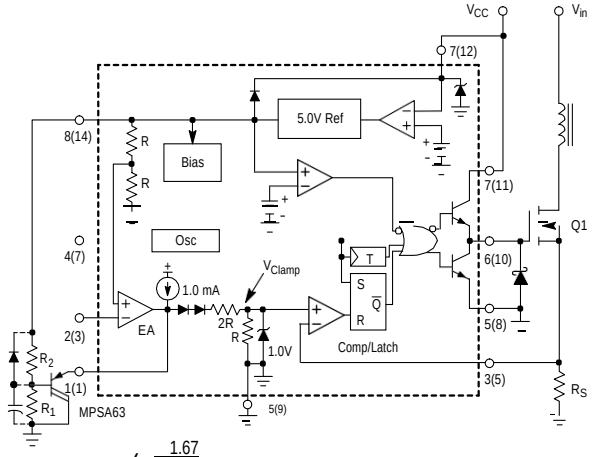
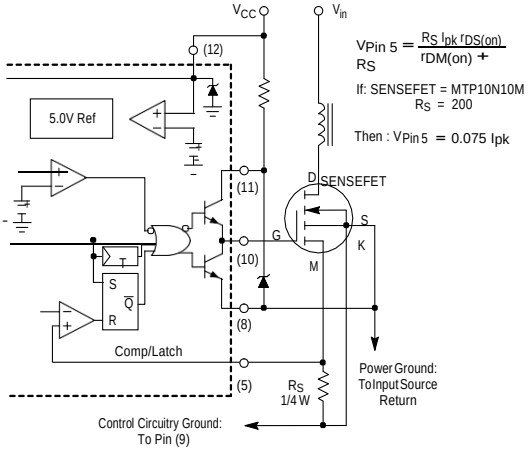


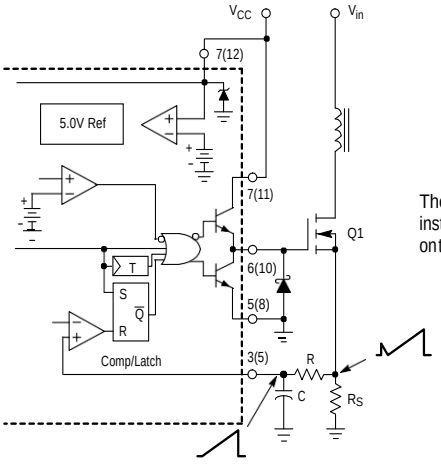
Figure 22. Adjustable Buffered Reduction of Clamp Level with Soft−Start



Virtually lossless current sensing can be achieved with the implementation of a SENSEFET

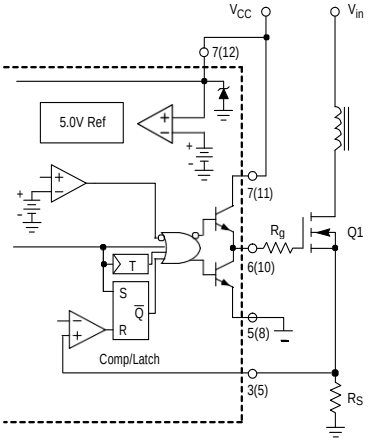
TM power switch. For proper operation during over-current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 20 and 22.

Figure 23. Current Sensing Power MOSFET



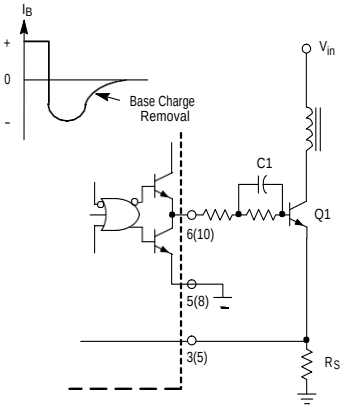
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 24. Current Waveform Spike Suppression



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

Figure 25. MOSFET Parasitic Oscillations



The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

Figure 26. Bipolar Transistor Drive

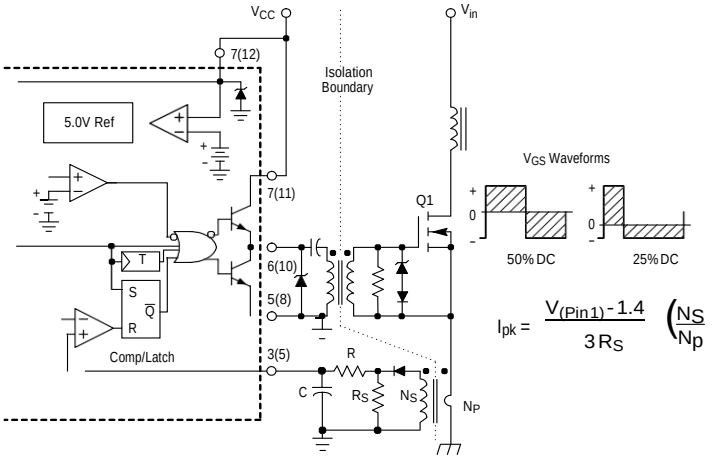
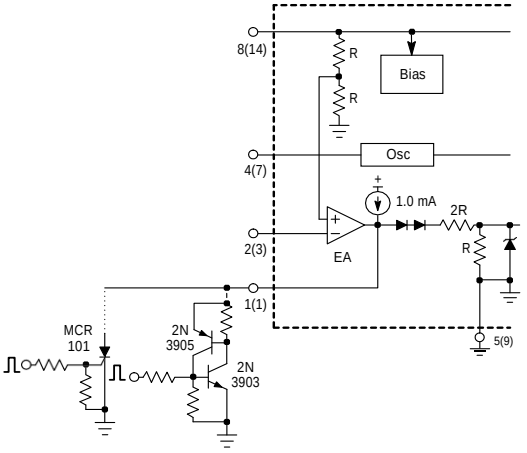
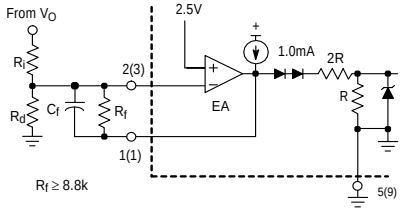


Figure 27. Isolated MOSFET Drive

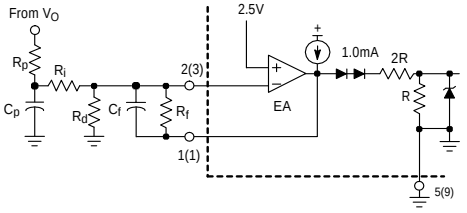


The MCR101 SCR must be selected for a holding of < 0.5 mA @ $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 28. Latched Shutdown

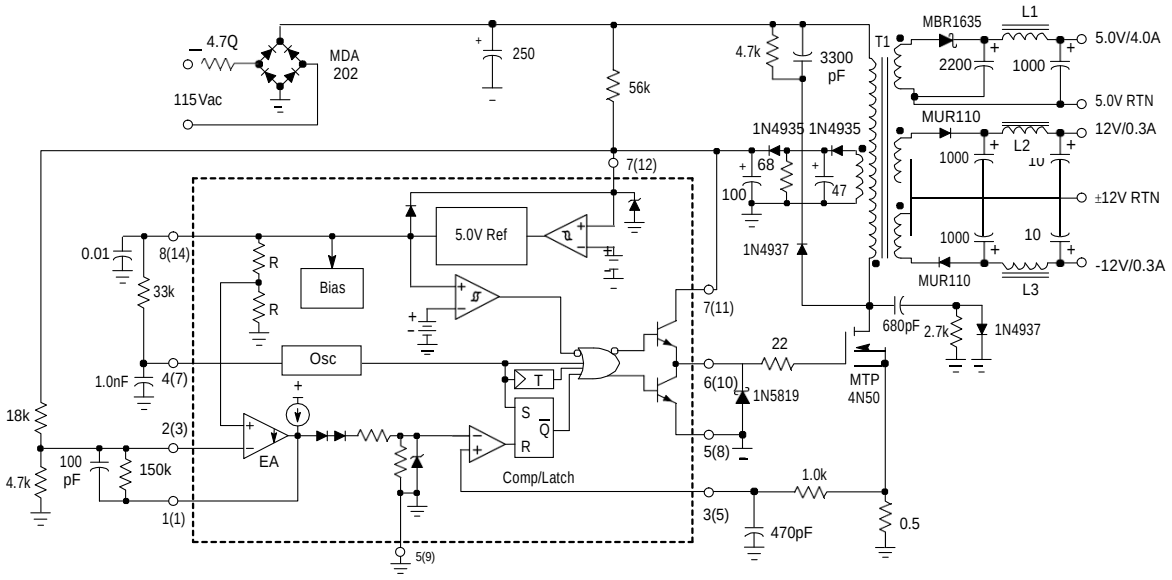


Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

Figure 29. Error Amplifier Compensation



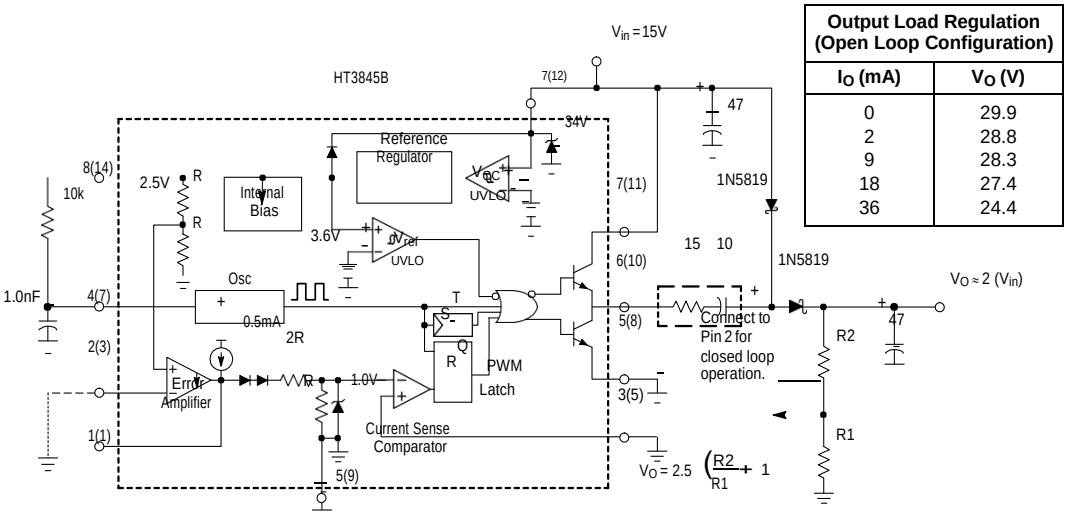
T1 - Primary: 45 Turns #26 AWG
Secondary ±12 V: 9 Turns #30 AWG (2 Strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands) #26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35-3C8
Bobbin: Ferroxcube EC35PCB1
Gap: ≈ 0.10" for a primary inductance of 1.0 mH

L1 - 15 μH at 5.0 A, Coilcraft Z7156
L2, L3 - 25 μH at 5.0 A, Coilcraft Z7157

Figure 30. 7 W Off–Line Flyback Regulator

Test	Conditions	Results
Line Regulation: 5.0 V ±12 V	V_{in} = 95 Vac to 130 Vac	M = 50 mV or ±0.5% M = 24 mV or ±0.1%
Load Regulation: 5.0 V ±12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	M = 300 mV or ±3.0% M = 60 mV or ±0.25%
Output Ripple: 5.0 V ±12 V	V_{in} = 115 Vac	40 mV_{pp} 80 mV_{pp}
Efficiency	V_{in} = 115 Vac	70%

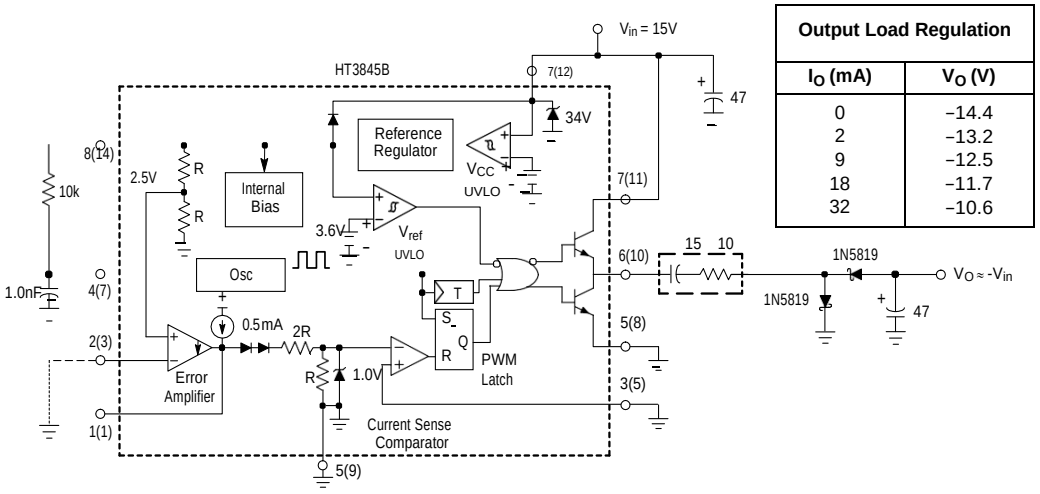
All outputs are at nominal load currents unless otherwise noted.



Output Load Regulation (Open Loop Configuration)	
I_O (mA)	V_O (V)
0	29.9
2	28.8
9	28.3
18	27.4
36	24.4

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The converter's output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

Figure 31. Step–Up Charge Pump Converter

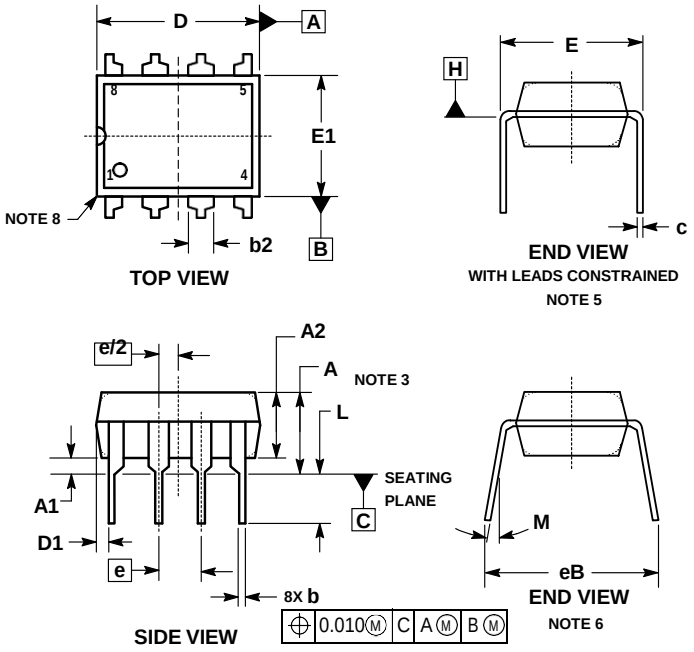


Output Load Regulation	
I_O (mA)	V_O (V)
0	−14.4
2	−13.2
9	−12.5
18	−11.7
32	−10.6

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A.
An additional series resistor may be required when using tantalum or other low ESR capacitors.

Figure 32. Voltage–Inverting Charge Pump Converter

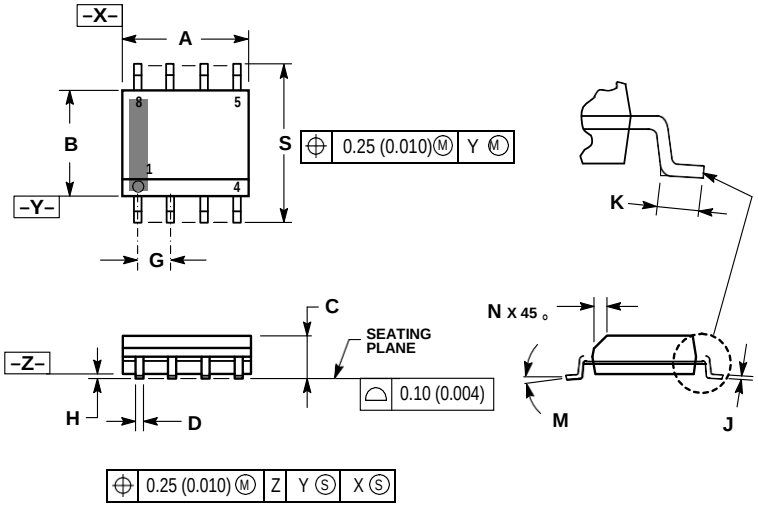
PDIP–8
N SUFFIX
CASE 626–05
ISSUE N



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION E3 IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10 °	---	10 °

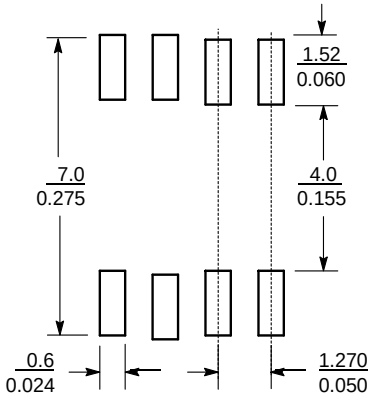
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0	8	0	8
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

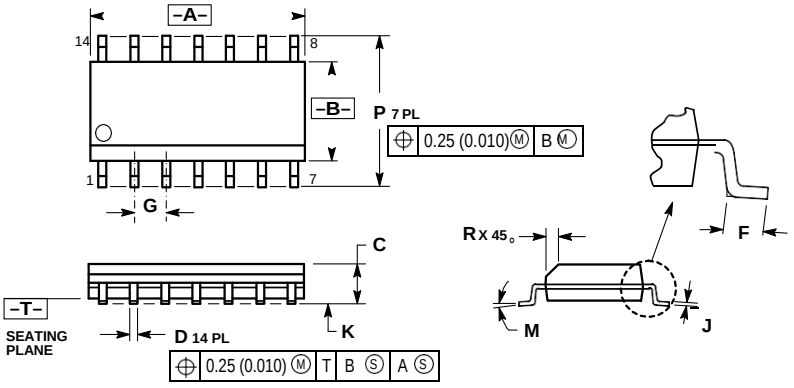
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOIC−14
CASE 751A−03
ISSUE H



NOTES:
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2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
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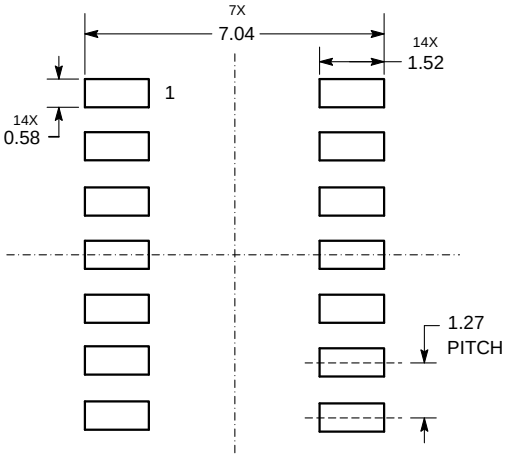
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT



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