

Current Mode PWM Control

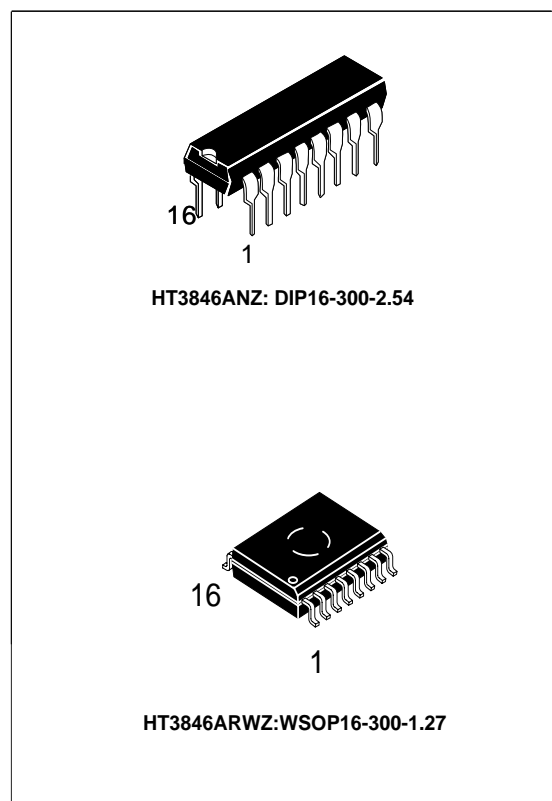
DESCRIPTION

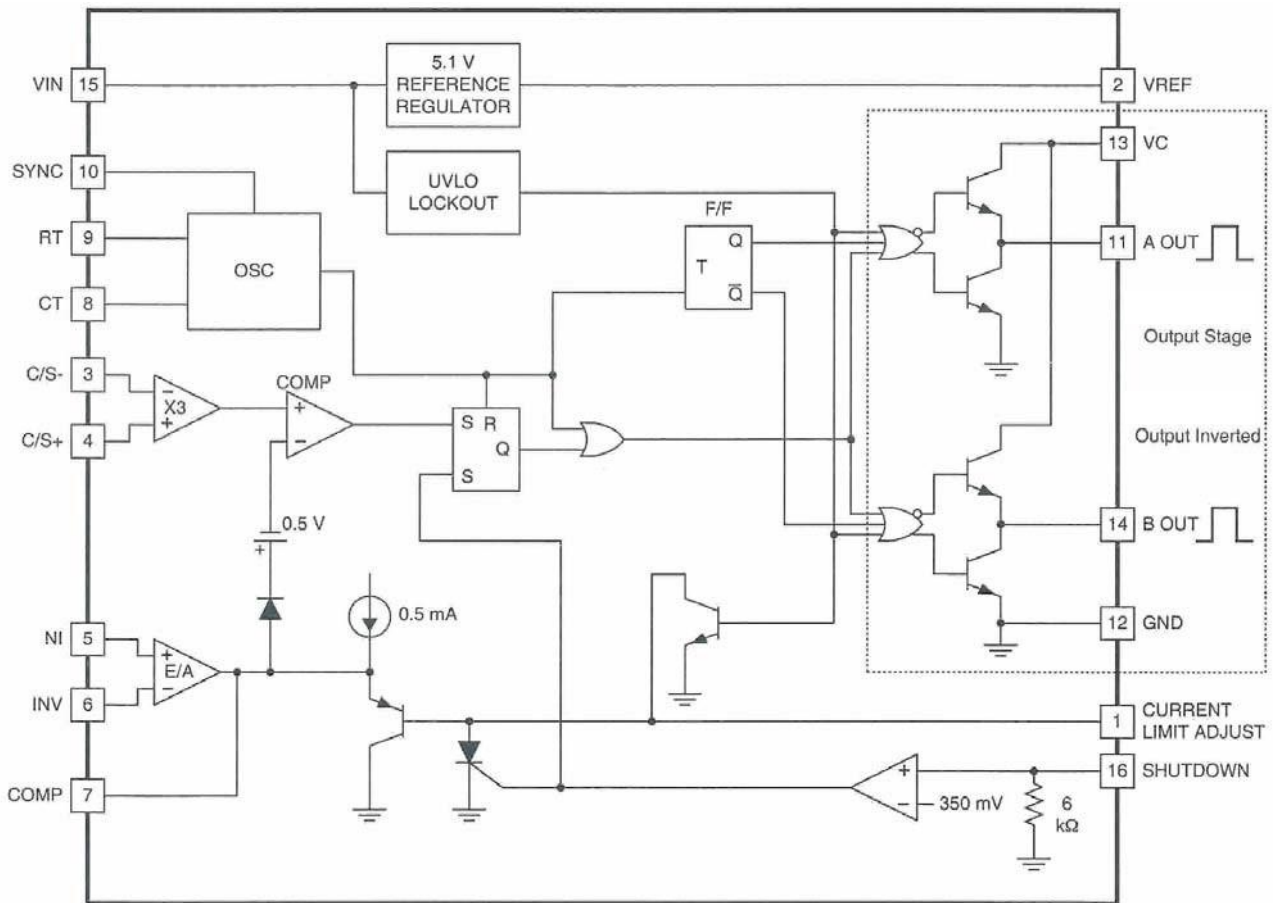
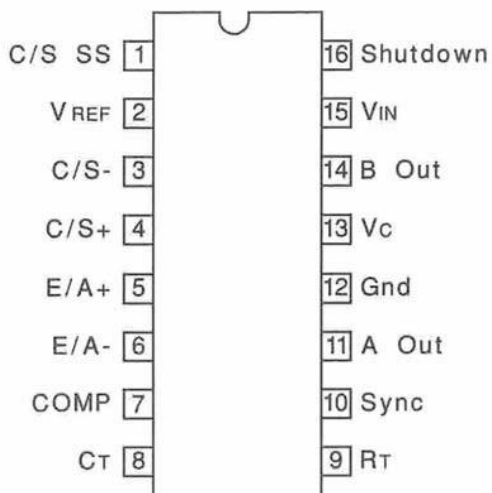
The HT3846A IC provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Other features include fully latched operation, double pulse suppression, deadline adjust capability, and a $\pm 1\%$ trimmed bandgap reference.

FEATURES

- Automatic Feed Forward Compensation
- Programmable Pulse-by-Pulse Current
- Automatic Symmetry Correction in Push-pull Configuration
- Enhanced Load Response Characteristics
- Parallel Operation Capability for Modular Power Systems
- Differential Current Sense Amplifier with Wide Common Mode Range
- Double Pulse Suppression
- 500mA (Peak) Totem-pole Outputs
- 1% Bandgap Reference
- Under-voltage Lockout
- Soft Start Capability
- Shutdown Terminal
- 500 kHz Operation



BLOCK DIAGRAM

PIN CONNECTION

PIN DESCRIPTION

PACKAGE PIN FUNCTION	
FUNCTION	PIN
C/S SS	1
V _{REF}	2
C/S-	3
C/S+	4
E/A+	5
E/A-	6
Comp	7
CT	8
RT	9
Sync	10
A Out	11
Gnd	12
V _C	13
B Out	14
V _{IN}	15
Shutdown	16

ABSOLUTE MAXIMUM RATINGS *

Characteristic		Limit	Unit
Supply voltage(pin 15)		40	V
Collector supply voltage(pin 13)		40	V
Output current,source or sink(pins 11,14)		500	mA
Analog inputs(pins 3,4,5,6,16)		-0.3 ~ +V _{IN}	V
Reference output current(pin 2)		-30	mA
Sync output current(pin 10)		-5	mA
Error amplifier output current(pin 7)		-5	mA
Soft start sink current(pin 1)		50	mA
Oscillator charging current(pin 9)		5	mA
Power dissipation	T _a =25 °C	1000	mW
	T _c =25 °C	2000	mW
Storage temperature range		-65 ~ +150	°C
Lead temperature (soldering, 10 seconds)		300	°C

Note 1. All voltages are with respect to Ground, Pin 13 . Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limits and considerations of packages. Pin numbers refer to DIL and SOIC packages only.

ELECTRICAL CHARACTERISTICS:

(Unless otherwise stated, these specifications apply for 0 °C to + 70 °C V_{IN} = 15V , R_T = 10 k, C_T = 4.7nF, T_A = T_J.)

Characteristic	Test conditions	Min.	Typ.	Max	Unit
Reference Section					
Output voltage	T _J = 25 °C, I _O = 1 mA	5.00	5.10	5.20	V
Line regulation	V _{IN} = 8V to 40V		5	20	mV
Load regulation	I _L = 1 mA to 10 mA		3	15	mV
Temperature stability	Over operating range *2		0.4		mV/ °C
Total output variation	Line, load and temperature *2	4.95		5.25	V
Output noise voltage	10Hz ≤ f ≤ 10kHz, T _J = 25 °C *2		100		μV
Long term stability	T _J = 25 °C, 1000 Hrs *2		5		mV
Short circuit output current	V _{REF} = 0V	-10	-45		mA

Continues:

Characteristic	Test conditions	Min.	Typ.	Max	Unit
Oscillator Section					
Initial accuracy	$T_J=25^\circ\text{C}$	39	43	47	kHz
Voltage stability	$V_{IN}=8\text{V to }40\text{V}$		-1	2	%
Temperature stability	Over operating range *2		-1		%
Sync output high level		3.9	4.35		V
Sync output low level			2.3	2.5	V
Sync input high level	Pin 8= 0V	3.9			V
Sync input low level	Pin 8= 0V			2.5	V
Sync input current	Sync voltage=3.9V, Pin 8=0V		1.3	1.5	mA
Error Amp Section					
Input offset voltage			0.5	10	mV
Input bias current			-0.6	-2	μA
Input offset current			40	250	nA
Common mode range	$V_{IN}=8\text{V to }40\text{V}$	0		$V_{IN}-2$	V
Open loop voltage gain	$\Delta V_o=1.2\text{V to }3\text{V}, V_{CM}=2\text{V}$	80	105		dB
Unity gain bandwidth	$T_J=25^\circ\text{C}$ *2	0.7	1.0		MHz
CMRR	$V_{CM}=0\text{V to }38\text{V}, V_{IN}=40\text{V}$	75	100		dB
PSRR	$V_{IN}=8\text{V to }40\text{V}$	80	105		dB
Output sink current	$V_{ID}=-15\text{ mV to }-5\text{V},$ $V_{PIN7}=1.2\text{V}$	2	6		mA
Output source current	$V_{ID}=15\text{ mV to }5\text{V}, V_{PIN7}=2.5\text{V}$	-0.4	-0.5		mA
High level output voltage	$R_L=(\text{Pin }7) 15\text{k}\Omega$	4.3	4.6		V
Low level output voltage			0.7	1	V
Current Sense Amplifier Section					
Amplifier gain	$V_{PIN3}=0\text{V}, \text{Pin }1 \text{ open}$ *3,4	2.5	2.75	3.0	V
Maximum differential input signal ($V_{PIN4}-V_{PIN3}$)	Pin 1 open *3 $R_L=(\text{Pin }7) 15\text{k}\Omega$	1.1	1.2		V
Input offset voltage	$V_{PIN1}=0.5\text{V}, \text{Pin}7 \text{ open}$ *3		5	25	mV
CMRR	$V_{CM}=1\text{V to }12\text{V}$	60	83		dB
PSRR	$V_{IN}=8\text{V to }40\text{V}$	60	84		dB
Input bias current	$V_{PIN1}=0.5\text{V}, \text{Pin}7 \text{ open}$ *3		-2.5	-10	μA
Input offset current	$V_{PIN1}=0.5\text{V}, \text{Pin}7 \text{ open}$ *3		0.08	1	μA
Input common mode range		0		$V_{IN}-3$	V
Delay to outputs	$T_J=25^\circ\text{C}$ *2		200	500	ns

Continues:

Characteristic	Test conditions	Min.	Typ.	Max	Unit
Current Limit Adjust Section					
Current limit offset	$V_{PIN3}=0V, V_{PIN4}=0V, Pin\ 7$ open *3	0.45	0.5	0.55	V
Input bias current	$V_{PIN5}=V_{REF}, V_{PIN6}=0V$		-10	-30	μA
Shutdown Terminal Section					
Threshold voltage		250	350	400	mV
Input voltage range		0		V_{IN}	V
Minimum latching current (I_{PIN1})	*6	3.0	1.5		mA
Shutdown Terminal Section (cont.)					
Maximum non-latching current (I_{PIN1})	*7		1.5	0.8	mA
Delay to outputs	$T_J=25\ ^\circ C$ *2		300	600	ns
Output Section					
Collector-emitter voltage		40			V
Collector leakage current	$V_C=40V$ *5			200	μA
Output low level	$I_{SINK}=20\ mA$		0.1	0.4	V
	$I_{SINK}=100\ mA$		0.4	2.1	V
Output high level	$I_{SOURCE}=20\ mA$	13	13.5		V
	$I_{SOURCE}=100\ mA$	12	13.5		V
Rise time	$C_L=1\ nF, T_J=25\ ^\circ C$ *2		50	300	ns
Fall time	$C_L=1\ nF, T_J=25\ ^\circ C$ *2		50	300	ns
Under-Voltage Lockout Section					
Start-up threshold			7.7	8.0	V
Threshold hysteresis			0.75		V
Total Standby Current					
Supply current			17	21	mA

*2. These parameters, although ensured over the recommended operating conditions, are not 100% tested in production.

*3. Parameter measured at trip point of latch with $V_{PIN5}=V_{REF}; V_{PIN6}=0V$

$$G = \frac{\Delta V_{PIN7}}{\Delta V_{PIN4}}$$

*4. Amplifier gain defined as: $\Delta V_{PIN4}; V_{PIN4}=0$ to $1.0V$

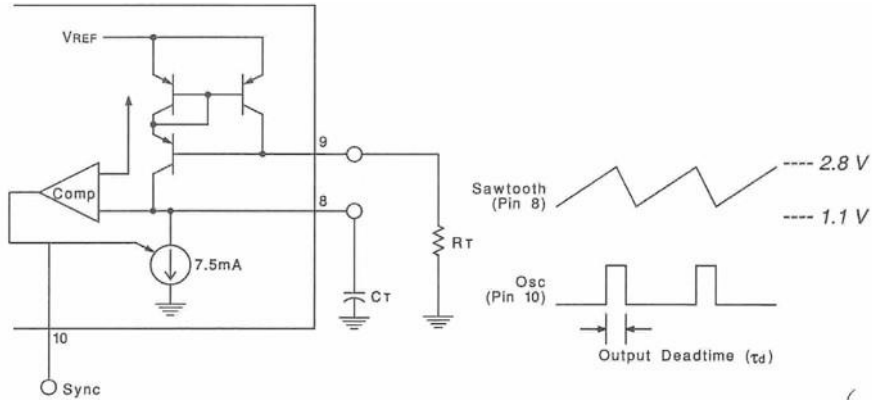
*5. Applies to HT3846A only due to polarity of outputs

*6. Current into Pin1 ensured to latch circuit in shutdown state.

*7. Current into Pin1 ensured not to latch circuit in shutdown state.

APPLICATION DATA

Oscillator Circuit

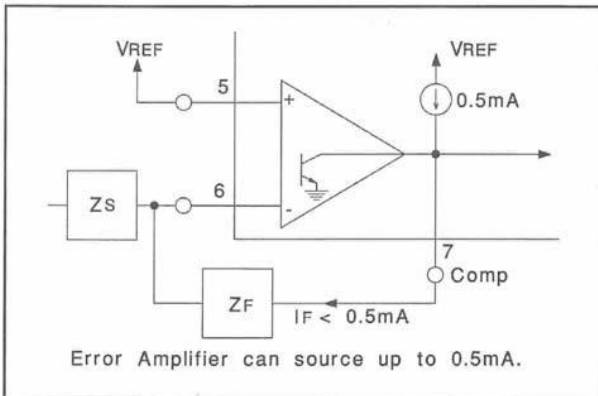


Output deadtime is determined by the external capacitor, C_T , according to the formula: $\tau_d (\mu s) = 145 C_T (\mu f) \left(\frac{I_D}{I_D - \frac{3.6}{RT (k\Omega)}} \right)$.

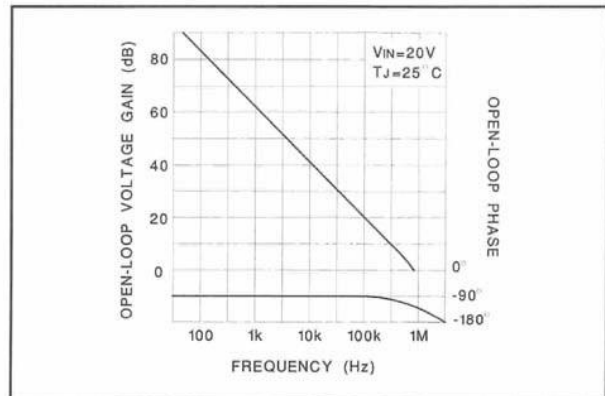
I_D = Oscillator discharge current at 25°C is typically 7.5.
 For large values of R_T : $\tau_d (\mu s) \approx 145 C_T (\mu f)$.

Oscillator frequency is approximated by the formula: $f_T (kHz) = \frac{2.2}{RT (k\Omega) \cdot C_T (\mu f)}$.

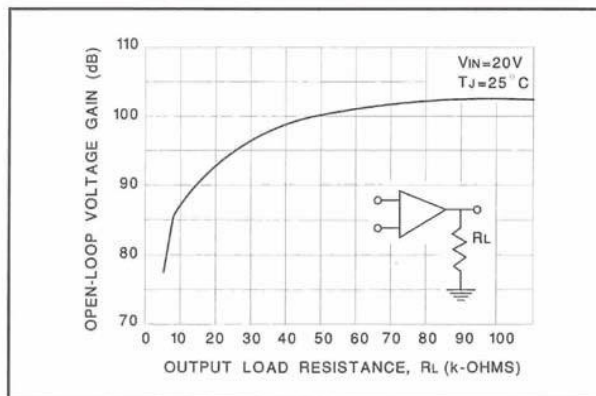
Error Amp Output Configuration

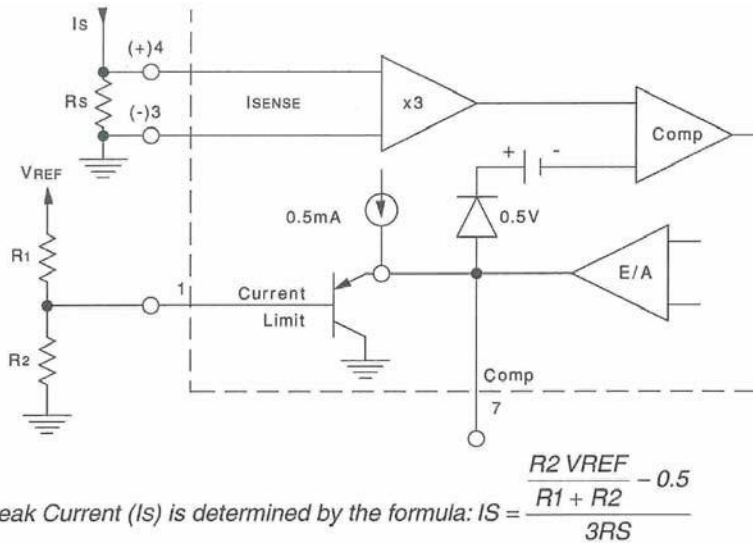
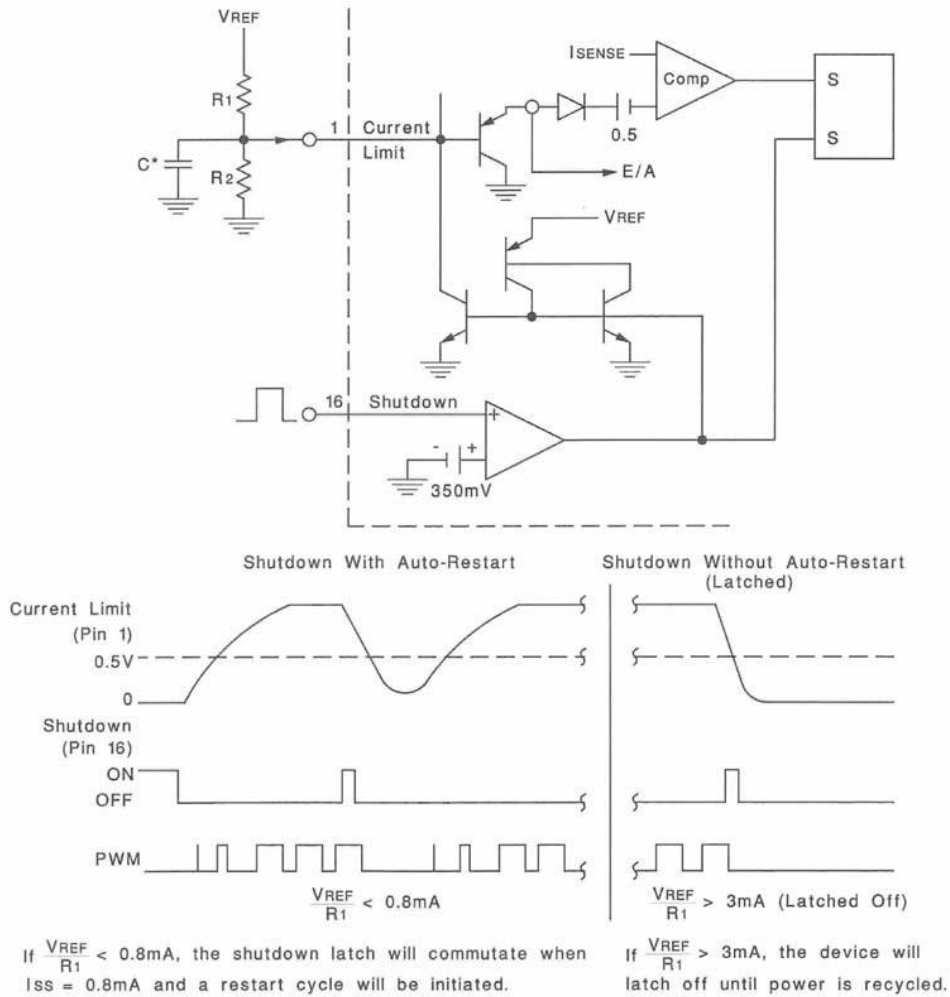


Error Amp Gain and Phase vs Frequency

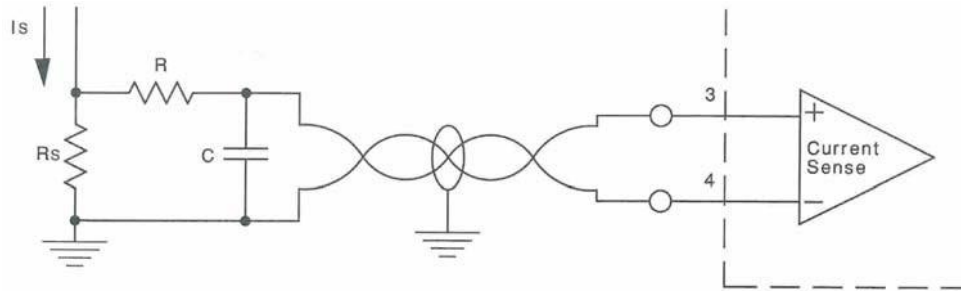


Error Amp Open-Logic D.C. Gain vs Load Resistance



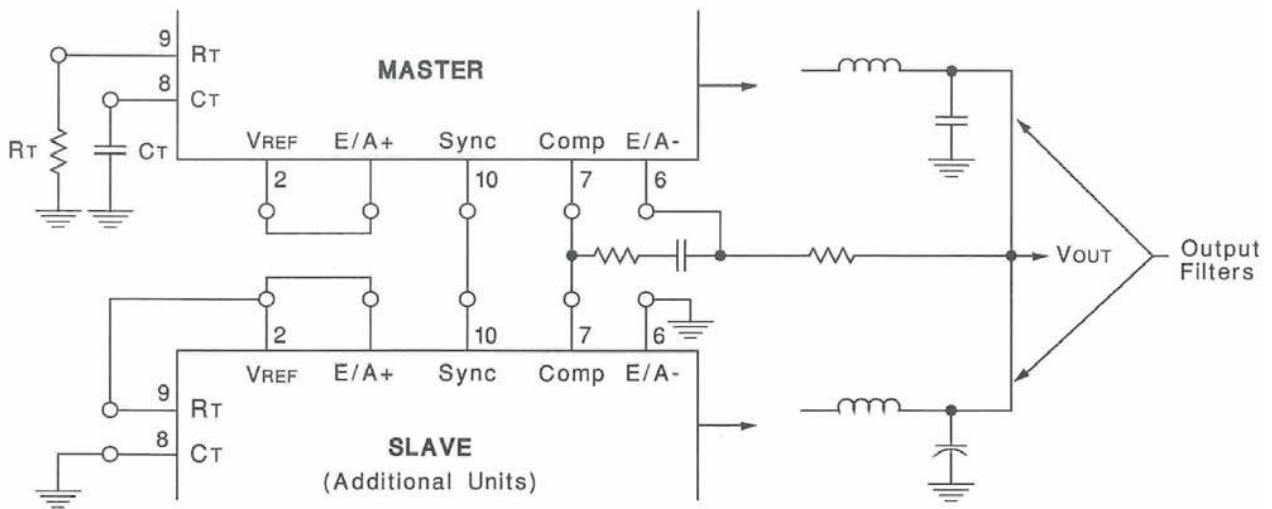
Pulse by Pulse Current Limiting

Soft Start and Shutdown/Restart Function


Current Sense Amp Connection

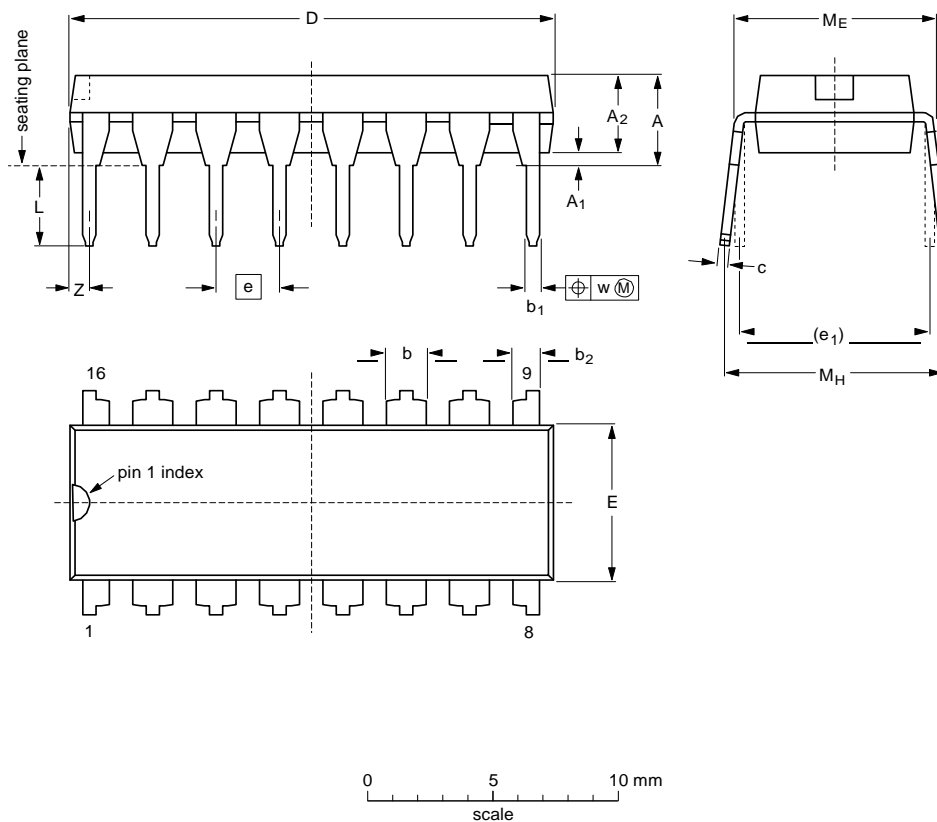


A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise free sensing.

Parallel Operation




Slaving allows parallel operation of two or more units with equal current sharing.

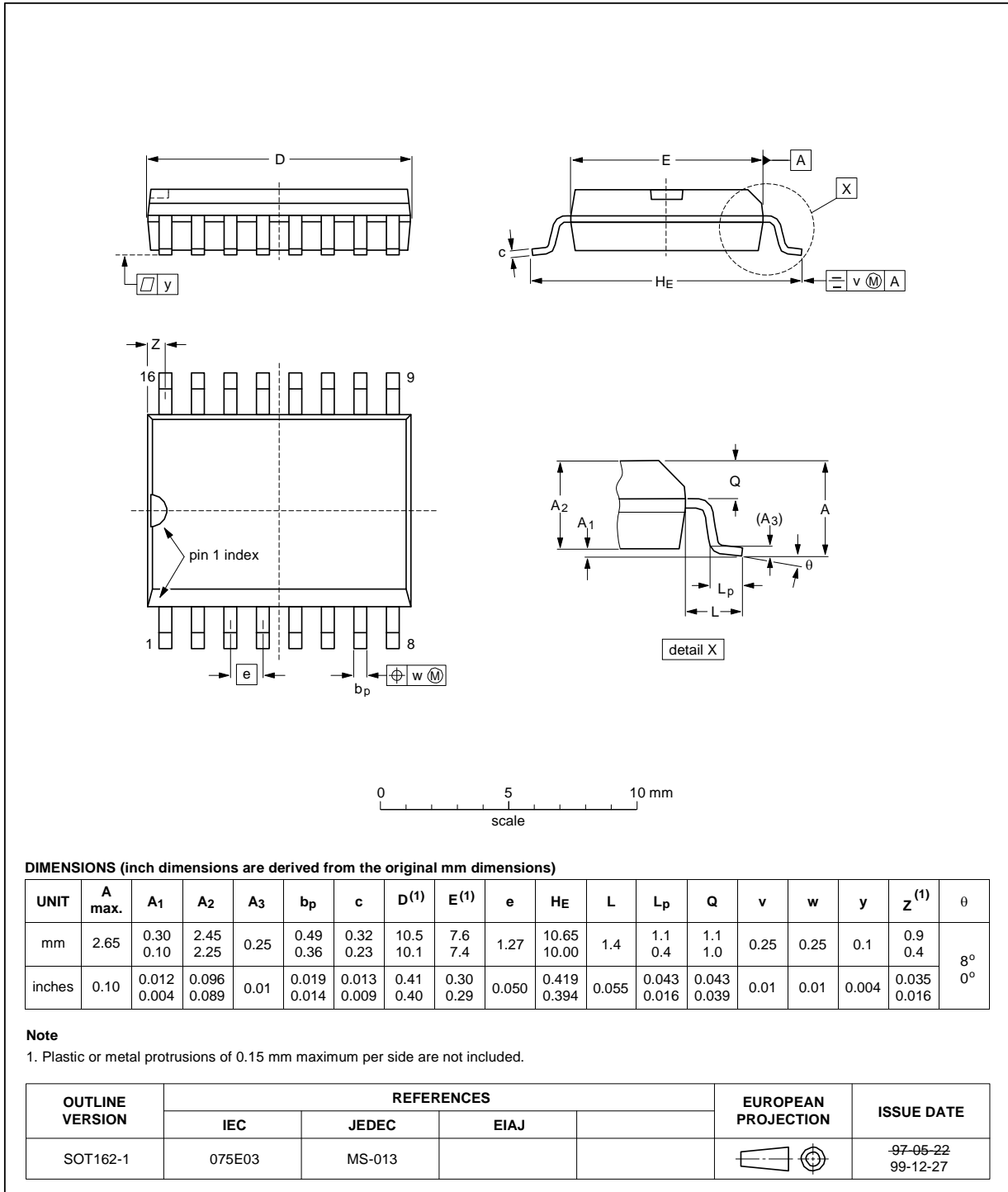
OUTLINE DRAWING
DIP16: plastic dual in-line package; 16 leads (300 mil)

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

OUTLINE DRAWING
WSOP16: plastic small outline package; 16 leads; body width 7.5 mm


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