

Dual 4-Bit Static Shift Register

The HT4015A dual 4-bit static shift register is constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-state serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. These complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design
- Logic State is Retained Indefinitely with Clock Level either High or Low; Information is Transferred to the Output only on the Positive-going Edge of the Clock Pulse
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

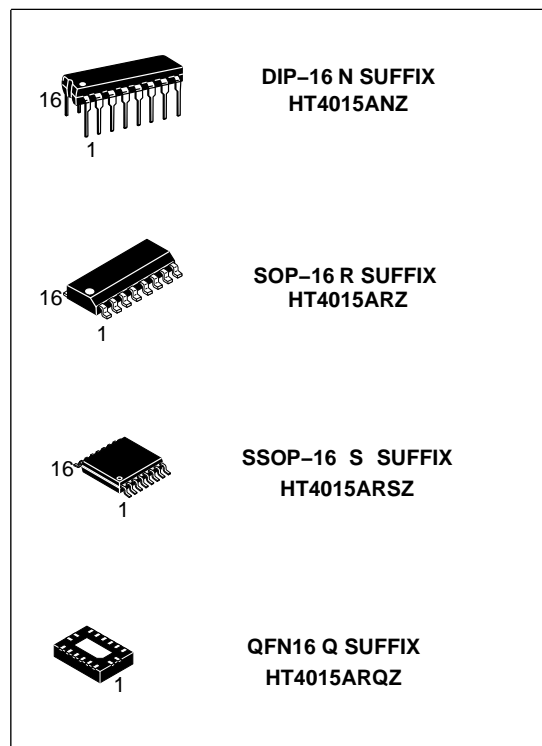
MAXIMUM RATINGS (Voltages Referenced to V_{SS})

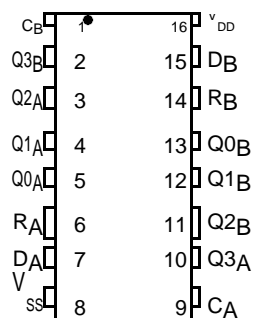
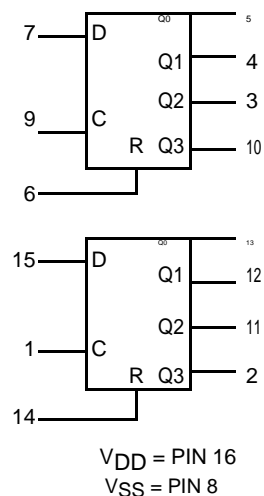
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Package: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.



PIN ASSIGNMENT

BLOCK DIAGRAM

TRUTH TABLE

C	D	R	Q0	Q _n
↗	0	0	0	Q _{n-1}
↗	1	0	1	Q _{n-1}
↘	X	0	No Change	No Change
X	X	1	0	0

X = Don't Care

Q_n = Q0, Q1, Q2, or Q3, as applicable.

Q_{n-1} = Output of prior stage.

ORDERING INFORMATION

Device	Package	Shipping [†]
HT4015ADG	SOIC-16 (Pb-Free)	48 Units / Rail
HT4015ADR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14015BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	-55_C		25_C			125_C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0	“0” Level V_{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
		10	-	0.05	-	0	0.05	-	0.05	
$V_{in} = 0$ or V_{DD}	“1” Level V_{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
		10	9.95	-	9.95	10	-	9.95	-	
Input Voltage ($V_O = 4.5$ or $.05$ Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	“0” Level V_{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
		10	-	3.0	-	4.50	3.0	-	3.0	
($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	“1” Level V_{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
		10	7.0	-	7.0	5.50	-	7.0	-	
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	Source I_{OH}	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	Sink I_{OL}	10	-1.6	-	-1.3	-2.25	-	-0.9	-	mAdc
		15	-4.2	-	-3.4	-8.8	-	-2.4	-	
Input Current	I_{in}	15	-	± 0.1	-	± 0.00001	± 0.1	-	± 1.0	mAdc
Input Capacitance ($V_{in} = 0$)	C_{in}	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)	I_{DD}	5.0	-	5.0	-	0.005	5.0	-	150	mAdc
		10	-	10	-	0.010	10	-	300	
		15	-	20	-	0.015	20	-	600	
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.2 \text{ mA/kHz})f + I_{DD}$ $I_T = (2.4 \text{ mA/kHz})f + I_{DD}$ $I_T = (3.6 \text{ mA/kHz})f + I_{DD}$							mAdc
		10								
		15								

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
- The formulas given are for the typical characteristics only at 25_C.
- To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in mA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.002$.

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25_{\text{C}}$)

Characteristic	Symbol	V_{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}^{\uparrow} t_{THL}^{\downarrow}	5.0 10 15	- - -	100 50 40	200 100 80	ns
Propagation Delay Time Clock, Data to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 225 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$ Reset to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 375 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 147 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 95 \text{ ns}$	t_{PLH}^{\uparrow} t_{PHL}^{\downarrow}	5.0 10 15 5.0 10 15	- - - - - -	310 125 90 460 180 120	750 250 170 750 250 170	ns
Clock Pulse Width	t_{WH}	5.0 10 15	400 175 135	185 85 55	- - -	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	- - -	2.0 6.0 7.5	1.5 3.0 3.75	MHz
Clock Pulse Rise and Fall Times	t_{TLH}^{\uparrow} t_{THL}^{\downarrow}	5.0 10 15	- - -	- - -	15 5 4	ms
Reset Pulse Width	t_{WH}	5.0 10 15	400 160 120	200 80 60	- - -	ns
Setup Time	t_{su}	5.0 10 15	350 100 75	100 50 40	- - -	ns

5. The formulas given are for typical characteristics only at 25_C.

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

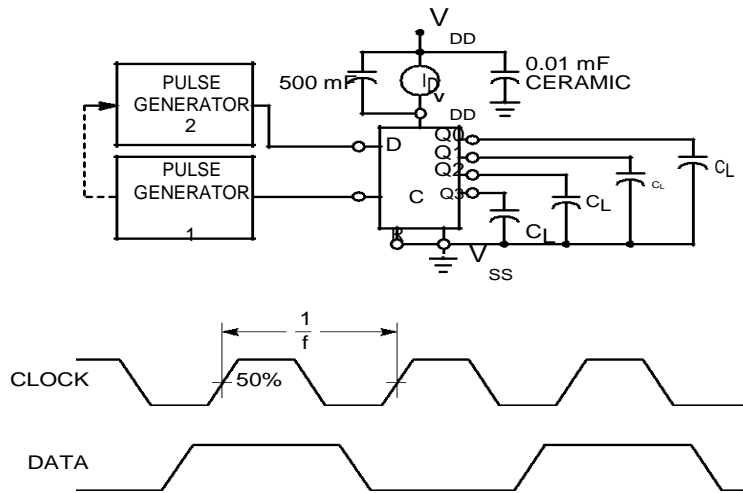


Figure 1. Power Dissipation Test Circuit and Waveform

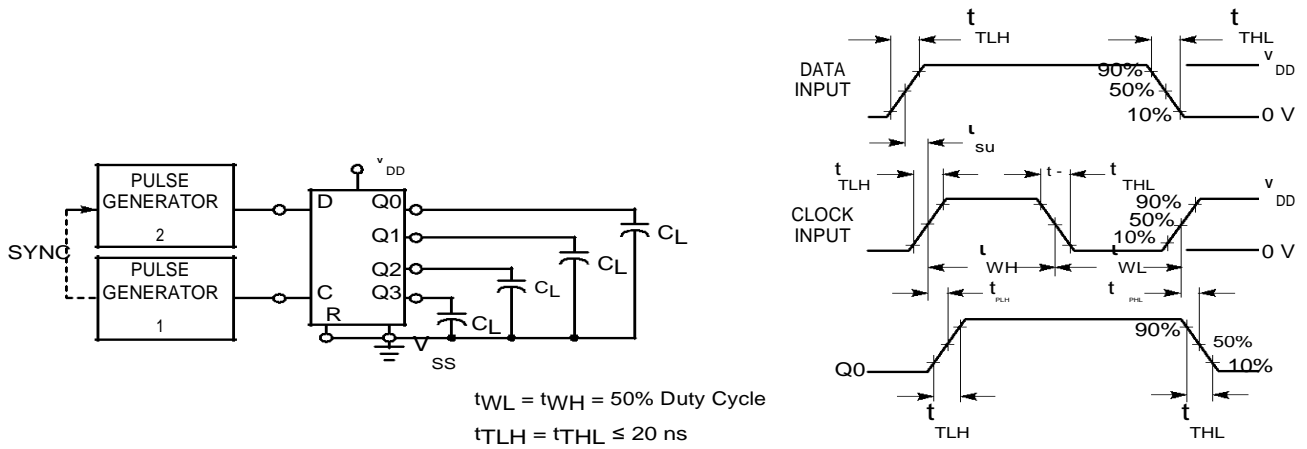


Figure 2. Switching Test Circuit and Waveforms

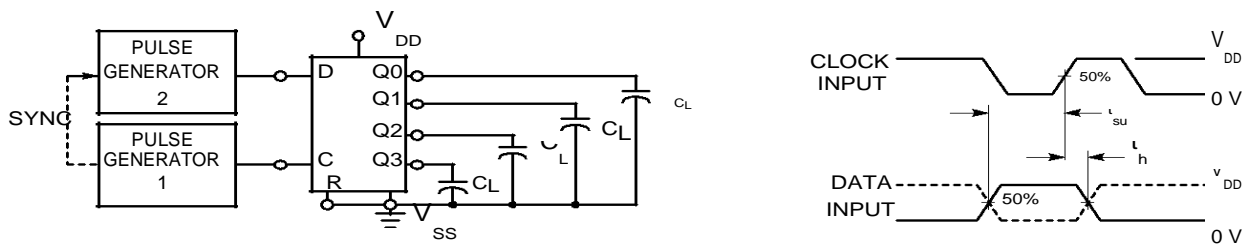
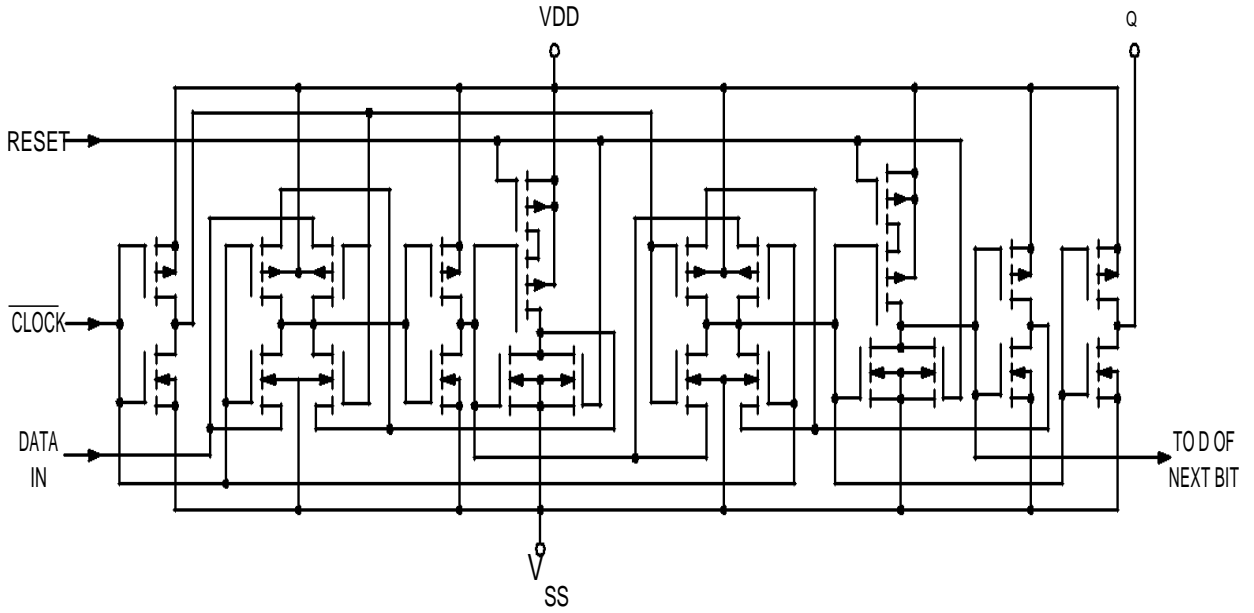
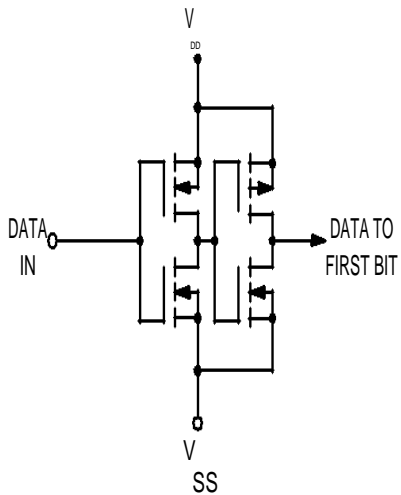


Figure 3. Setup and Hold Time Test Circuit and Waveforms

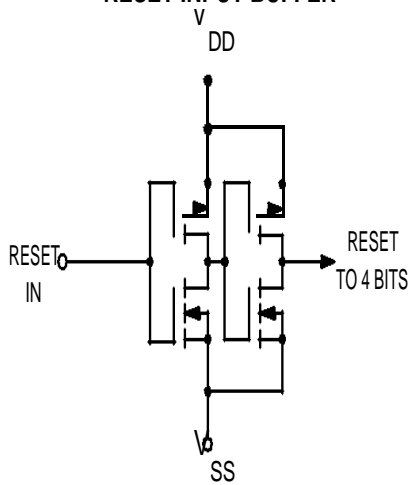
SINGLE BIT



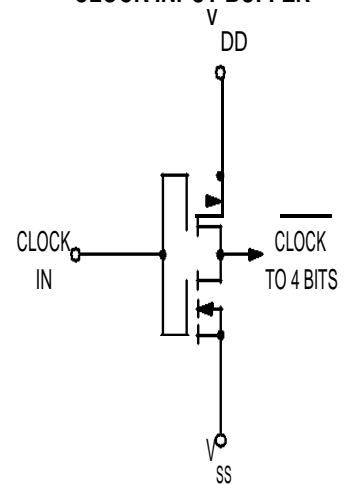
DATA INPUT BUFFER



RESET INPUT BUFFER

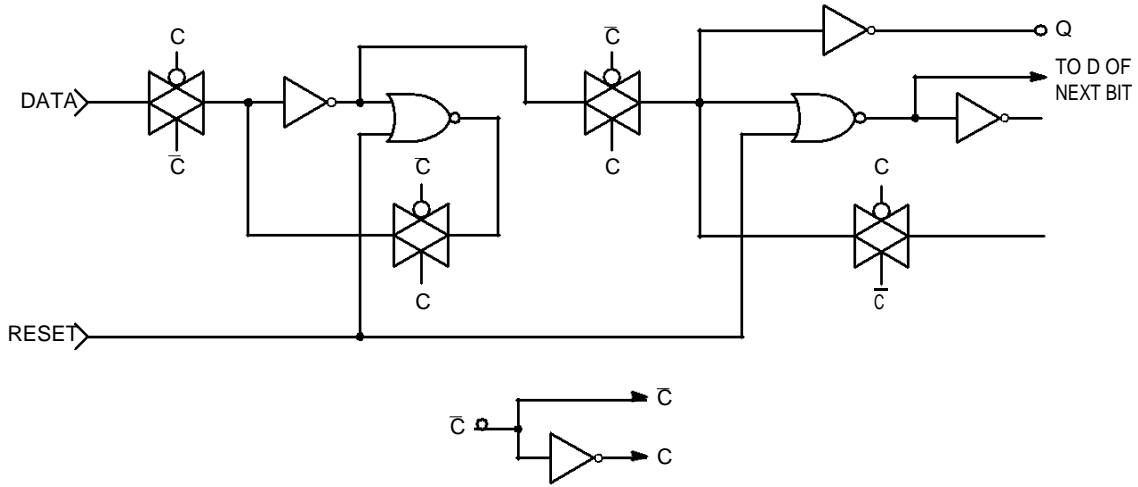


CLOCK INPUT BUFFER

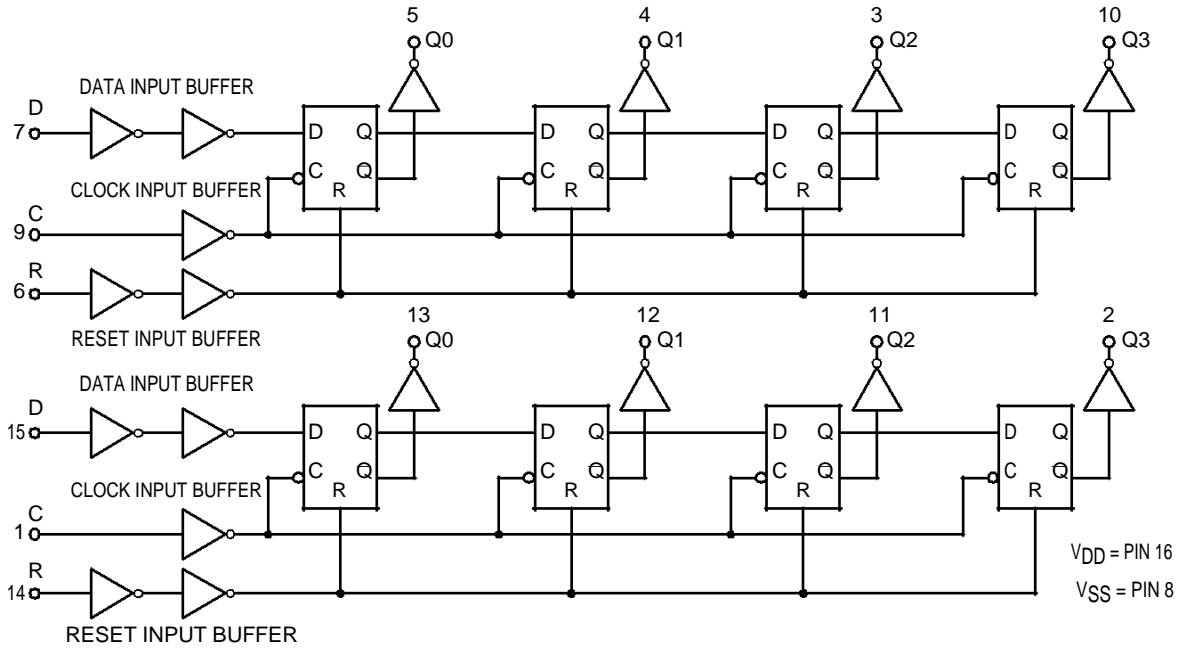


LOGIC DIAGRAMS

SINGLE BIT



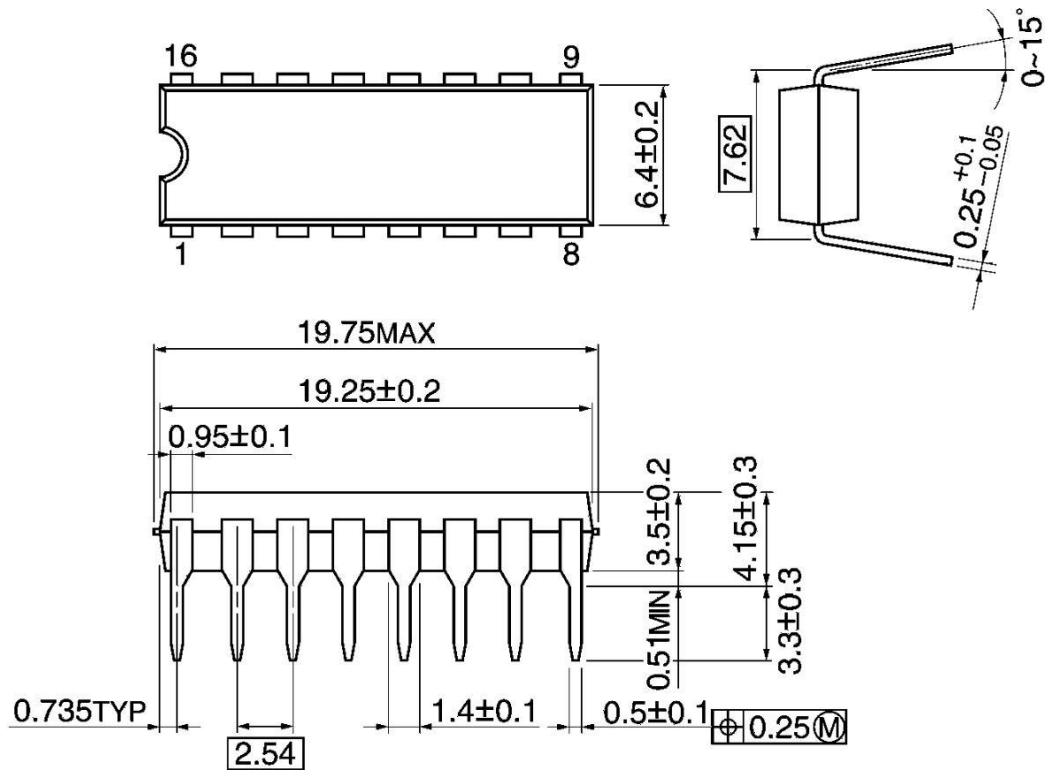
COMPLETE DEVICE



Package Dimensions

DIP16-P-300-2.54A

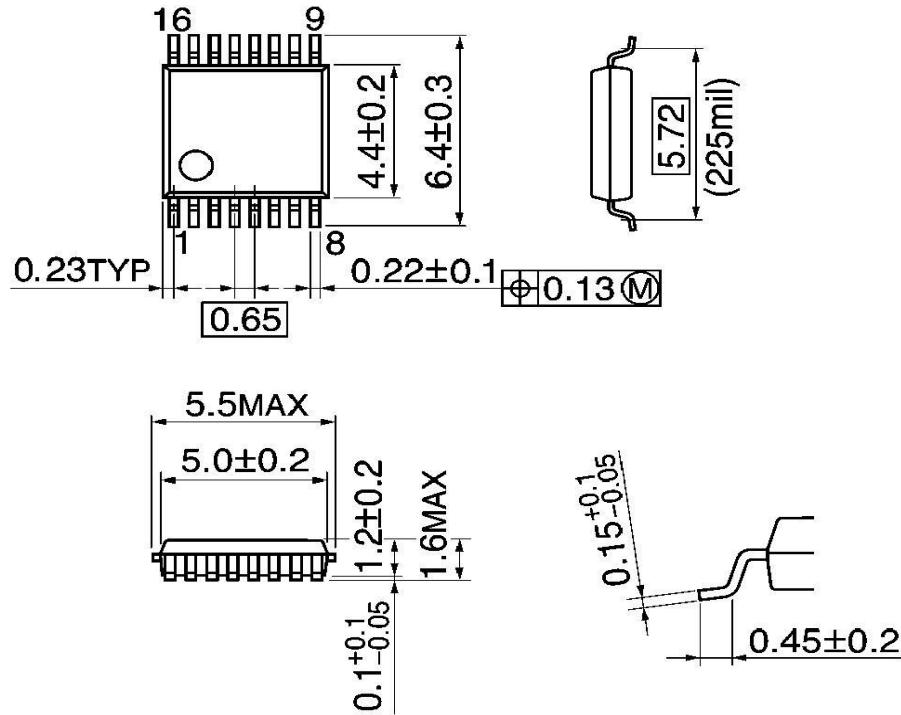
Unit: mm



Weight: 1.11 g (Typ.)

SSOP16-P-225-0.65B

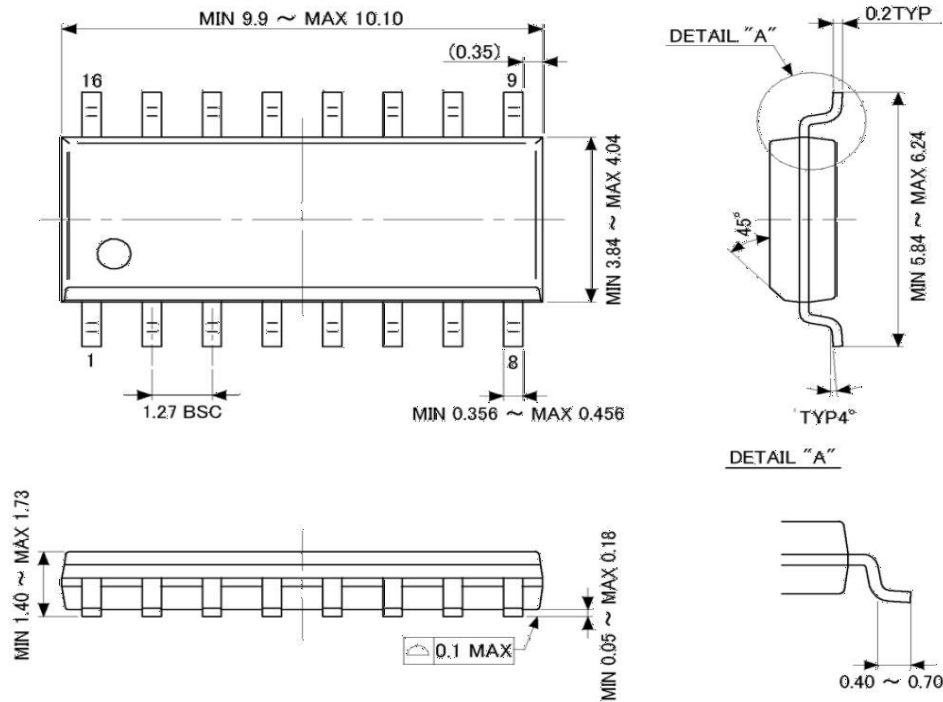
Unit: mm



Weight: 0.07 g (Typ.)

P-SOP16-0410-1.27-002

Unit: mm



Weight: 0.15 g (Typ.)

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