

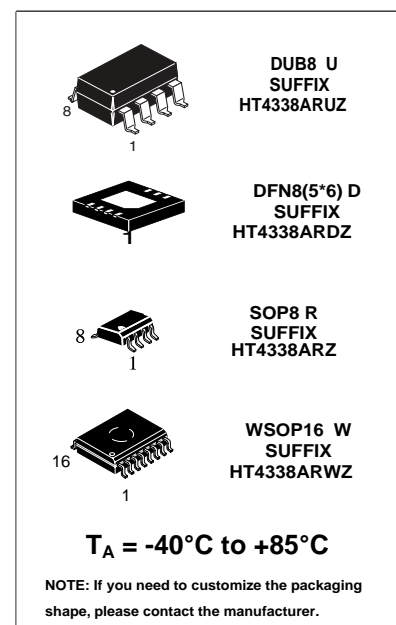
CMOS IC of Real Time Watch with Serial Interface, 56 X 8 RAM

General Description

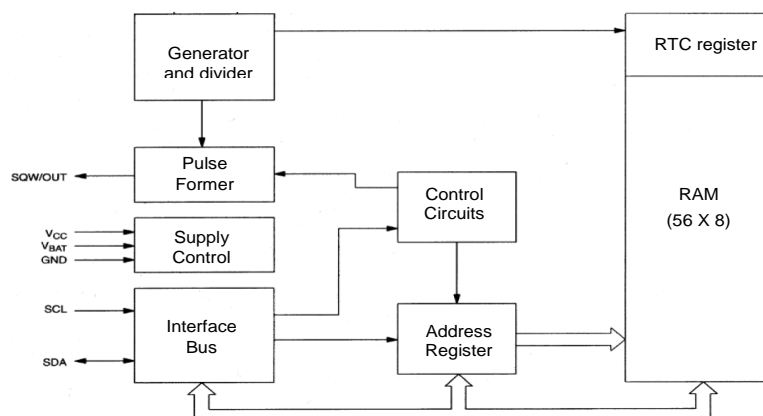
HT4338 is essentially the binary – decimal digital watch with a calendar, it has the additional 56 bytes of the power self-sufficient static RAM and possesses the low power consumption. The addresses and data are applied consecutively via the two-wire bi-directional bus. The microcircuit is intended for count of the real time in hours, minutes and seconds, count of week days, date, month and year. The last day of the month is automatically adjusted for the months of less, than 31 days, including correction for the leap year. The watches function in the 24-hour format or in the 12-hour format with the AM / PM-indicator. HT4338 has the built-in power supply control circuit, which determines the supply disruption and automatically switches over the device into the battery mode.

Functions and Features

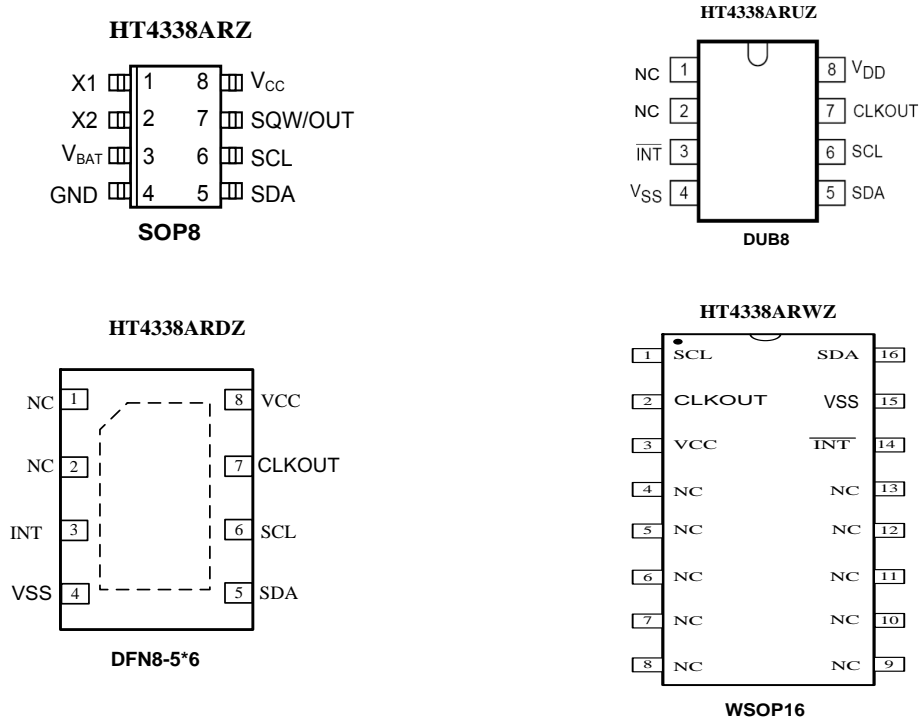
- Count of seconds, minutes, hours, week days, date, months and years with consideration of the leap years (before 2100);
- 56 bytes of the power self-sufficient RAM for the data storage;
- Two-wire consecutive interface;
- Programmable rectangular output signal;
- Automatic determination of the supply voltage drop and the switching diagram;
- Consumption of less than 500 nA in the back-up supply mode with the operating generator;
- Temperature range of the industrial application: -40°C – +85°C.
- **The HT4338ARWZ version has an internal integrated oscillator; No need for external crystal oscillator..**



Block Diagram



Pin Configuration and Functions



NAME	FUNCTION
X1 X2	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C _L) of 12.5pF. X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, X2, is floated if an external oscillator is connected to X1.
V _{BAT}	Backup Supply Input for Any Standard 3V Lithium Cell or Other Energy Source. Battery voltage must be held between the minimum and maximum limits for proper operation. Diodes in series between the battery and the V _{BAT} pin may prevent proper operation. If a backup supply is not required, V _{BAT} must be grounded. The nominal power-fail trip point (V _{PF}) voltage at which access to the RTC and user RAM is denied is set by the internal circuitry as 1.25 x V _{BAT} nominal. A lithium battery with 48mAh or greater will back up the HT4338 for more than 10 years in the absence of power at +25°C. UL recognized to ensure against reverse charging current when used with a lithium battery.
GND	Ground
SDA	Serial Data Input/Output. SDA is the data input/output for the I ² C serial interface. The SDA pin is open drain and requires an external pullup resistor.
SCL	Serial Clock Input. SCL is the clock input for the I ² C interface and is used to synchronize data movement on the serial interface.
SQW/OUT	Square Wave/Output Driver. When enabled, the SQWE bit set to 1, the SQW/OUT pin outputs one of four square-wave frequencies (1Hz, 4kHz, 8kHz, 32kHz). The SQW/OUT pin is open drain and requires an external pullup resistor. SQW/OUT operates with either V _{CC} or V _{BAT} applied.
V _{CC}	Primary Power Supply. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and V _{CC} is below V _{TP} , read and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.

Operating Temperatures Range

Operating temperatures range of the microcircuit HT4338: $T_A = -40 \dots +85 \text{ }^\circ\text{C}$.

Limit Mode and limit permissible operational

Description, Unit	Symbol	Norm			
		Limit Permissible		Limit	
		min	max	min	max
Supply voltage, V	V_{CC}	4.5	5.5	-0.5	7.0
Battery voltage, V	V_{BAT}	2.0	3.5	-0.5	7.0
Low level input voltage, V	V_{IL}	-0.3	0.8	-0.5	7.0
High level input voltage, V	V_{IH}	2.2	$V_{CC} + 0.3$	-0.5	7.0
Storage temperature, $^\circ\text{C}$	T_S	-	-	-55	+125

All voltages are indicated relative to ground. Under influence of the limit mode serviceability of the microcircuits is not guaranteed. After measuring the limit mode serviceability is guaranteed in the limit permissible mode.

Electric Parameters ($T_A = -40 \dots +85 \text{ }^\circ\text{C}$ $V_{CC} = 4.5 - 5.5 \text{ V}$)

Description, Unit	Symbol	Condition	Norm	
			min	max
Input leakage current, μA (SCL only)	I_{LI}	-	-	1
In / Out leakage current, μA (SDA and SQW/OUT)	I_{LO}	-	-	1
Low level output voltage, V	$V_{OL}^{1)}$	$V_{CC} = 4.5 \text{ V}$	-	0.4
Consumption current in the data transfer mode, μA	I_{CCA}	$f_{SCL} = 100 \text{ kHz}$	-	1500
Consumption current in the static mode, μA	I_{CCS}	$V_{CC} = 5 \text{ V}$ and SDA, SCL = 5 V	-	200
Consumption current in the battery mode (SQW/OUT OFF., 32 kHz – ON), μA	I_{BAT1}	$V_{CC} = 0 \text{ V}$, $V_{BAT} = 3 \text{ V}$	-	0.5
Consumption current in the battery mode (SQW/OUT – ON, 32 kHz – ON), μA	I_{BAT2}	$V_{CC} = 0 \text{ V}$, $V_{BAT} = 3 \text{ V}$	-	0.8

Low level voltage is determined under the load current of 5 mA; $V_{OL} = \text{GND}$ under the capacitance load

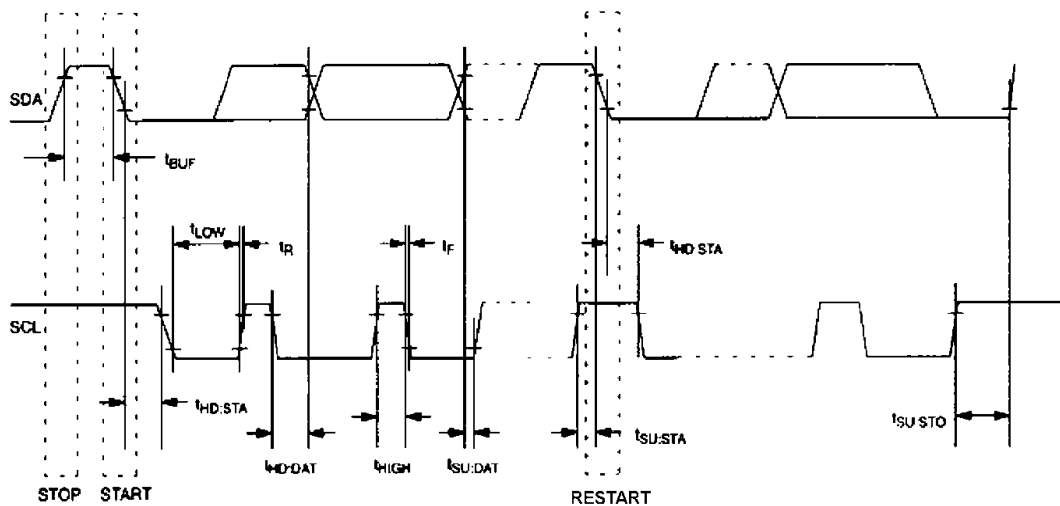
Dynamic Parameters ($T_A = -40...+85^\circ\text{C}$, $V_{CC} = 4.5 - 5.5\text{ V}$)

Description, Unit	Symbol	Condition	Norm	
			Not less	Not more
Cycle frequency SCL, kHz	f_{SCL}	–	0	100
Time of the bus vacant status between the statuses of STOP and START, μsec	t_{BUF}	–	4.7	–
Hold time (repeated) of START status, μsec	$t_{HD:STA}^{1)}$	–	4.0	–
Duration of the low status of the cycle pulse SCL, μsec	t_{LOW}	–	4.7	–
Duration of the cycle pulse high status SCL, μsec	t_{HIGH}	–	4.0	–
Pre-set time for the repeated status START, μsec	$t_{SU:STA}$	–	4.7	–
Data hold time, μsec	$t_{HD:DAT}^{2)}$	–	0	–
Data pre-set time, nsec	$t_{SU:DAT}$	–	250	–
Rise time of signals SDA and SCL, nsec	t_R	–	–	1000
Drop time of signals SDA and SCL, nsec	t_F	–	–	300
Pre-set time for the status STOP, μsec	$t_{SU:STO}$	–	4.7	–
Total capacitance load per each bus line, pF	C_B	–	–	400
IN / OUT capacitance, pF	$C_{I/O}$	–	10	10
Load capacitance of the quartz resonator, pF	C_{LX}	–	12.5	12.5

After this time interval the first time cycle signal is formed;

Device should internally ensure the hold time, at least, 300 nsec for the signal SDA (relative to V_{IHMIN} of signal SCL) in order to overlap the indeterminacy area of the fall signal of SCL.

maximum value $t_{HD:DAT}$ should be definite in that case, if the device does not increase duration of the low status (t_{LOW}) of signal SCL.

Timing Chart


Function Description

HT4338 operates as the driven device on the serial bus. For access to it it is required to set the status START and to send after the register address the device identification code. It is possible to address the next register consequently, until the status STOP is set. When V_{CC} drops below $1.25 \times V_{BAT}$, the access in progress to the device is ceased and the address counter is reset. At this time the device does not recognize the input data, excluding the erroneous information writing. When V_{CC} drops below V_{BAT} , the device switches over to the battery mode, consuming low power. When switching on the power supply V_{CC} above $V_{BAT} + 0.2 \text{ V}$, the device switches over from the battery power supply to V_{CC} ; and recognizes the input data, when V_{CC} becomes above $1.25 \times V_{BAT}$.

Addresses Chart of RTC and RAM

Addresses chart of the registers RTC and RAM is indicated in the Figure. Hour registers of the real time are positioned at the addresses 00h – 07h. RAM registers are positioned at the addresses of 08h – 3Fh. In the mode of the multi-byte access, when reaching by the pointer of the address 3Fh, the end of the RAM address space, there happens transition to the register with the address 00h, beginning of the hour area.

00H	SECONDS
	MINUTES
	HOURS
	DAY
	DATE
	MONTH
	YEAR
07H	CONTROL
08H	RAM
3FH	56 x 8

Hours and Calendar

Information on the time and date is obtained by means of reading the appropriate register bytes. Hour registers of the real time are indicated in the Figure. Pre-setting and time and calendar initialization are performed by means of writing the appropriate bytes. Information, contained in the time and calendar registers, represents the binary-decimal code. Bit 7 of register 0 represents the hour stop bit (CH). When this bit is set to "1", the generator is off.

When switching on the power supply, the initial status of all registers is not determined. It is necessary to enable the generator (bit CH = 0) when setting the initial configurations.

HT4338 operates in the 12-hour or in the 24-hour format. The bit 6 of the watch register determines the operational mode. 12-hour mode corresponds to the high level. In the 12-hour mode the bit 5 is the AM/PM bit. The high level corresponds to PM. In the 24-hour mode, the 5 is the second bit of tens of hours (20 -23 hours).

During application of the signal "START" to the two-wire bus there happen transfer of the real time to the auxiliary set of registers. The time data are read from these auxiliary registers, while the watch proceeds in operation. This eliminates the necessity of repeated reading in case of updating the basic registers in the access process.

Registers RTC HT4338

	BIT7								BIT0
00H	CH	2nd DIGIT of SECONDS			1st DIGIT of SECONDS				00-59
	X	2nd DIGIT of MINUTES			1st DIGIT of MINUTES				00-59
	X	12 / 24	2nd DIGIT of HOURS A/P	2nd DIGIT of HOURS	1st DIGIT of HOURS				01-12 00-23
	X	X	X	X	X	DAY of WEEK			1-7
	X	X	2nd DIGIT of DATE		1st DIGIT of DATE				01-28/29 01-30 01-31
	X	X	X	2nd DIGIT of MONTH	1st DIGIT of MONTH				01-12
		2nd DIGIT of YEARS			1st DIGIT of YEARS				00-99
07H	OUT	X	X	SQWE	X	X	RS1	RS0	

Control Register

Control register is used for control of pin SQW/OUT.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUT	X	X	SQWE	X	X	RS1	RS0

OUT (output control): This bit presets the output logic level of the pin SQW/OUT, when the output of the rectangular signal is locked.

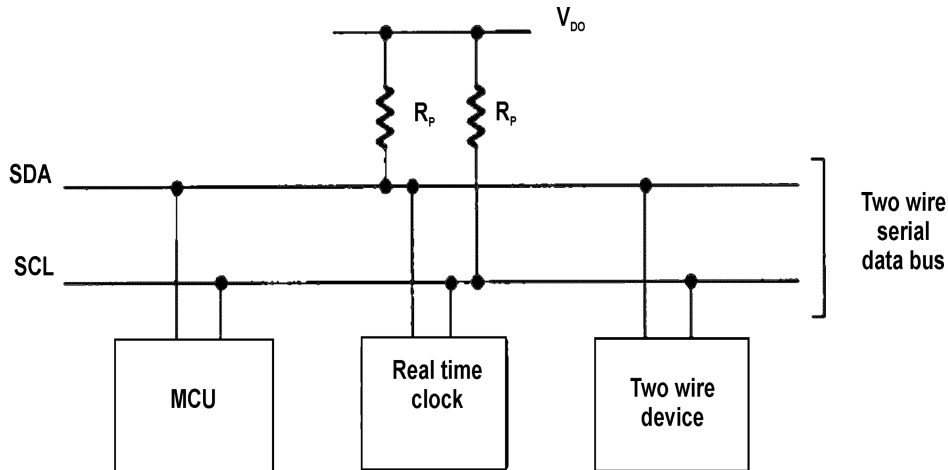
SQWE (rectangular signal enabling): This bit, pre-set to the logic "1", activates the generator output. Frequency of the output rectangular signal is determined by the bits RS0 and RS1.

RS (frequency selection): These bits determine the frequency of the output rectangular signal, when the output of the rectangular signal is activated. The table indicates the frequencies, which can be selected by the bits RS.

RS1	RS0	Frequency SQW/OUT
0	0	1 Hz
0	1	4,096 kHz
1	0	8,192 kHz
1	1	32,768 kHz

Two-wire Serial Data Bus

HT4338 supports the bi-directional two-wire bus and the protocol of the data exchange. The bus can be controlled by the “master” device, which generates the cycle signal (SCL), controls access to the bus, generates the statuses START and STOP. Typical configuration of the bus with the two-wire protocol is indicated in Figure.



Data transfer can be initiated only when the bus is not occupied. In the process of the data transfer the data line should remain stable, while the line of the cycle signal is in the high status. Status alterations of the data line at that moment, when the cycle line is in the high status, will be regarded as the control signals.

In compliance with this the following conditions are determined:

Bus not occupied: both the data line and the cycle signal are in the HIGH status.

Data transfer start: Status alteration of the data line during transition from HIGH to LOW, while the cycle line is in the HIGH status, is determined as the status START.

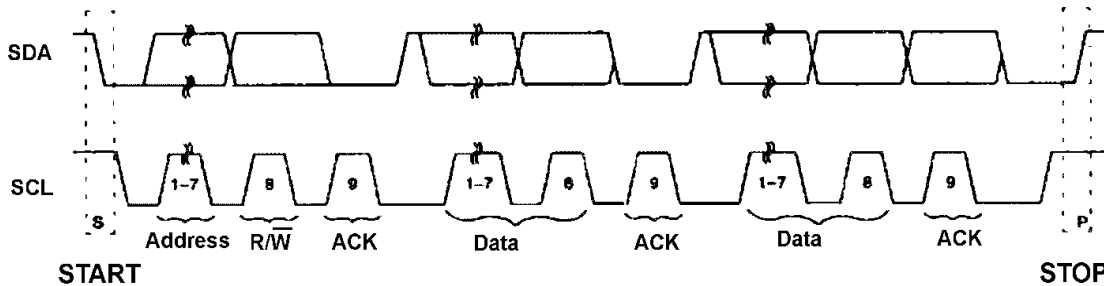
Data transfer stop: Status alteration of the data line during transition from LOW to HIGH, while the cycle line is in the HIGH status, is determined as the status STOP.

Valid data: Data line status complies with the valid data, when after the status START the data line is stable during the HIGH status of the cycle signal. Data on the line should be altered at the time of the LOW status of the cycle signal. One cycle pulse per one data bit.

Each data transfer starts at the beginning of the status START and ceases at the beginning of the status STOP. Number of the data bytes, transferred between the statuses START and STOP is not limited and is determined by the «master» device. Information is transferred byte by byte, and each receipt is confirmed by the ninth byte. HT4338 operates in the normal mode only (100 kHz).

Confirmation of receipt: Each receiving device, when it being addressed, has to generate the receipt confirmation after receiving each byte. «Master» device should generate the cycle pulses, which are allocated in compliance with the confirmation bits.

If the receipt confirmation signal is in the high status, then on arrival of the confirmation cycle pulse, the device, confirming the receipt, should switch over the SDA line to the low status. Of course, there should be considered the pre-set time and the hold time. The «master» device should signalize on completion of the data transfer to the “slave” device, ceasing generation of the confirmation bit on receiving the receipt confirmation from the “slave” cycle pulse. In this case, the «slave one should switch over the data line to the low status, in order to enable the «master» one generate the condition of STOP.



Depending on the status of bit R/\overline{W} , there are possible two types of transfer:

1. **Data are transferred from the «master» transmitter to the «slave» receiver.** The first byte, transmitted by the «master» one, is the address for the «slave» one. Then follows a sequence of the data bytes. The «slave» one returns the receipt confirmation bytes after each received byte. Order of the data transfer: the first is the most senior digit (MSB).

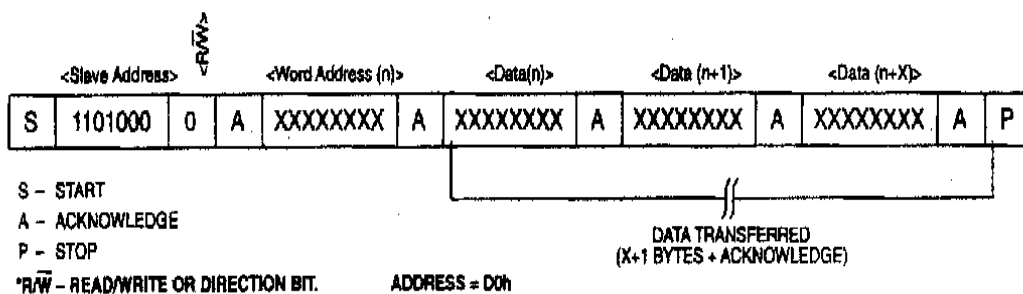
2. **The data are transferred from the «slave» transmitter to the «master» receiver.** The first byte (address of «slave») is applied to the «master». Then the «master» returns the confirmation bit. This follows after the transfer by the «slave» of the data sequence. The «master» returns the receipt confirmation bit after each received byte, with the exception of the last byte. After receipt of the last byte the receipt confirmation bit is not returned.

The «master» device generates all cycle pulses and the statuses START and STOP. Transfer is completed at emergence of the status STOP or the repeated emergence of the status START. As the repeated status START is the beginning of the next serial transfer, the bus is not vacated. The data transfer order: the first is the most senior digit (MSB).

HT4338 can operate in the two following modes:

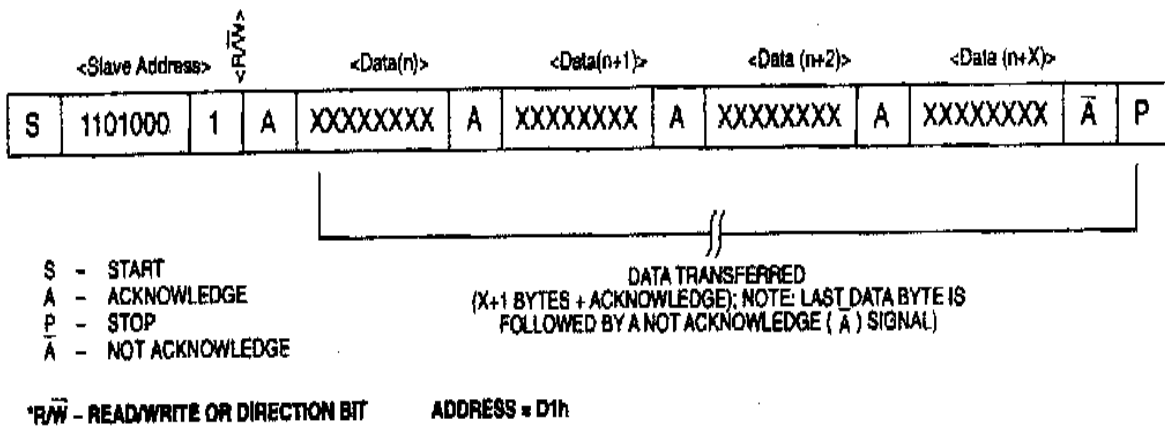
1. **Mode of «slave» receiver (write mode of HT4338):** Serial data and cycles are received via SDA and SCL appropriately. After transfer of each byte the confirmation bit is sent. The statuses START and STOP are recognized as the beginning and the end of the serial transfer. The address recognition is performed by means of the hardware after receipt of the «slave» address and the direction bit. The address byte is the first byte, received after occurrence of the START status, generated by the «master». The address byte contains the seven address bits of HT4338, equal to 1101000, accompanied by the direction bit (R/\overline{W}), which for write is equal to 0. After receipt and decoding of the address byte, HT4338 applies confirmation to the line SDA. After confirmation by HT4338 of the «slave» address and the write bit, the «master» sends the register address of HT4338. Thus the register indicator will be preset in HT4338. Then the «smart» shall start to send each data byte with the subsequent receipt confirmation of each byte. Upon completion of writing the «master» shall formulate the status STOP for termination of the data transfer.

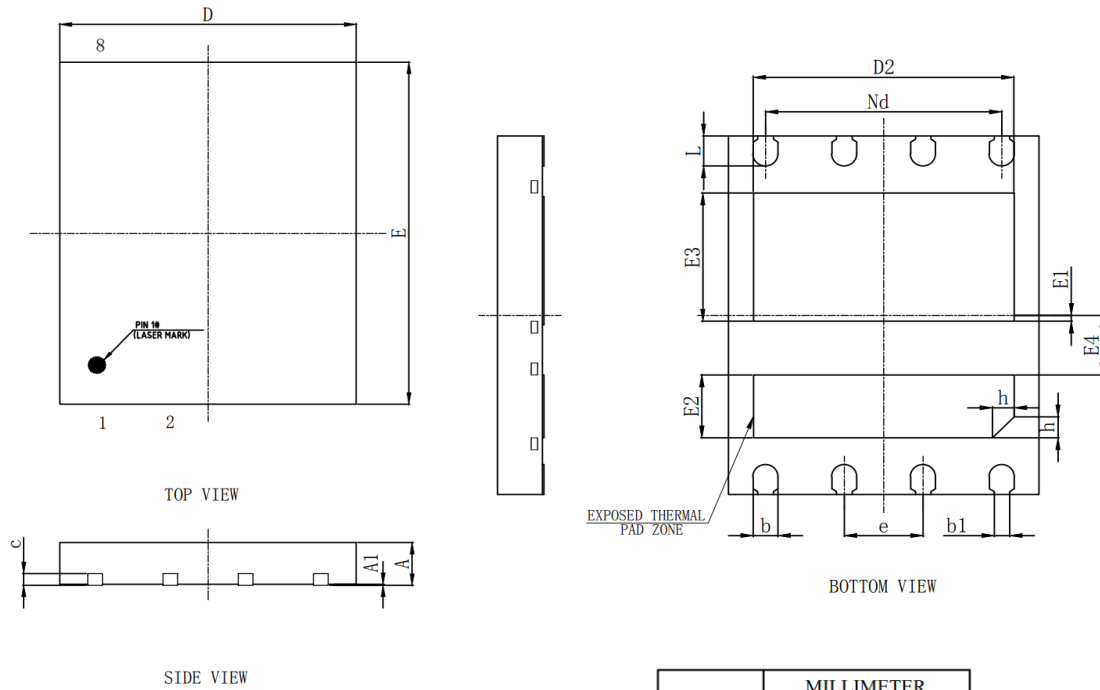
Data writing – mode of «slave» receiver



2. **Mode of «slave» receiver (write mode from HT4338):** The first byte is received and processed as in the mode of the «slave» receiver. However, in this mode the direction bit will signify, that the transmission direction is changed. HT4338 sends the serial data by SDA, the cycle pulses - by SCL. statuses START and STOP are understood as the beginning and end of the consecutive transmission. The address byte is the first byte, received after occurrence of the status START, generated by the «master». The address byte contains the seven bits of the address HT4338, equal to 1101000, accompanied by the direction bit ($\overline{R/W}$), which is equal to 1 for reading. After receipt and decoding of the address byte HT4338 receives confirmation from the line SDA. Then HT4338 starts to send the data from the address, which is indicated by the register indicator. If the register indicator is not written prior to initialization of the read mode, then the first read address is the last address, retained in the register indicator. HT4338 should send the bit of «non-confirmation», in order to complete the reading.

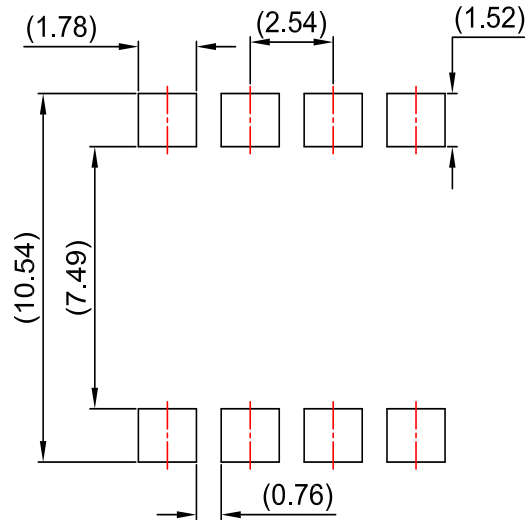
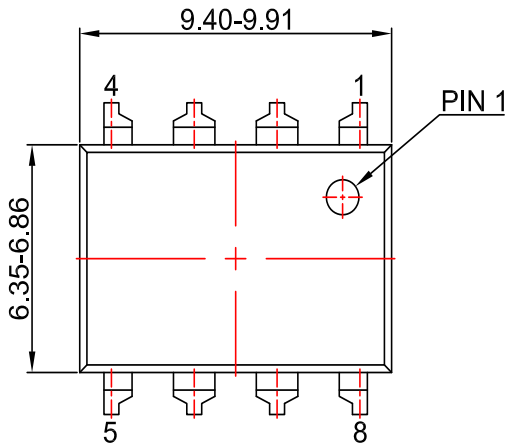
Data reading – mode of «slave» transmitter



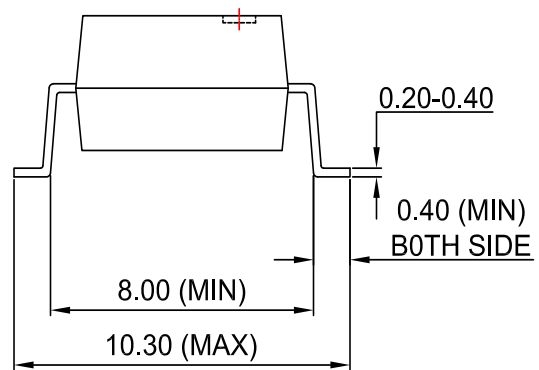
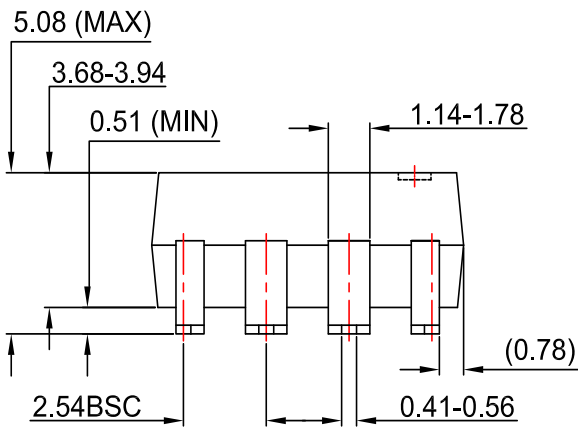
DFN8(5*6) package information


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.35	0.40	0.45
b1	0.25REF		
c	0.15	0.20	0.25
D	4.90	5.00	5.10
Nd	3.81 BSC		
e	1.27 BSC		
E	5.90	6.00	6.10
D2	4.10	4.20	4.30
E1	0.05	0.10	0.15
E2	0.95	1.05	1.15
E3	2.10	2.15	2.20
E4	0.95	1.00	1.05
L	0.45	0.50	0.55
h	0.30	0.35	0.40
L/F载体尺寸	4.60x2.55/4.60x1.45		

DUB8 (7.5*6.5) package information



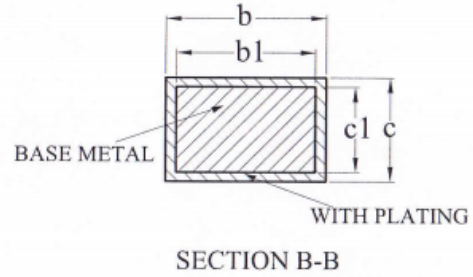
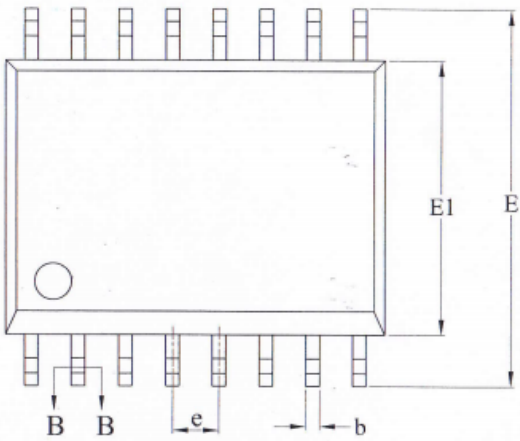
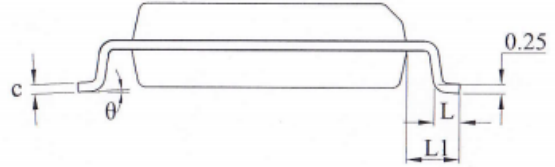
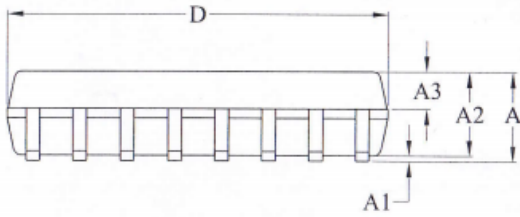
LAND PATTERN RECOMMENDATION



NOTES:

- A) NO STANDARD APPLIES TO THIS PACKAGE
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION
- D) DRAWING FILENAME AND REVISION: MKT-N08Hrev7.

WSOP16: plastic small outline package; 16 leads; body width 7.5 mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	—	0.43
b1	0.34	0.37	0.40
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.55	—	0.85
L1	1.40REF		
θ	0	—	8°

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