1uA, Rail-to-Rail Input/Output Op Amps

Features

- Low Quiescent Current: 1uA/amplifier (typical)
- Rail-to-Rail Input/Output
- Gain Bandwidth Product: 14 kHz (typical)
- Wide Supply Voltage Range: 1.4V to 6.0V
- Unity Gain Stable
- Available in Single, Dual, and Quad
- Chip Select ($\overline{CS}$) with HT6043
- Available in 5-lead and 6-lead SOT-23 Packages
- Temperature Ranges:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

Applications

- Toll Booth Tags
- Wearable Products
- Temperature Measurement
- Battery Powered

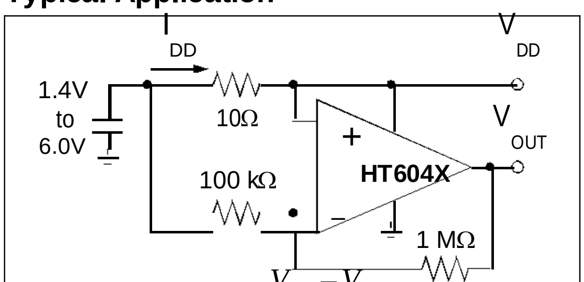
Design Aids

- SPICE Macro Models
- FilterLab® Software
- Analog Demonstration and Evaluation Boards
- Application Notes

Related Devices

- HT6141/2/3/4: G = +10 Stable Op Amps

Typical Application



$$I_{DD} = \frac{V_{DD} - V_{OUT}}{(10\ V/V) \cdot (10\ \Omega)}$$

High Side Battery Current Sensor

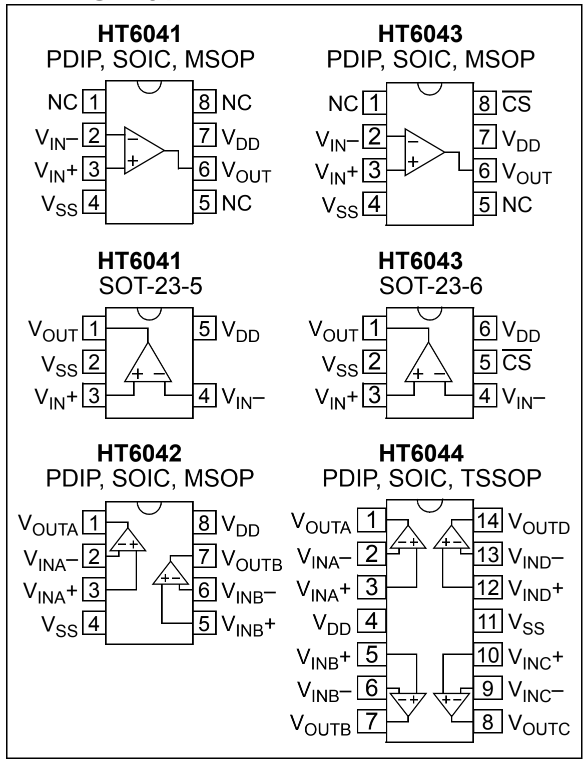
Description

The HT6041/2/3/4 family of operational amplifiers (op amps) from HTCSEMI Technology Inc. operate with a single supply voltage as low as 1.4V, while drawing less than 1 µA (maximum) of quiescent current per amplifier. These devices are also designed to support rail-to-rail input and output operation. This combination of features supports battery-powered and portable applications.

The HT6041/2/3/4 amplifiers have a gain-bandwidth product of 14 kHz (typical) and are unity gain stable. These specifications make these op amps appropriate for low frequency applications, such as battery current monitoring and sensor conditioning.

The HT6041/2/3/4 family operational amplifiers are offered in single (HT6041), single with Chip Select ($\overline{CS}$) (HT6043), dual (HT6042), and quad (HT6044) configurations. The HT6041 device is available in the 5-lead SOT-23 package, and the HT6043 device is available in the 6-lead SOT-23 package.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
Current at Input Pins .... ±2 mA
Analog Inputs ($V_{IN}+$, $V_{IN}-$) .... V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs.......... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input voltage .... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .... continuous
Current at Output and Supply Pins ....±30 mA
Storage Temperature.......... –65°C to +150°C
Junction Temperature.......... +150°C
ESD protection on all pins (HBM; MM) .... ≥ 4 kV; 200V

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
†† See **Section 4.1 "Rail-to-Rail Input"**

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, and R_L = 1 MΩ to V_L (refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-3	—	+3	mV	$V_{CM} = V_{SS}$
Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±2	—	µV/°C	$V_{CM} = V_{SS}$, T_A= -40°C to +85°C
	$\Delta V_{OS}/\Delta T_A$	—	±15	—	µV/°C	$V_{CM} = V_{SS}$, T_A= +85°C to +125°C
Power Supply Rejection	PSRR	70	85	—	dB	$V_{CM} = V_{SS}$
Input Bias Current and Impedance						
Input Bias Current	I_B	—	1	—	pA	
Industrial Temperature	I_B	—	20	100	pA	T_A = +85°
Extended Temperature	I_B	—	1200	5000	pA	T_A = +125°
Input Offset Current	I_{OS}	—	1	—	pA	
Common-mode Input Impedance	Z_{CM}	—	10^{13}‖6	—	Ω‖pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}‖6	—	Ω‖pF	
Common-mode						
Common-mode Input Range	V_{CMR}	V_{SS}–0.3	—	V_{DD}+0.3	V	
Common-mode Rejection Ratio	CMRR	62	80	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 5.3V
	CMRR	60	75	—	dB	V_{DD} = 5V, V_{CM} = 2.5V to 5.3V
	CMRR	60	80	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 2.5V
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	95	115	—	dB	R_L = 50 kΩ to V_L, V_{OUT} = 0.1V to V_{DD}–0.1V
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 10	—	V_{DD} – 10	mV	R_L = 50 kΩ to V_L, 0.5V input overdrive
Linear Region Output Voltage Swing	V_{OVR}	V_{SS} + 100	—	V_{DD} – 100	mV	R_L = 50 kΩ to V_L, A_{OL} ≥ 95 dB
Output Short Circuit Current	I_{SC}	—	2	—	mA	V_{DD} = 1.4V
	I_{SC}	—	20	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.4	—	6.0	V	(**Note 1**)
Quiescent Current per Amplifier	I_Q	0.3	0.6	1.0	µA	I_O = 0

Note 1: All parts with date codes November 2007 and later have been screened to ensure operation at V_{DD} = 6.0V. However, the other minimum and maximum specifications are measured at 1.4V and/or 5.5V.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 MΩ to V_L, and C_L = 60 pF (refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	14	—	kHz	
Slew Rate	SR	—	3.0	—	V/ms	
Phase Margin	PM	—	65	—	°	G = +1 V/V
Noise						
Input Voltage Noise	E_{ni}	—	5.0	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Voltage Noise Density	e_{ni}	—	170	—	nV/√Hz	f = 1 kHz
Input Current Noise Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

HT6043 CHIP SELECT ($\overline{CS}$) ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 MΩ to V_L, and C_L = 60 pF (refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	V_{SS}+0.3	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	5	—	pA	$\overline{CS} = V_{SS}$
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	V_{DD}–0.3	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	5	—	pA	$\overline{CS} = V_{DD}$
$\overline{CS}$ Input High, GND Current	I_{SS}	—	-20	—	pA	$\overline{CS} = V_{DD}$
Amplifier Output Leakage, $\overline{CS}$ High	I_{OLEAK}	—	20	—	pA	$\overline{CS} = V_{DD}$
Dynamic Specifications						
$\overline{CS}$ Low to Amplifier Output Turn-on Time	t_{ON}	—	2	50	ms	G = +1V/V, $\overline{CS}$ = 0.3V to $V_{OUT} = 0.9V_{DD}/2$
$\overline{CS}$ High to Amplifier Output High-Z	t_{OFF}	—	10	—	µs	G = +1V/V, $\overline{CS} = V_{DD}$–0.3V to $V_{OUT} = 0.1V_{DD}/2$
Hysteresis	V_{HYST}	—	0.6	—	V	V_{DD} = 5.0V

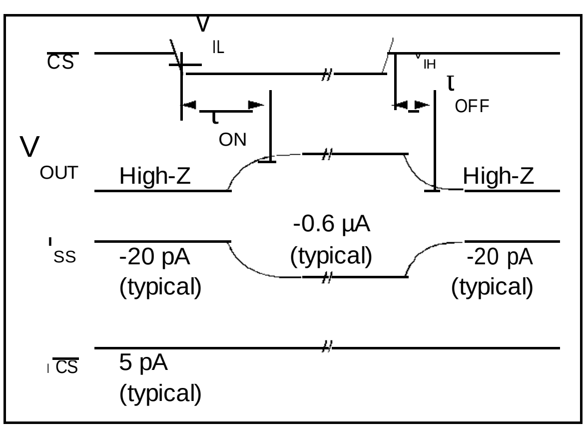


FIGURE 1-1: *Chip Select ($\overline{CS}$) Timing Diagram (HT6043 only).*

TEMPERATURE CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.4V to +5.5V, V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	Industrial Temperature parts
	T_A	-40	—	+125	°C	Extended Temperature parts
Operating Temperature Range	T_A	-40	—	+125	°C	(**Note 1**)
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	230	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note **1:** The HT6041/2/3/4 family of Industrial Temperature op amps operates over this extended range, but with reduced performance. In any case, the internal Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in Figure 1-2 and Figure 1-3. The bypass capacitors are laid out according to the rules discussed in **Section 4.6 "Supply Bypass"**.

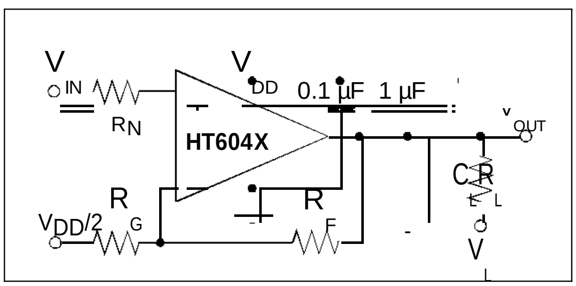


FIGURE 1-2: *AC and DC Test Circuit for Most Non-Inverting Gain Conditions.*

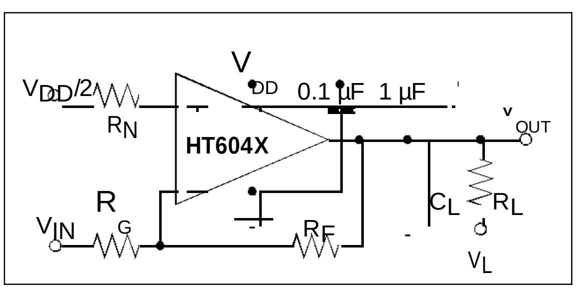


FIGURE 1-3: *AC and DC Test Circuit for Most Inverting Gain Conditions.*

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, and C_L = 60 pF.

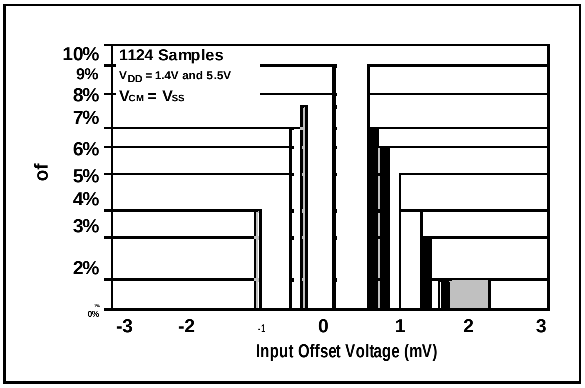


FIGURE 2-1: *Input Offset Voltage.*

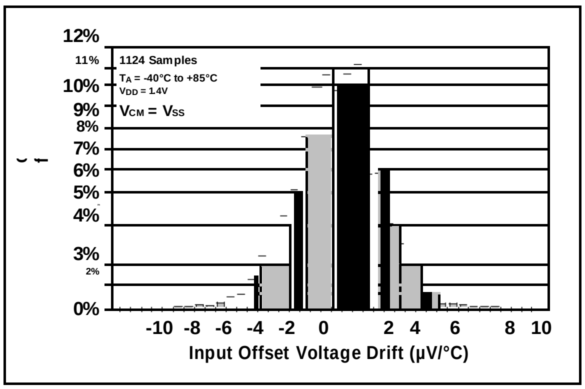


FIGURE 2-2: *Input Offset Voltage Drift with T_A = -40°C to +85°C.*

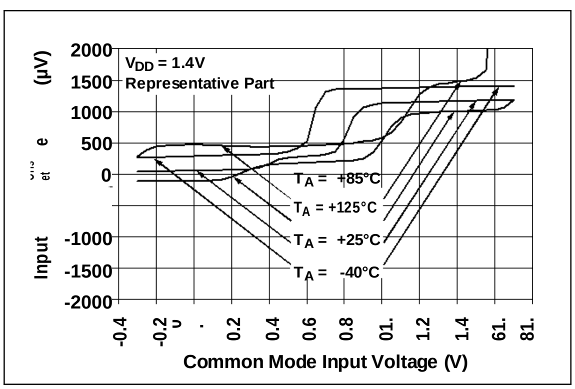


FIGURE 2-3: *Input Offset Voltage vs. Common-mode Input Voltage with V_{DD} = 1.4V.*

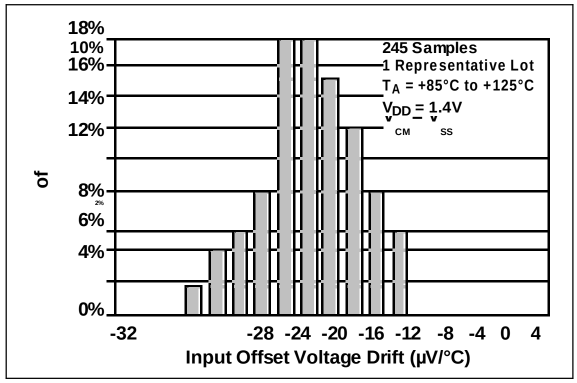


FIGURE 2-4: *Input Offset Voltage Drift with T_A = +85°C to +125°C and V_{DD} = 1.4V.*

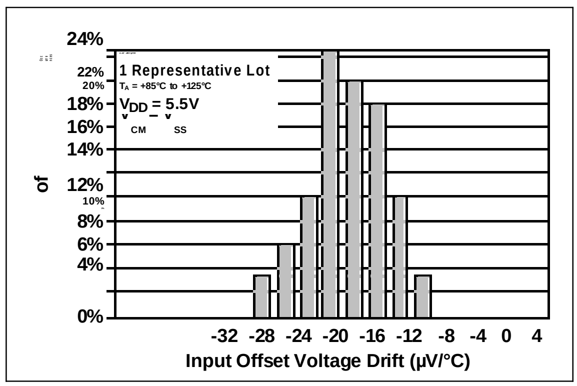


FIGURE 2-5: *Input Offset Voltage Drift with T_A = +25°C to +125°C and V_{DD} = 5.5V.*

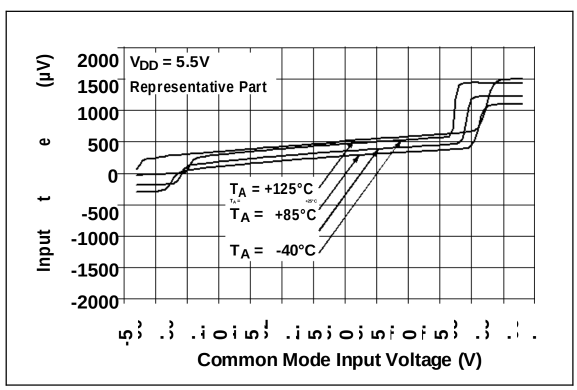


FIGURE 2-6: *Input Offset Voltage vs. Common -mode Input Voltage with V_{DD} = 5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, and C_L = 60 pF.

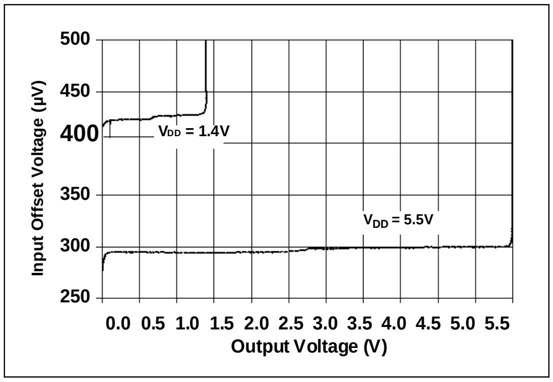


FIGURE 2-7: *Input Offset Voltage vs. Output Voltage.*

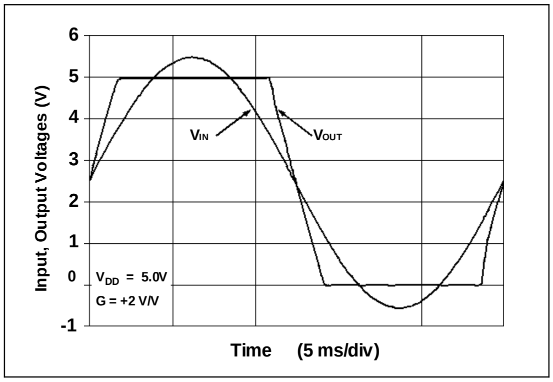


FIGURE 2-10: *The HT6041/2/3/4 family shows no phase reversal.*

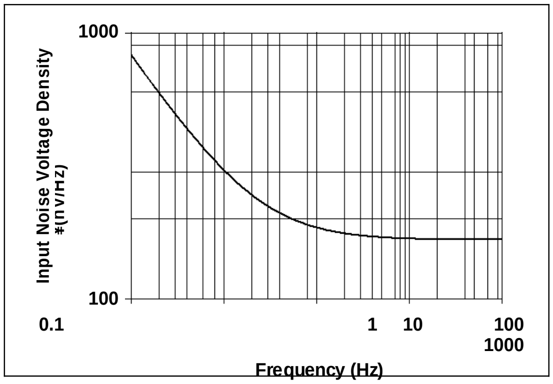


FIGURE 2-8: *Input Noise Voltage Density vs. Frequency.*

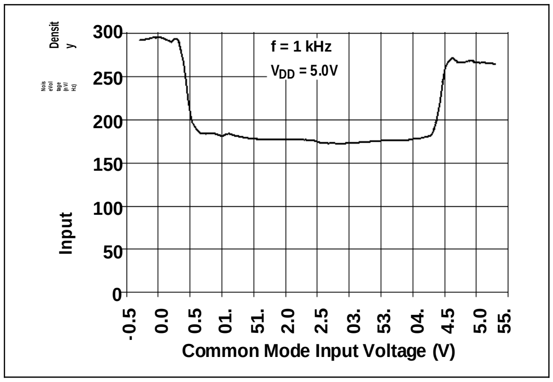


FIGURE 2-11: *Input Noise Voltage Density vs. Common-mode Input Voltage.*

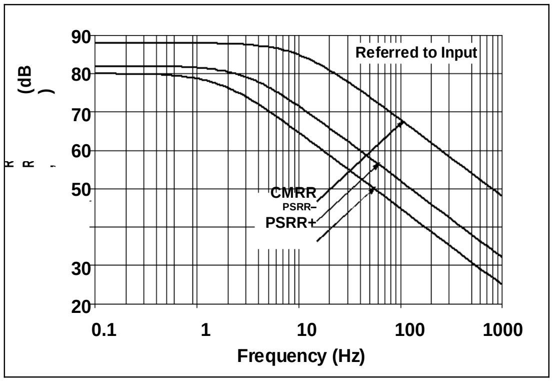


FIGURE 2-9: *CMRR, PSRR vs. Frequency.*

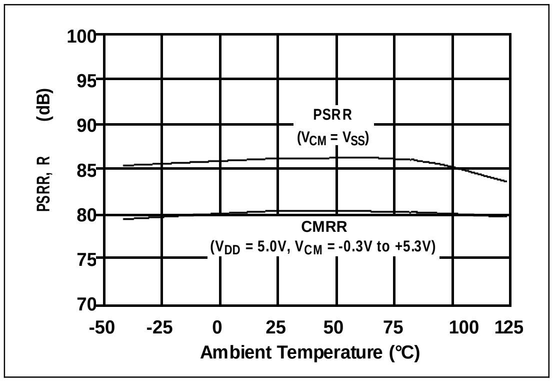


FIGURE 2-12: *CMRR, PSRR vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +6.0V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 1 MΩ to V_L, and C_L = 60 pF.

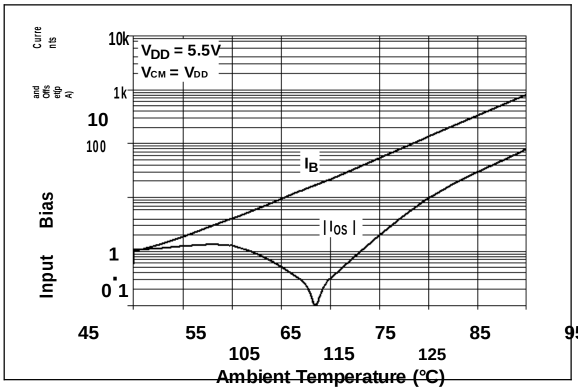


FIGURE 2-13: *Input Bias, Offset Currents vs. Ambient Temperature.*

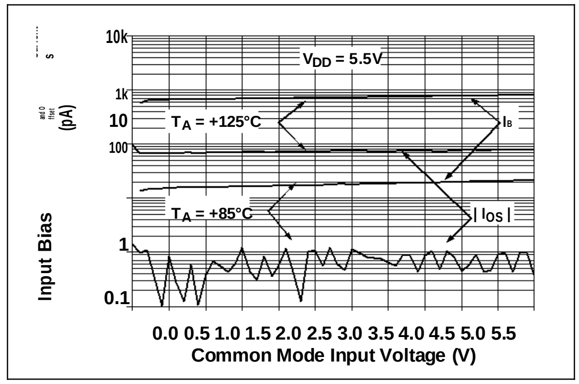


FIGURE 2-16: *Input Bias, Offset Currents vs. Common-mode Input Voltage.*

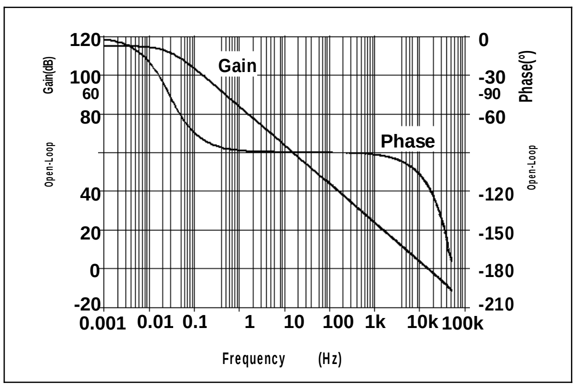


FIGURE 2-14: *Open-Loop Gain, Phase vs. Frequency.*

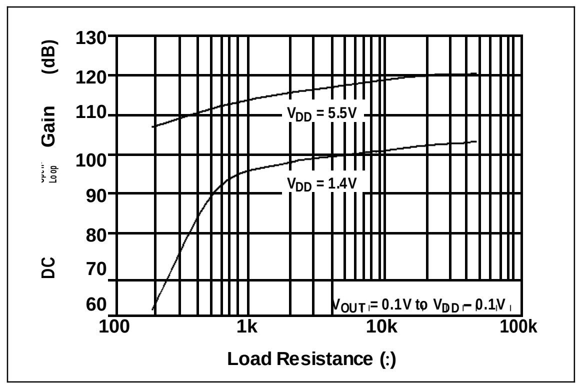


FIGURE 2-17: *DC Open-Loop Gain vs. Load Resistance.*

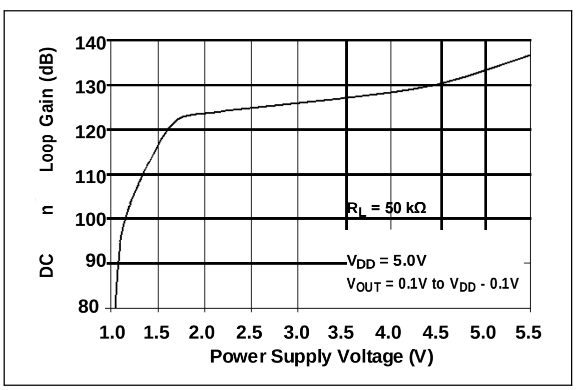


FIGURE 2-15: *DC Open-Loop Gain vs. Power Supply Voltage.*

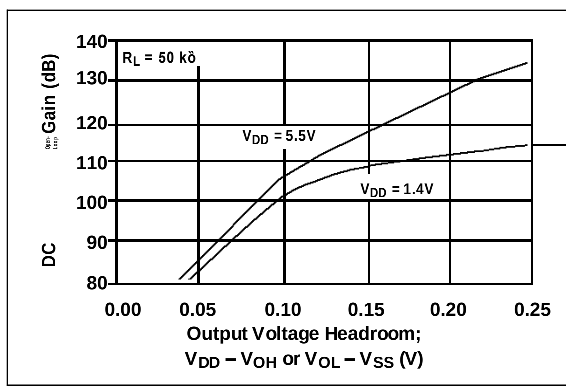


FIGURE 2-18: *DC Open-Loop Gain vs. Output Voltage Headroom.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, and C_L = 60 pF.

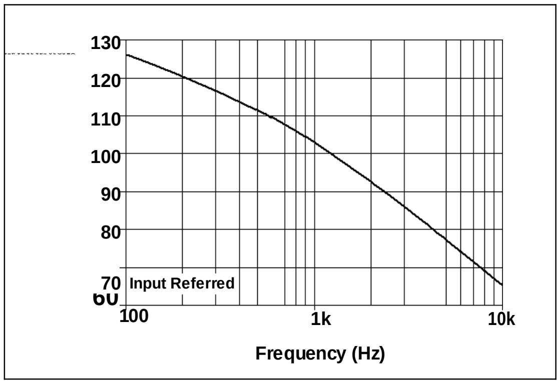


FIGURE 2-19: *Channel-to-Channel Separation vs. Frequency (HT6042 and HT6044 only).*

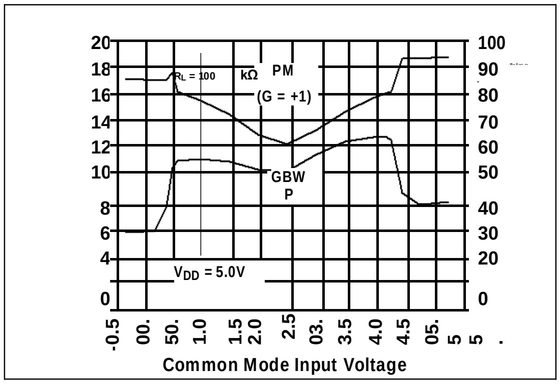


FIGURE 2-22: *Gain Bandwidth Product, Phase Margin vs. Common-mode Input Voltage.*

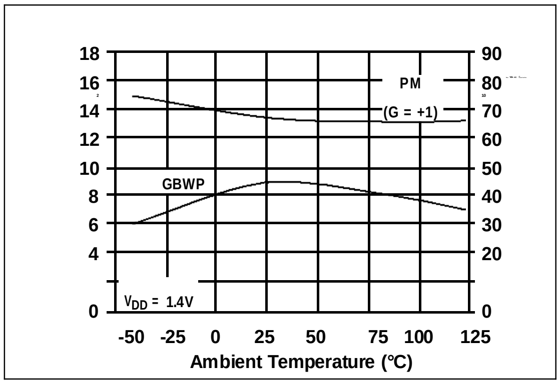


FIGURE 2-20: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature with V_{DD} = 1.4V.*

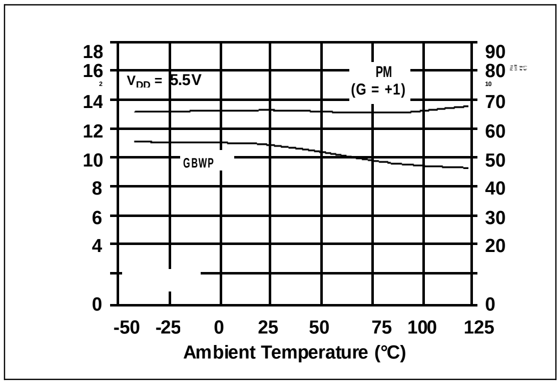


FIGURE 2-23: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature with V_{DD} = 5.5V.*

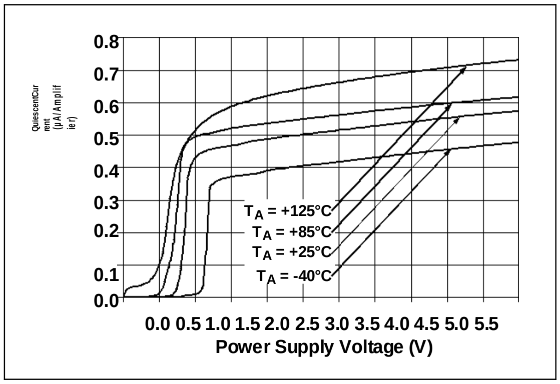


FIGURE 2-21: *Quiescent Current vs. Power Supply Voltage.*

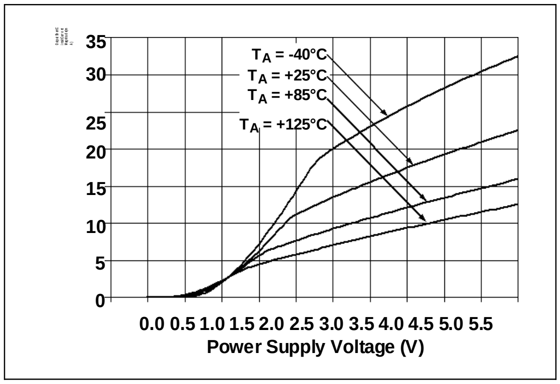


FIGURE 2-24: *Output Short Circuit Current vs. Power Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, and C_L = 60 pF.

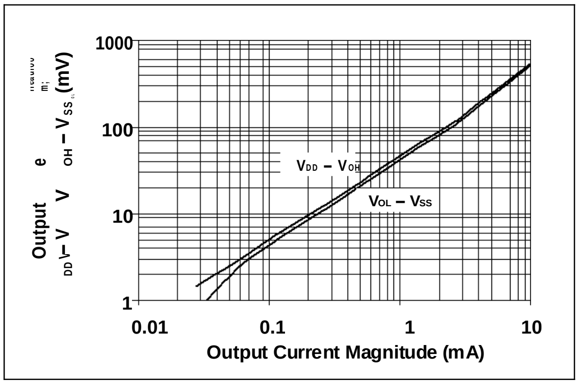


FIGURE 2 -25: *Output Voltage Headroom vs. Output Current Magnitude.*

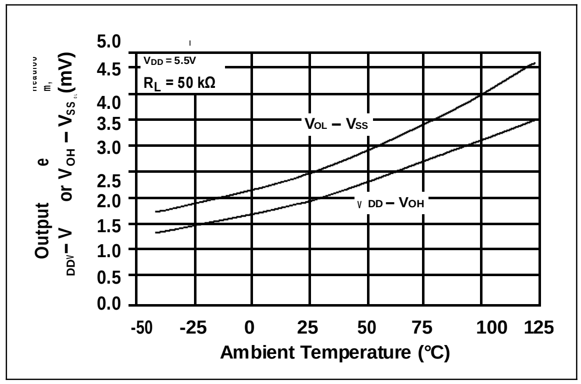


FIGURE 2-28: *Output Voltage Headroom vs. Ambient Temperature.*

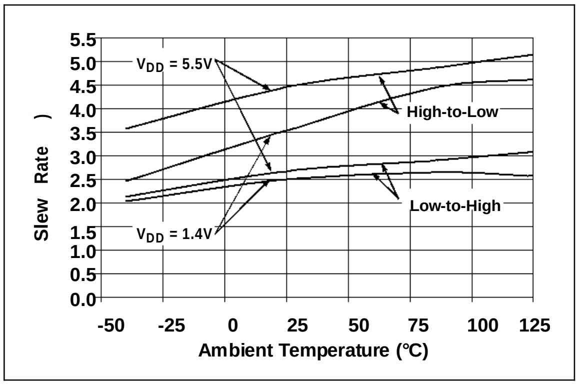


FIGURE 2-26: *Slew Rate vs. Ambient Temperature.*

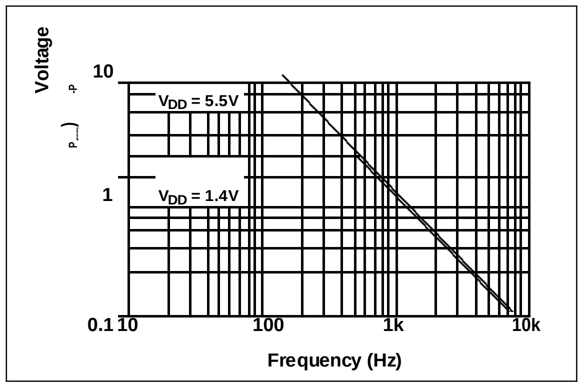


FIGURE 2-29: *Maximum Output Voltage Swing vs. Frequency.*

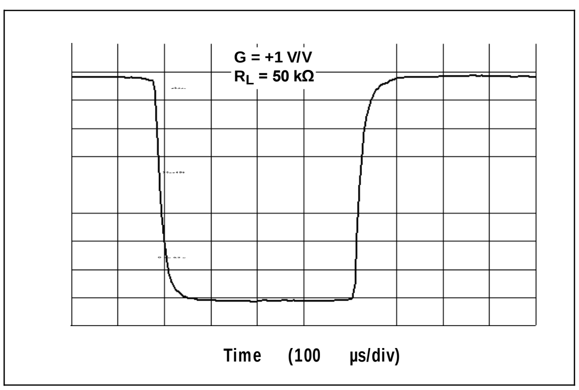


FIGURE 2-27: *Small Signal Non-inverting Pulse Response.*

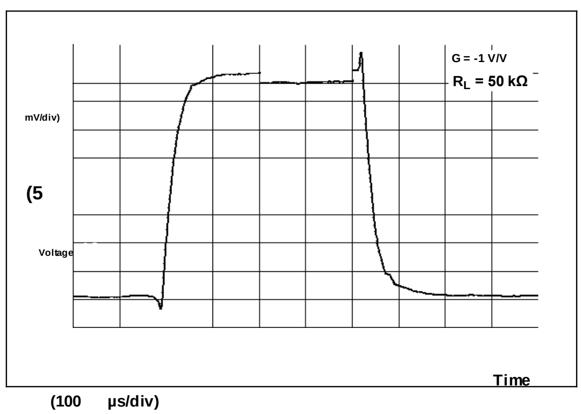


FIGURE 2-30: *Small Signal Inverting Pulse Response.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, and C_L = 60 pF.

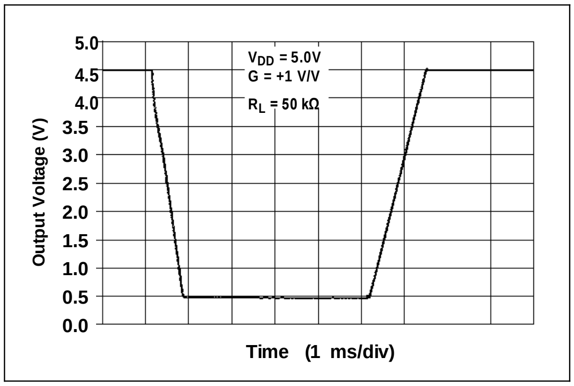


FIGURE 2-31: *Large Signal Non-inverting Pulse Response.*

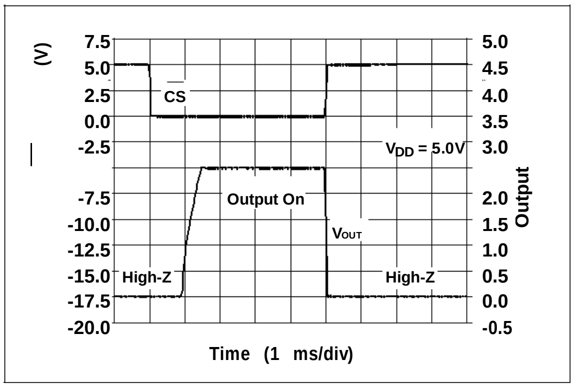


FIGURE 2-32: *Chip Select ($\overline{CS}$) to Amplifier Output Response Time (HT6043 only).*

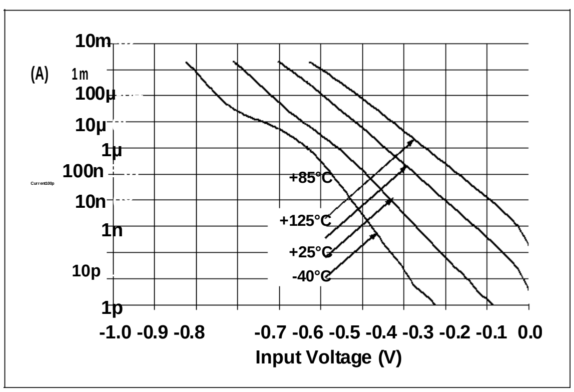


FIGURE 2-33: *Input Current vs. Input Voltage (below V_{SS}).*

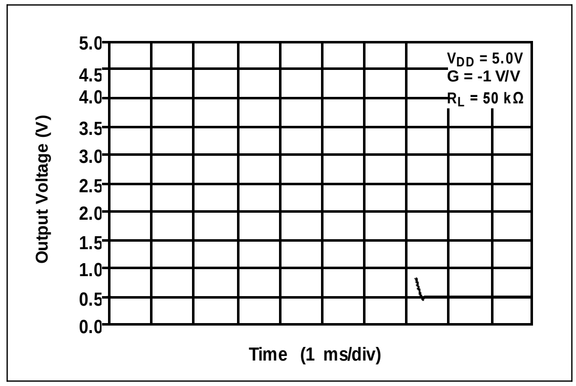


FIGURE 2-34: *Large Signal Inverting Pulse Response.*

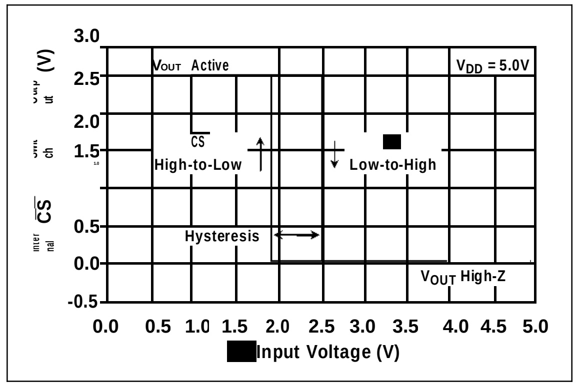


FIGURE 2- 35: *Chip Select (CS) $\overline{\text{Hysteresis}}$ (HT6043 only).*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

HT6041		HT6042	HT6043		HT6044	Symbol	Description
PDIP, SOIC, MSOP	SOT-23-5	PDIP, SOIC, MSOP	PDIP, SOIC, MSOP	SOT-23-6	PDIP, SOIC, TSSOP		
6	1	1	6	1	1	V_{OUT}, V_{OUTA}	Analog Output (op amp A)
2	4	2	2	4	2	$V_{IN}-$, $V_{INA}-$	Inverting Input (op amp A)
3	3	3	3	3	3	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (op amp A)
7	5	8	7	6	4	V_{DD}	Positive Power Supply
—	—	5	—	—	5	$V_{INB}+$	Non-inverting Input (op amp B)
—	—	6	—	—	6	$V_{INB}-$	Inverting Input (op amp B)
—	—	7	—	—	7	V_{OUTB}	Analog Output (op amp B)
—	—	—	—	—	8	V_{OUTC}	Analog Output (op amp C)
—	—	—	—	—	9	$V_{INC}-$	Inverting Input (op amp C)
—	—	—	—	—	10	$V_{INC}+$	Non-inverting Input (op amp C)
4	2	4	4	2	11	V_{SS}	Negative Power Supply
—	—	—	—	—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	—	—	—	—	13	$V_{IND}-$	Inverting Input (op amp D)
—	—	—	—	—	14	V_{OUTD}	Analog Output (op amp D)
—	—	—	8	5	—	$\overline{CS}$	Chip Select
1, 5, 8	—	—	1, 5	—	—	NC	No Internal Connection

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-imped-ance CMOS inputs with low bias currents.

3.3 Chip Select Digital Input

This is a CMOS, Schmitt-triggered input that places the part into a low power mode of operation.

3.4 Power Supply Pins

The positive power supply pin (V_{DD}) is 1.4V to 6.0V higher than the negative power supply pin (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

4.0 APPLICATIONS INFORMATION

The HT6041/2/3/4 family of op amps is manufactured using Htcsemi's state of the art CMOS process. These op amps are unity gain stable and suitable for a wide range of general purpose, low-power applications.

See Htcsemi's related HT6141/2/3/4 family of op amps for applications, at a gain of 10 V/V or higher, needing greater bandwidth.

4.1 Rail-to-Rail Input

4.1.1 PHASE REVERSAL

The HT6041/2/3/4 op amps are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-10 shows an input voltage exceeding both supplies with no phase inversion.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

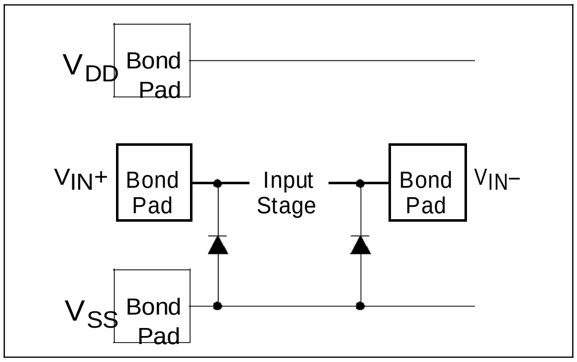
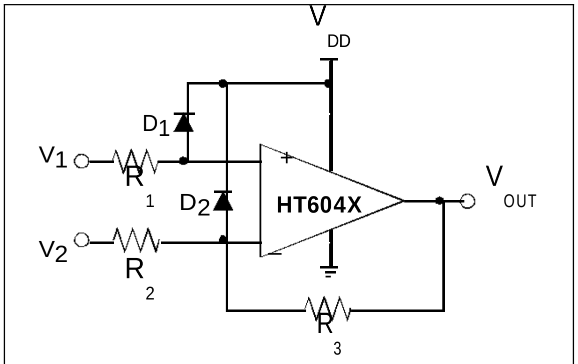


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents (and voltages) at the input pins (see **Absolute Maxi-mum Ratings †** at the beginning of **Section 1.0 "Elec-trical Characteristics"**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins ($V_{IN}+$ and $V_{IN}-$) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins ($V_{IN}+$ and $V_{IN}-$) from going too far above V_{DD}, and dump any currents onto V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.



$$R_1 > \frac{V_{SS} - (\text{minimum expected } V_1)}{2\ mA}$$

$$R_2 > \frac{V_{SS} - (\text{minimum expected } V_2)}{2\ mA}$$

FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of the resistor R_1 and R_2. In this case, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins ($V_{IN}+$ and $V_{IN}-$) should be very small.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the Common-mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-33. Applications that are high impedance may need to limit the useable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the HT6041/2/3/4 op amps uses two differential input stages in parallel. One operates at a low Common-mode input voltage (V_{CM}), while the other operates at a high V_{CM}. With this topology, the device operates with a V_{CM} up to 300 mV above V_{DD} and 300 mV below V_{SS}. The input offset voltage is measured at $V_{CM} = V_{SS} - 0.3V$ and $V_{DD} + 0.3V$ to ensure proper operation.

There are two transitions in input behavior as V_{CM} is changed. The first occurs, when V_{CM} is near V_{SS} + 0.4V, and the second occurs when V_{CM} is near V_{DD} – 0.5V (see Figure 2-3 and Figure 2-6). For the best distortion performance with non-inverting gains, avoid these regions of operation.

4.2 Rail-to-Rail Output

There are two specifications that describe the output swing capability of the HT6041/2/3/4 family of op amps. The first specification (Maximum Output Voltage Swing) defines the absolute maximum swing that can be achieved under the specified load condition. Thus, the output voltage swings to within 10 mV of either sup-ply rail with a 50 kΩ load to $V_{DD}/2$. Figure 2-10 shows how the output voltage is limited when the input goes beyond the linear region of operation.

The second specification that describes the output swing capability of these amplifiers is the Linear Output Voltage Range. This specification defines the maxi-mum output swing that can be achieved while the amplifier still operates in its linear region. To verify linear operation in this range, the large signal DC Open-Loop Gain (A_{OL}) is measured at points inside the supply rails. The measurement must meet the specified A_{OL} condition in the specification table.

4.3 Output Loads and Battery Life

The HT6041/2/3/4 op amp family has outstanding quiescent current, which supports battery-powered applications. There is minimal quiescent current glitching when Chip Select (CS) is raised or lowered. This prevents excessive current draw, and reduced battery life, when the part is turned off or on.

Heavy resistive loads at the output can cause excessive battery drain. Driving a DC voltage of 2.5V across a 100 kΩ load resistor will cause the supply cur-rent to increase by 25 µA, depleting the battery 43 times as fast as I_Q (0.6 µA, typical) alone.

High frequency signals (fast edge rate) across capacitive loads will also significantly increase supply current. For instance, a 0.1 µF capacitor at the output presents an AC impedance of 15.9 kΩ (1/2πfC) to a 100 Hz sinewave. It can be shown that the average power drawn from the battery by a 5.0 V_{p-p} sinewave (1.77 V_{rms}), under these conditions, is

EQUATION 4-1:

$$P_{Supply} = (V_{DD} - V_{SS})(I_Q + V_{L(p-p)} f C_L)$$

$$= (5V)(0.6\ \mu A + 5.0V_{p-p} \cdot 100Hz \cdot 0.1\ \mu F)$$

$$= 3.0\ \mu W + 50\ \mu W$$

This will drain the battery 18 times as fast as I_Q alone.

4.4 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity gain buffer (G = +1) is the most sensitive to capacitive loads, although all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 60 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

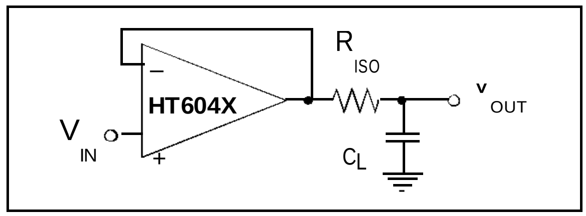


FIGURE 4-3: *Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.*

Figure 4-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

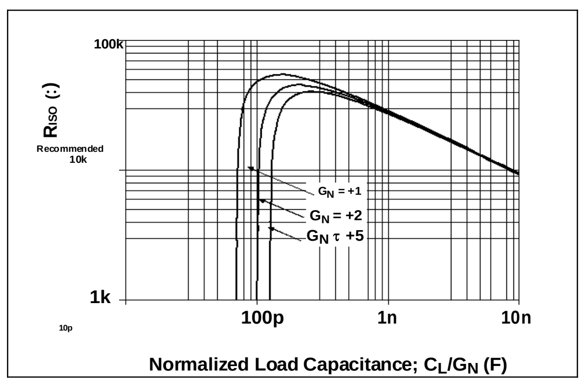


FIGURE 4-4: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the HT6041/2/3/4 SPICE macro model are helpful.

4.5 HT6043 Chip Select

The HT6043 is a single op amp with Chip Select (CS). When CS is pulled high, the supply current drops to 50 nA (typical) and flows through the CS pin to V_{SS}. When this happens, the amplifier output is put into a high impedance state. By pulling CS low, the amplifier is enabled. If the CS pin is left floating, the amplifier may not operate properly. Figure 1-1 shows the output voltage and supply current response to a CS pulse.

4.6 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor is not required for most applications and can be shared with nearby analog parts.

4.7 Unused Op Amps

An unused op amp in a quad package (HT6044) should be configured as shown in Figure 4-5. These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

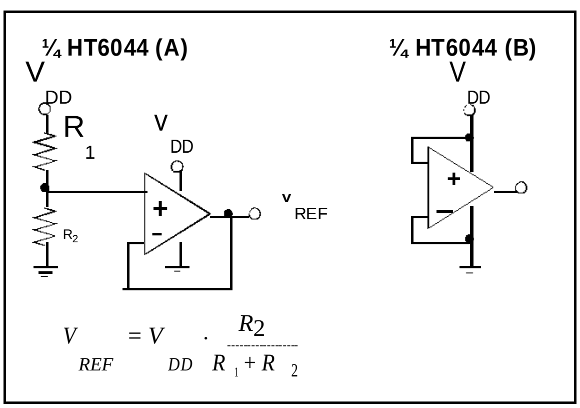


FIGURE 4-5: *Unused Op Amps.*

4.8 PCB Surface Leakage

In applications where low input bias current is critical, printed circuit board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the HT6041/2/3/4 family's bias current at +25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. Figure 4-6 shows an example of this type of layout.

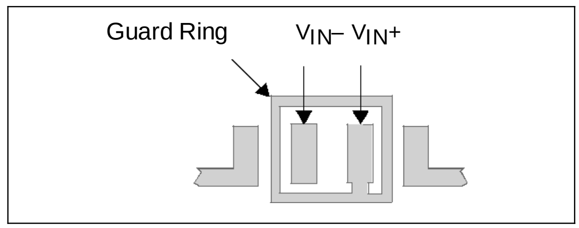


FIGURE 4-6: *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity Gain Buffer:
   a) Connect the non-inverting pin ($V_{IN}+$) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin ($V_{IN}-$). This biases the guard ring to the Common-mode input voltage.
2. Inverting Gain and Transimpedance Gain (convert current to voltage, such as photo detectors) amplifiers:
   a) Connect the guard ring to the non-inverting input pin ($V_{IN}+$). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b) Connect the inverting pin ($V_{IN}-$) to the input with a wire that does not touch the PCB surface.

4.9 Application Circuits

4.9.1 BATTERY CURRENT SENSING

The HT6041/2/3/4 op amps' Common-mode Input Range, which goes 0.3V beyond both supply rails, supports their use in high-side and low-side battery current sensing applications. The very low quiescent current (0.6 µA, typical) helps prolong battery life, and the rail-to-rail output supports detection low currents.

Figure 4-7 shows a high -side battery current sensor circuit. The 10Ω resistor is sized to minimize power losses. The battery current (I_{DD}) through the 10Ω resistor causes its top terminal to be more negative than the bottom terminal. This keeps the Common-mode input voltage of the op amp below V_{DD}, which is within its allowed range. The output of the op amp will also be below V_{DD}, which is within its Maximum Output Voltage Swing specification.

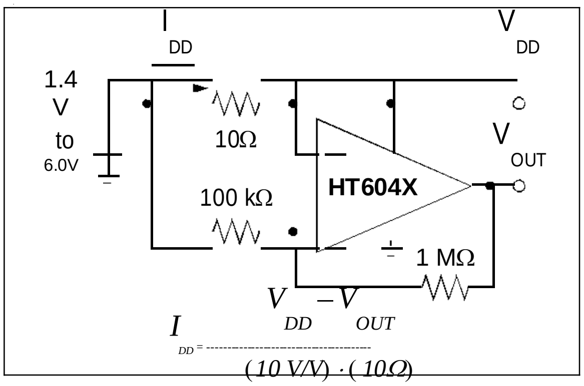


FIGURE 4-7: *High-Side Battery Current Sensor.*

4.9.2 INSTRUMENTATION AMPLIFIER

The HT6041/2/3/4 op amp is well suited for conditioning sensor signals in battery-powered applications. Figure 4-8 shows a two op amp instrumentation amplifier, using the HT6042, that works well for applications requiring rejection of Common-mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low impedance source. In single supply applications, V_{REF} is typically $V_{DD}/2$.

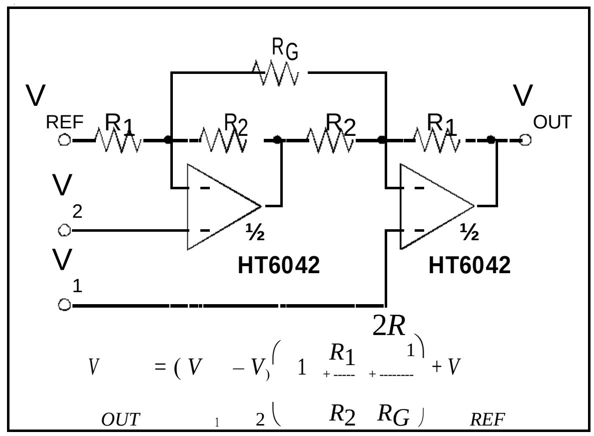
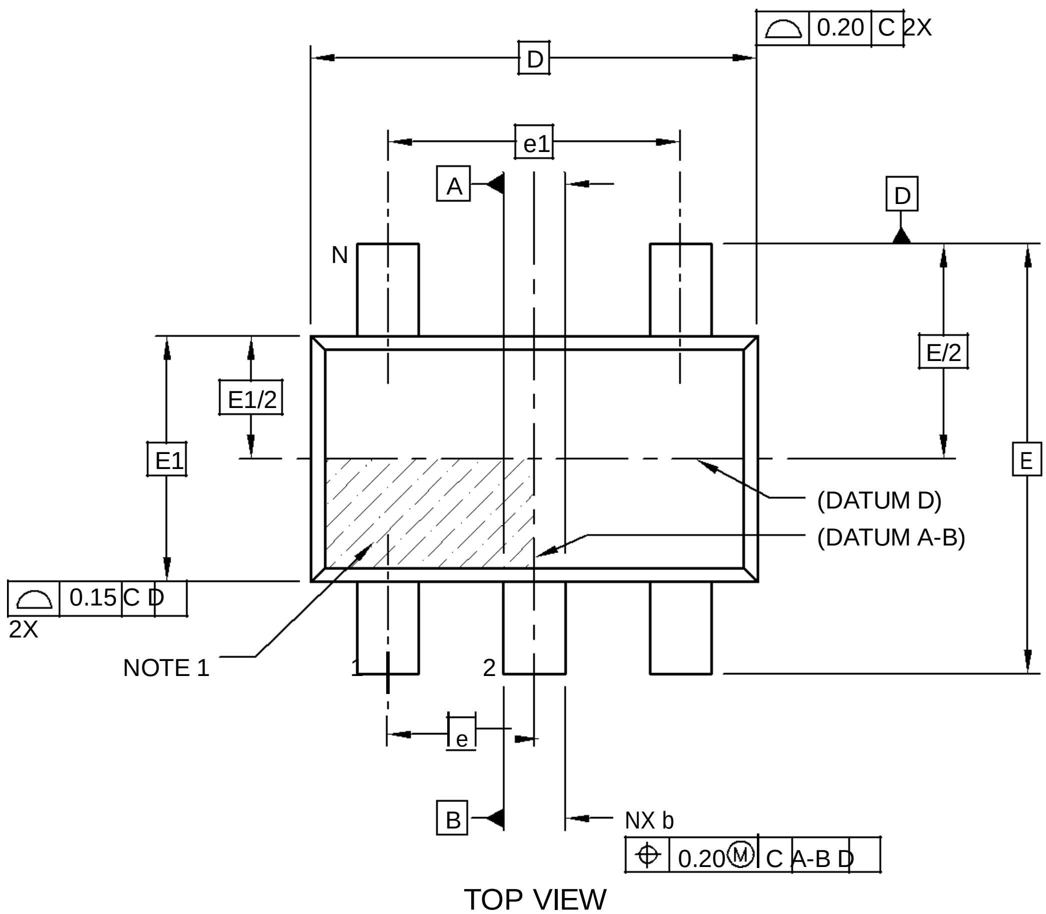
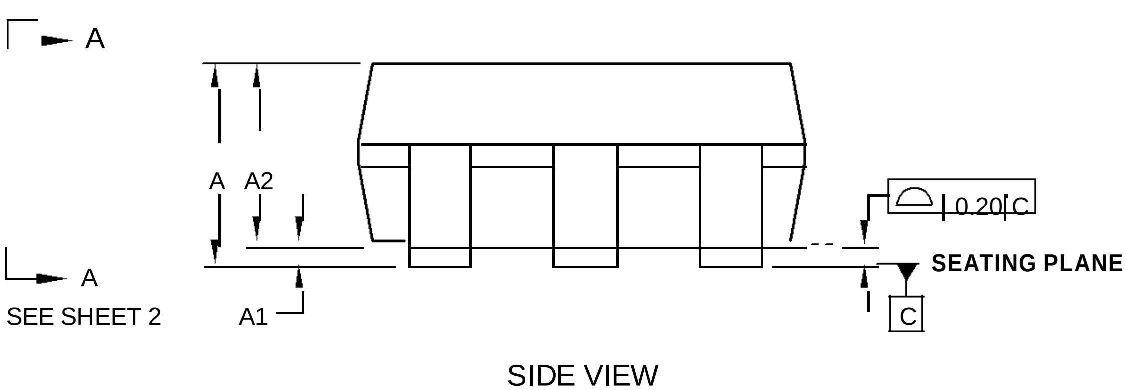


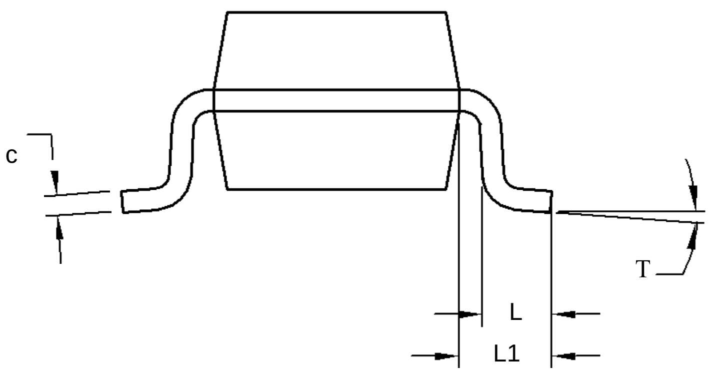
FIGURE 4-8: *Two Op Amp Instrumentation Amplifier.*

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

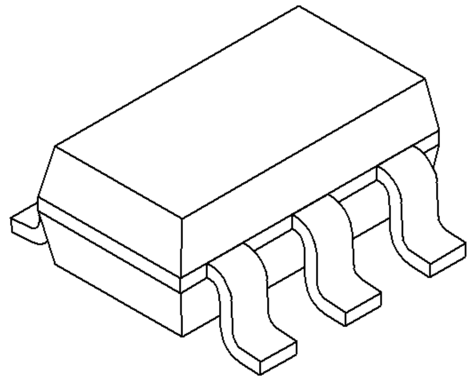




5-Lead Plastic Small Outline Transistor (OT) [SOT23]



VIEW A-A
SHEET 1

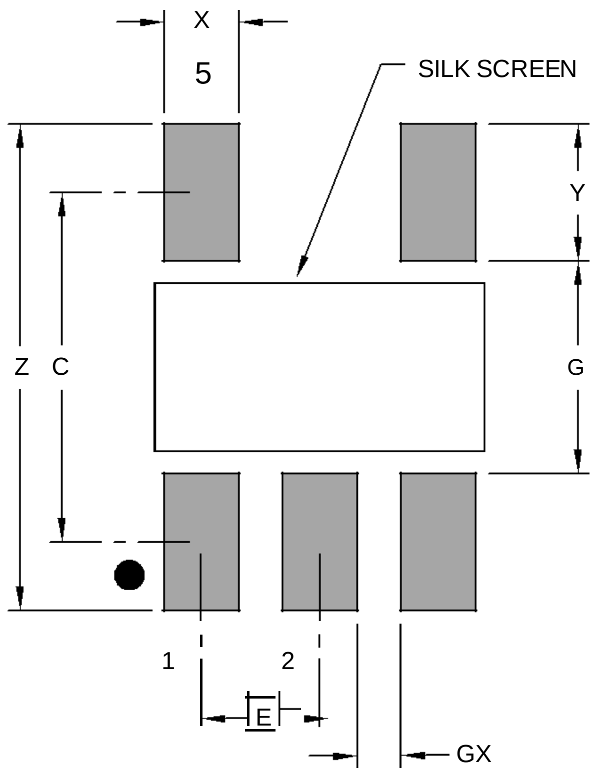


Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.95 BSC		
Outside lead pitch	e1	1.90 BSC		
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E	2.80 BSC		
Molded Package Width	E1	1.60 BSC		
Overall Length	D	2.90 BSC		
Foot Length	L	0.30	-	0.60
Footprint	L1	0.60 REF		
Foot Angle	I	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

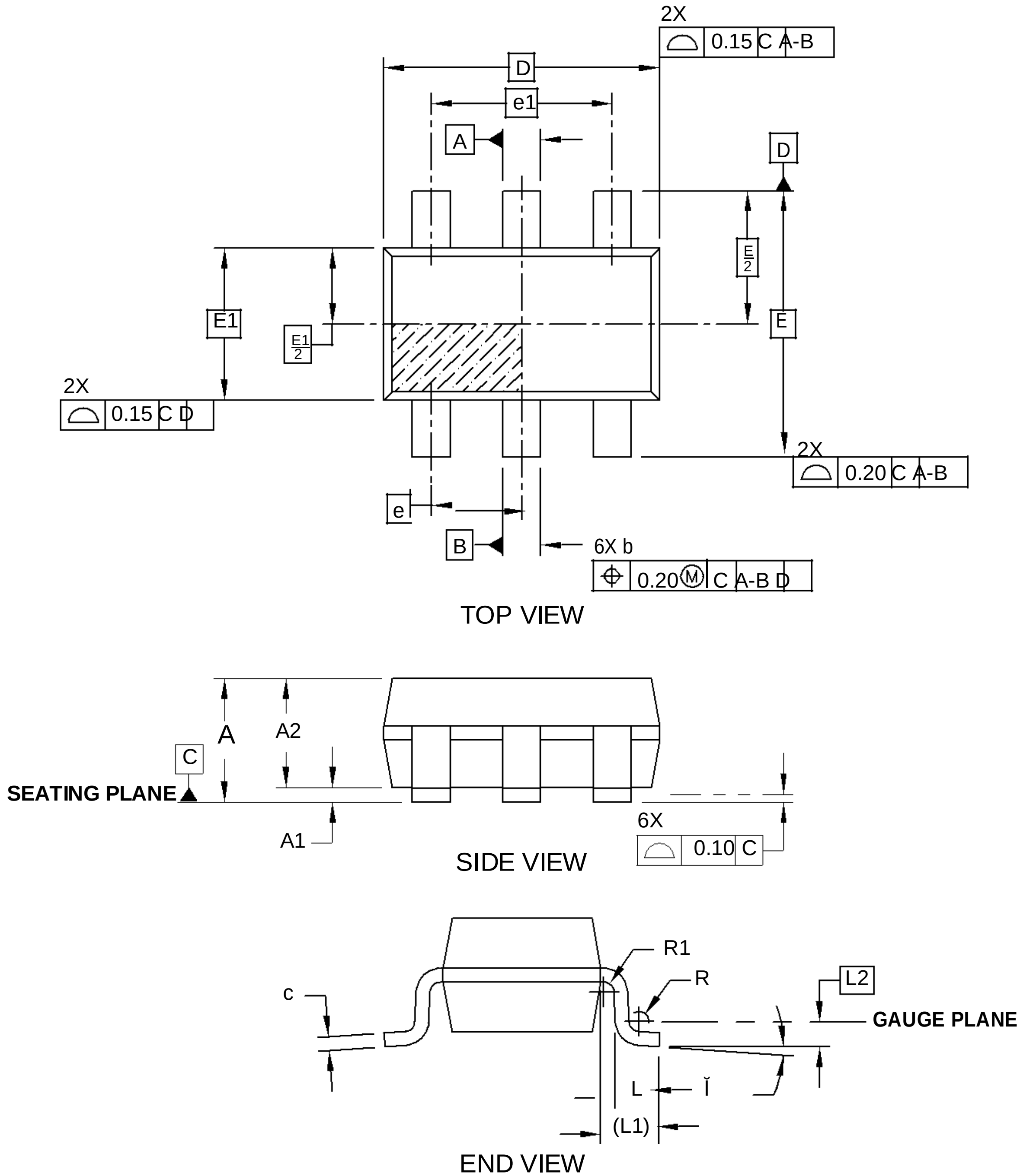
5-Lead Plastic Small Outline Transistor (OT) [SOT23]



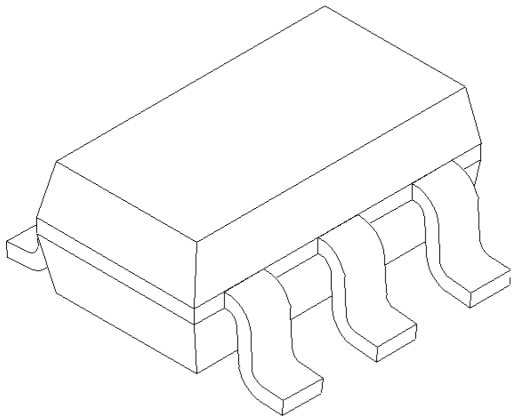
RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]



6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

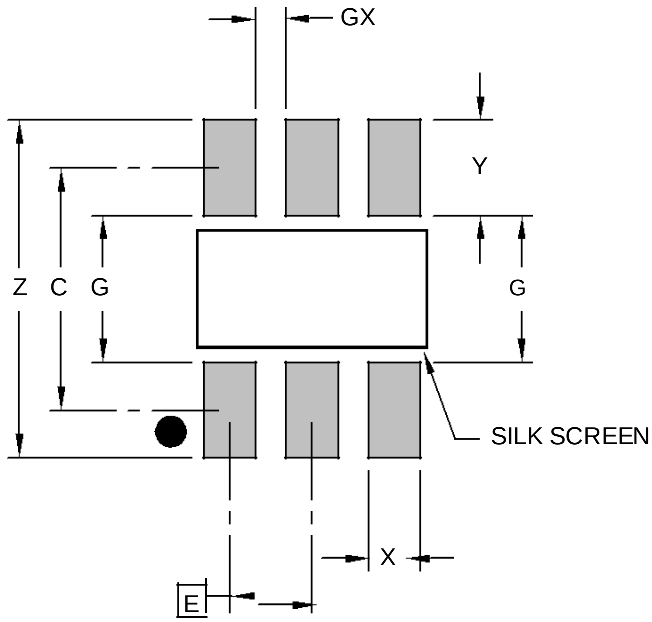


Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		6	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	1.15	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	0.45	0.60
Footprint	L1		0.60 REF	
Seating Plane to Gauge Plane	L1		0.25 BSC	
Foot Angle	φ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

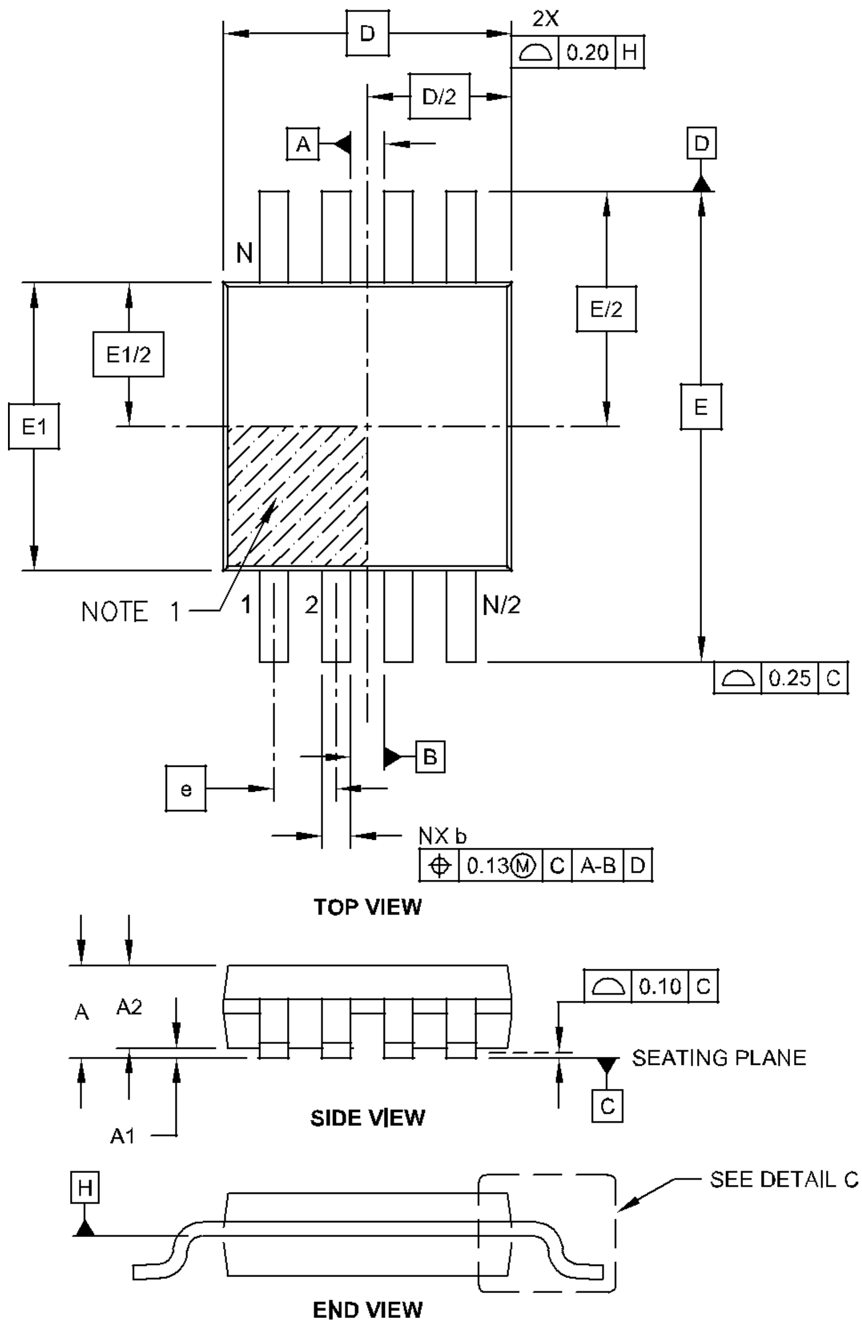
6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]



RECOMMENDED LAND PATTERN

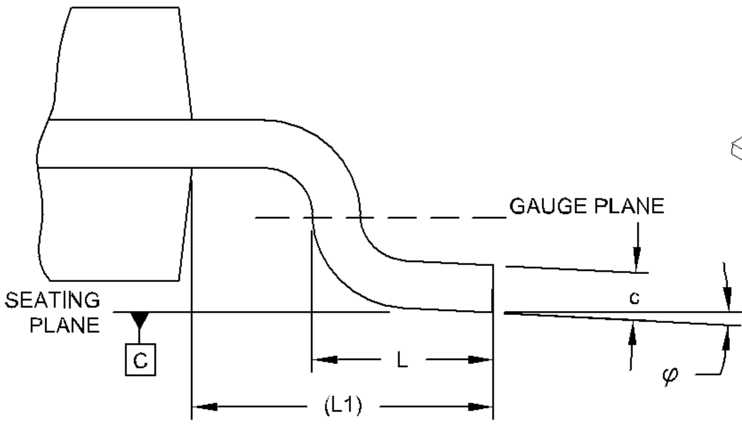
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X3)	X			0.60
Contact Pad Length (X3)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

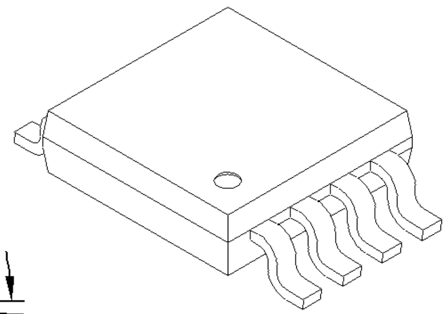


Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]



DETAIL C



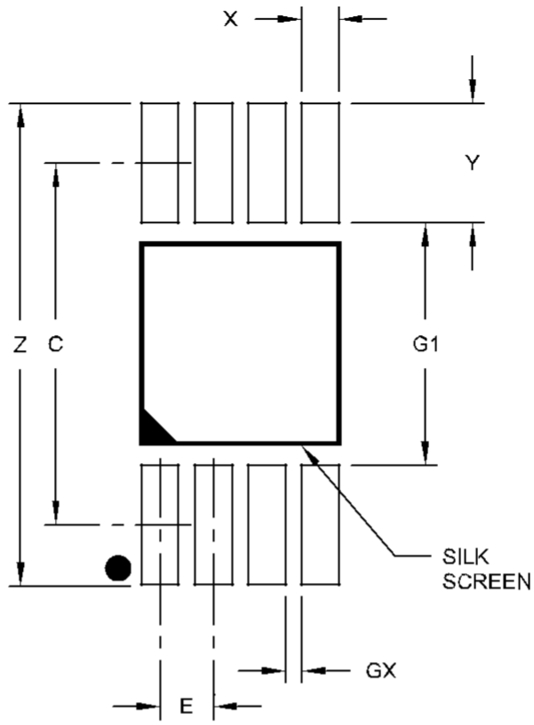
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]



RECOMMENDED LAND PATTERN

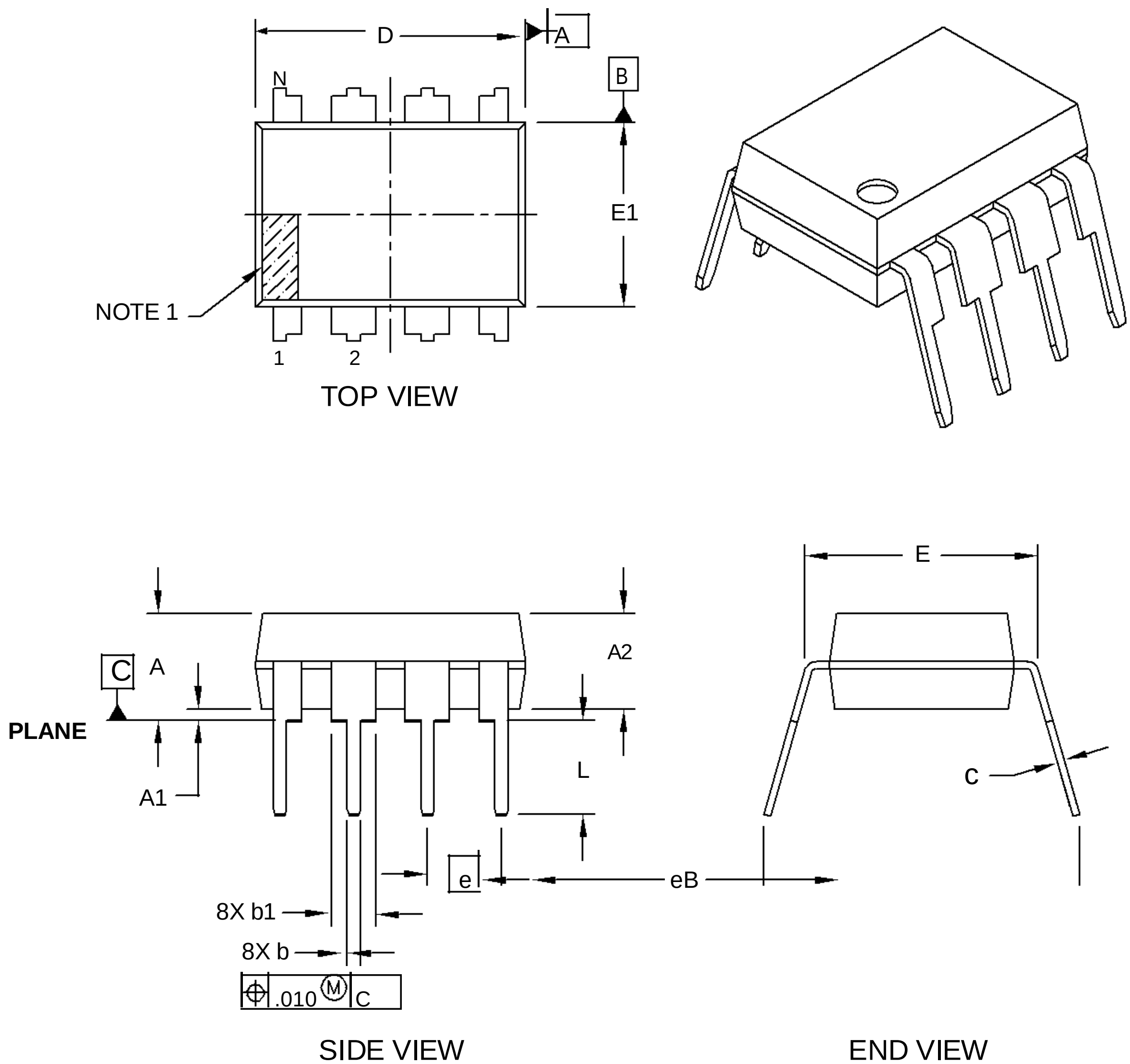
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

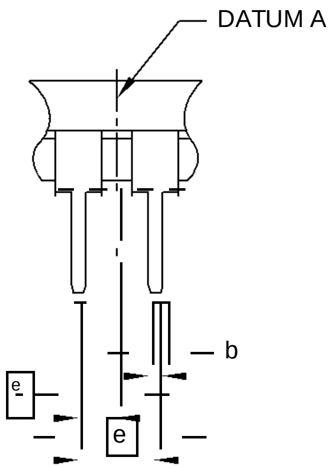
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

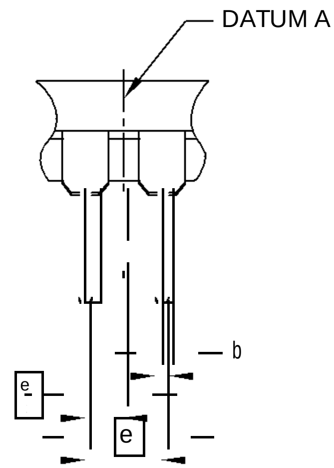
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]



8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]



ALTERNATE LEAD DESIGN
(NOTE 5)



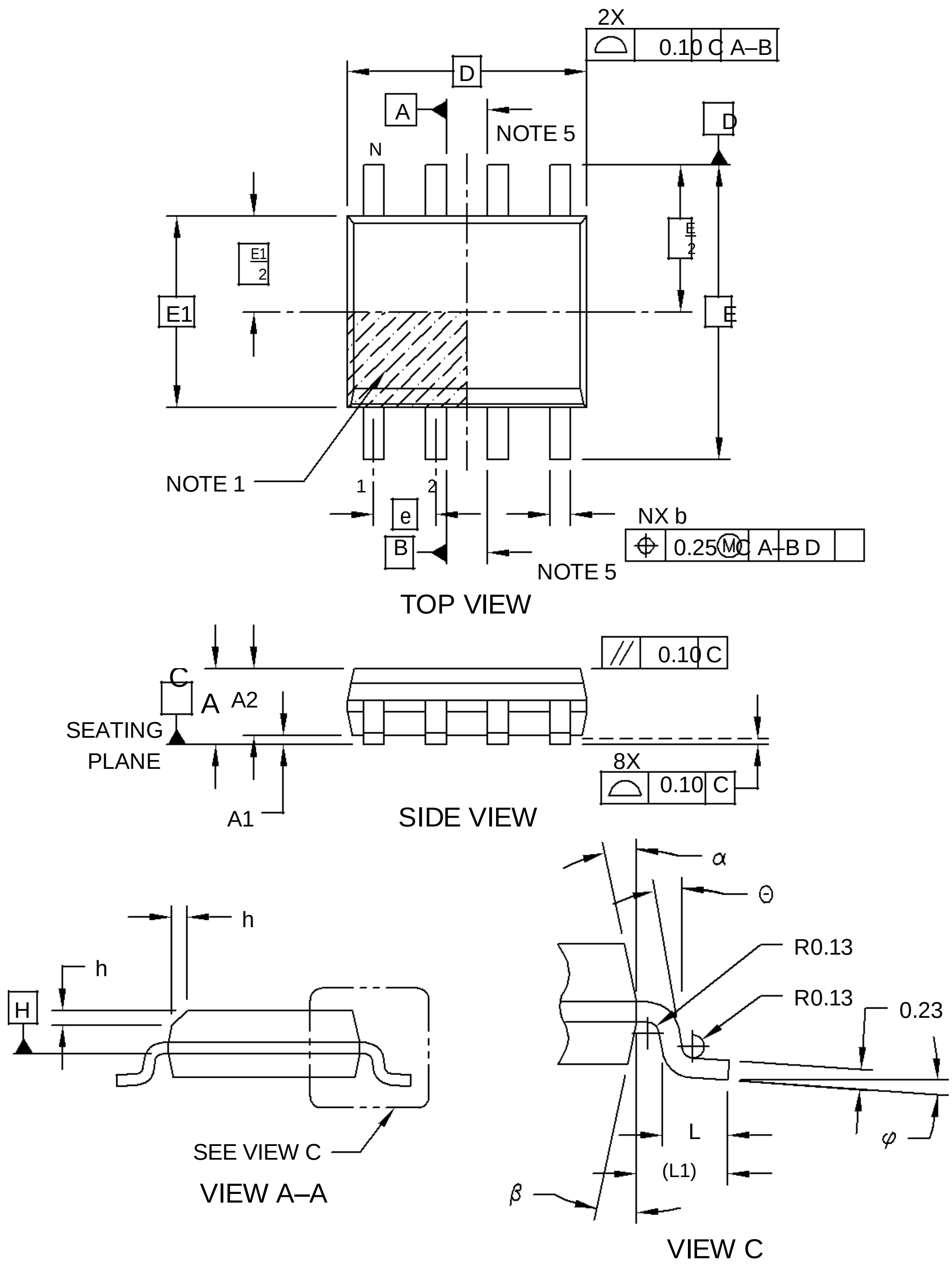
Units		INCHES		
Dimension Limits		MIN	NO M	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

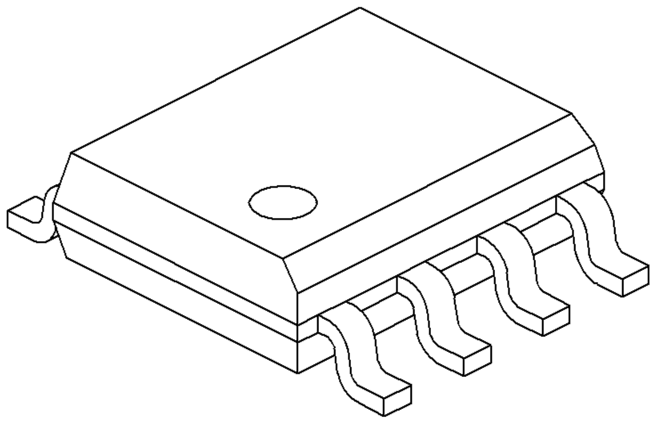
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]



8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

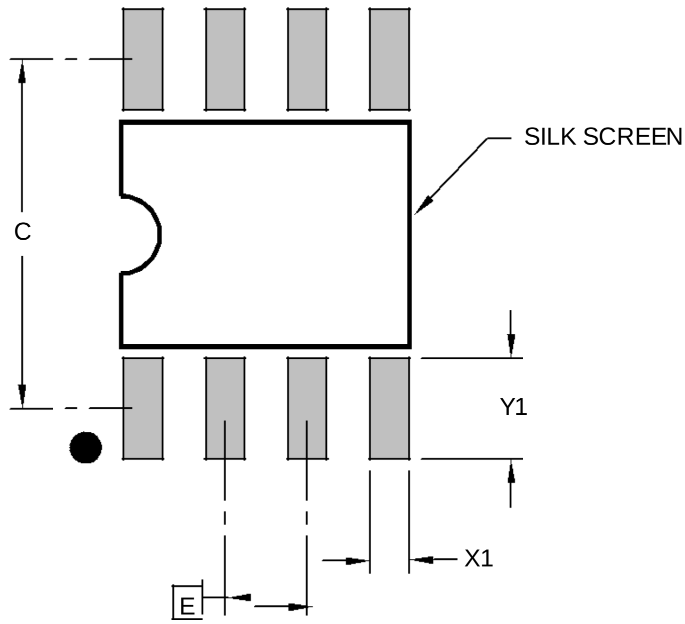
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]



RECOMMENDED LAND PATTERN

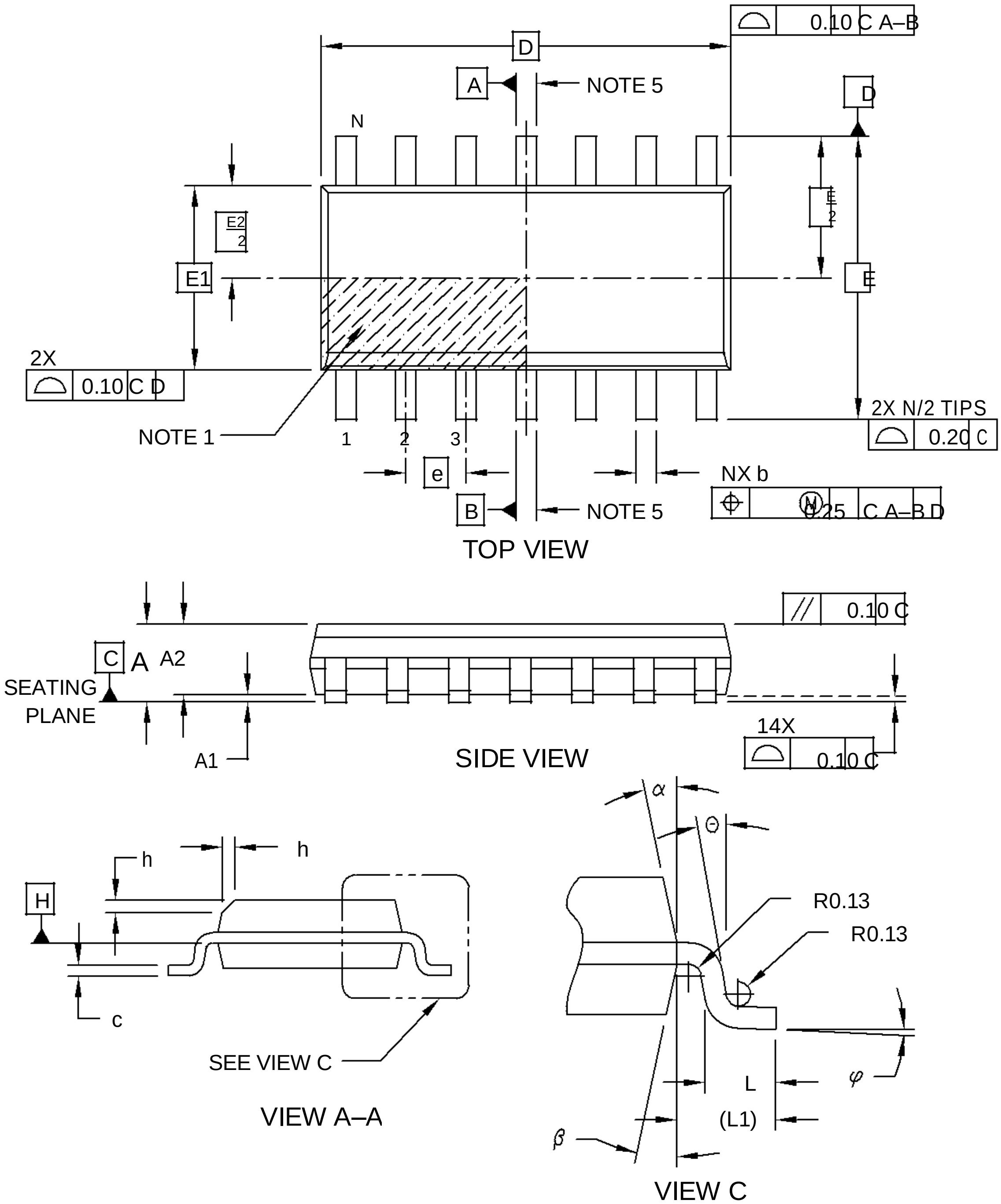
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

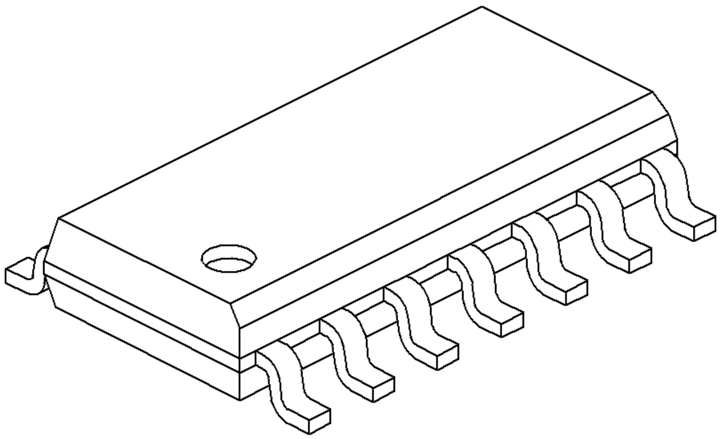
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]



14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

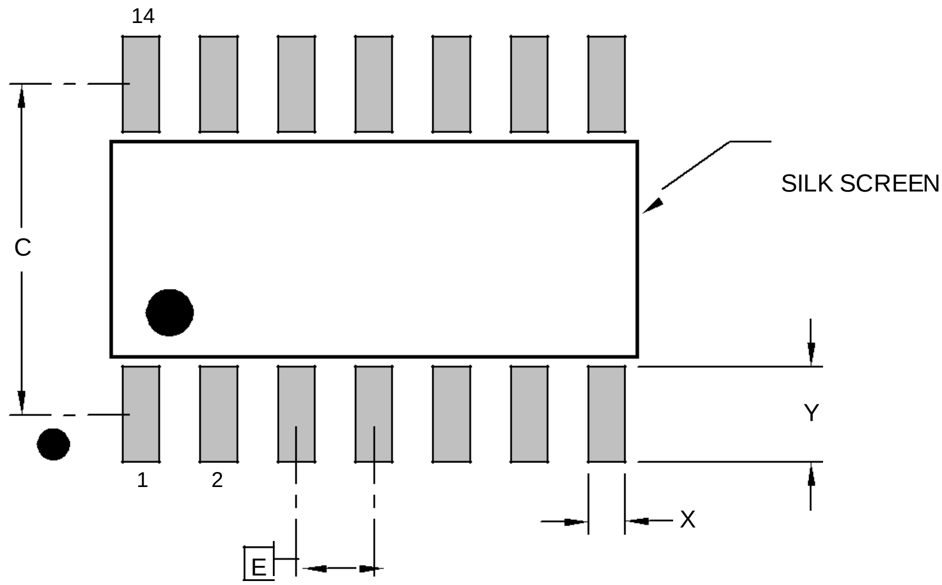
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]



RECOMMENDED LAND PATTERN

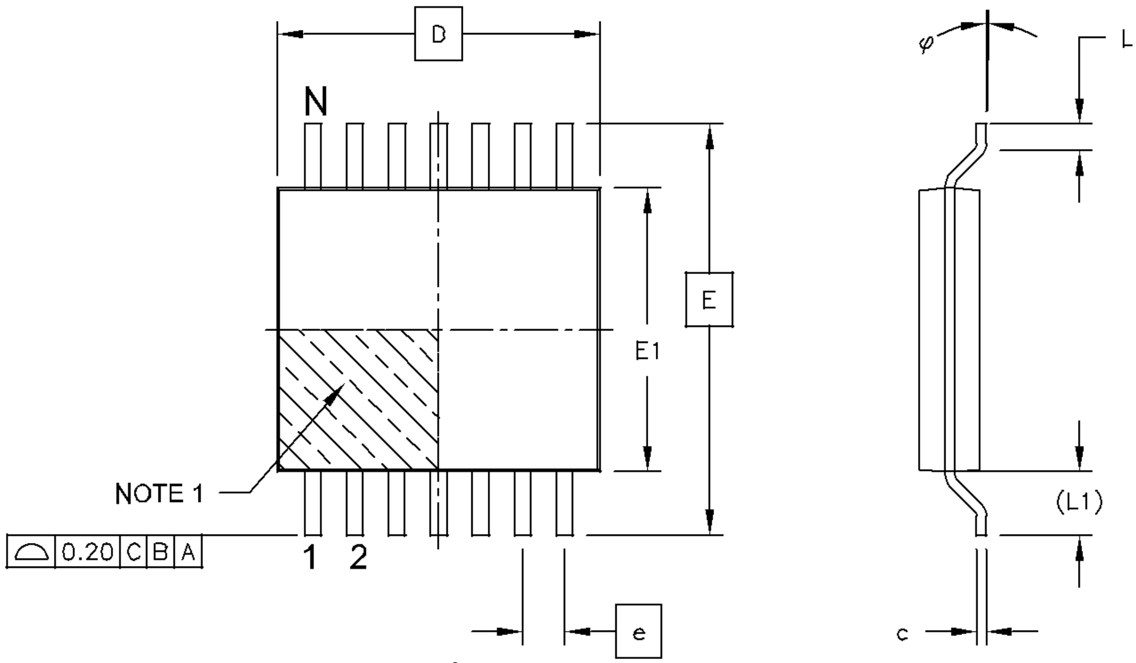
	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

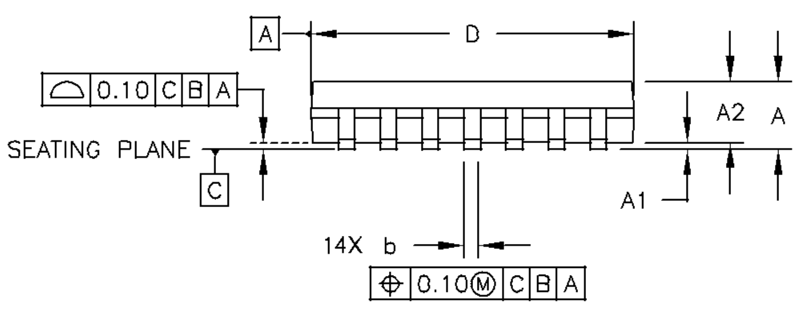
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

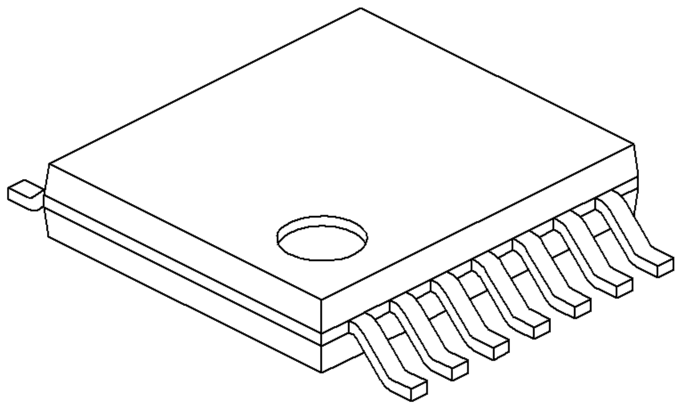


TOP VIEW



SIDE VIEW

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)		1.00 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

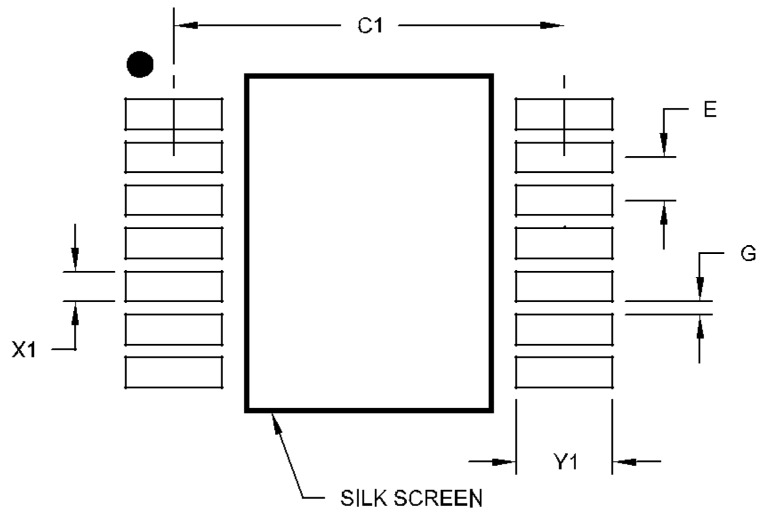
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes: