60V/3A Synchronous Step-Down Voltage Converter

Features

- 20-μA Quiescent current in regulation
- Input voltage range: 4V-60V
- Output voltage range: 1V-VIN
- Integrated upper and lower power MOSFET maximum current: 5A
- Adjustable frequency range: 200KHz~2MHz
- Automatic switching of CCM/DCM/PFM mode
- Adjustable soft-start time and Output voltage tracking capability
- Automatically switched bypass linear power supply
- Provides ultra-low input and output dropout voltage close to 100% duty cycle
- Internal Compensation
- Power-good flag
- Dynamic Frequency Stretch Technology
- Support large capacitive load start-up
- Protection function: UVLO/OCP/SCP/OTP/OVP
- Operating junction temperature range: -40℃ to +125℃
- All pins have ±2000V (HBM) ESD protection
- ETSSOP 16-Pin Exposed Pad Package

Applications

- Industrial power supply
- Wide voltage input range power supply
- Low ripple low noise power supply
- Automotive electronic power supply

Description

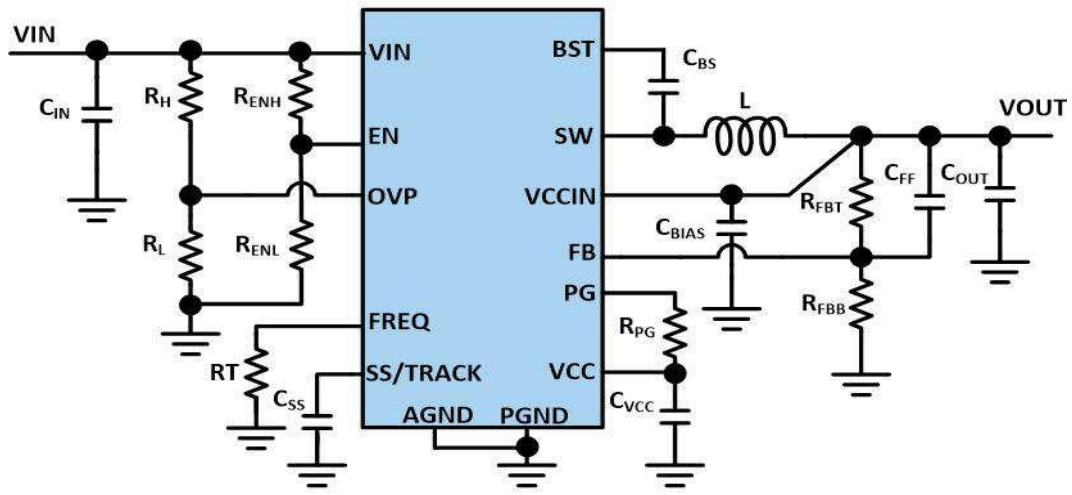
HT6050A is a step-down DC/DC regulator with an internal switch, featuring SKIP control mode, which combines low quiescent current with high switching frequency to achieve high-efficiency regulation over a wide range of load currents. SKIP mode uses a short "burst" cycle to switch the inductor current through the internal power MOSFET, followed by a sleep cycle in which the power switch is turned off and the load current is provided by the output capacitor. At light loads, burst cycles are a small fraction of the total cycle time, minimizing average supply current and greatly improving efficiency at light loads.

HT6050A has a wide input voltage range of 4V-60V, thus minimizing the need for external surge suppression components. Making it the best choice for wide input power range industrial and high cell count battery pack applications. HT6050A is ideal for use in the 48V automotive power bus range.

HT6050A features low-value 100mΩ high-side and 80mΩ low-side MOSFET that provide at least 3A output current capability with excellent load and line transient response.

Additional features include: soft-start, thermal shutdown, UVLO undervoltage lockout, gate driver undervoltage lockout, maximum duty cycle limit timer, and current limit shutdown timer. It also integrates output short-circuit protection, providing HICCUP mode when the FB voltage is low to avoid overheating during short-circuit.

Typical Application Circuit

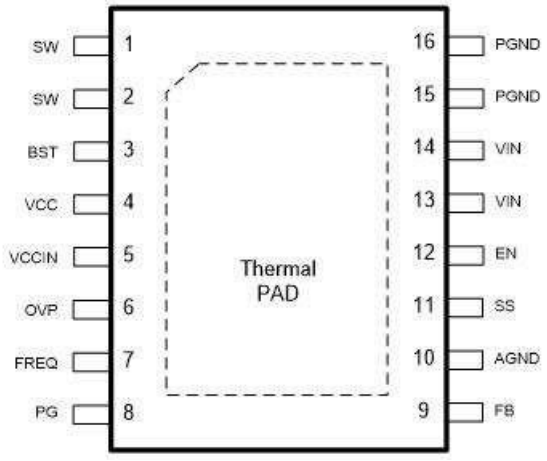


Absolute Maximum Ratings (†)

Parameter	Range
Pin to GND Voltage（VIN,SW,EN）	-0.3V~65V
Pin to GND Voltage（BST）	-0.3V~SW+5.5V
Pin to GND Voltage (FB,FREQ,SS, OVP, VCC)	-0.3~5.5V
Pin to GND Voltage (VCCIN, PG)	-0.3~36V
Storage temperature	-65℃ to 150℃
Operating temperature	-40℃ to 125℃
ESD Value（HBM）	±2KV
ESD Value（CDM）	±1KV

Pin arrangement

eTSSOP-16 Package



Top View

Pin number	pin name	instructions
1,2	SW	Internal power switch node. Externally connected to power inductor and CBST capacitor.
3	BST	Bootstrap drive power supply. High quality 100nF ceramic capacitors need to be connected between the BST and SW to bias the internal high voltage side gate driver.
4	VCC	A power supply to supply power to the internal control circuit. A 1uF~4.7uF ceramic decoupling capacitor must be connected between VCC and PGND, as close as possible to the chip pin. VCC is powered by VIN or VCCIN.
5	VCCIN	VCC is powered by VIN by default, If VCCIN conditions are suitable, it can be adaptively switched to VCCIN power supply to reduce the loss caused by VIN power supply. If not, the VCCIN can be grounded.
6	OVP	Overvoltage protection pin, connected to the output pin and ground divider resistance.
7	FREQ	Step-down transformer working frequency setting pin, a suitable resistance is connected between FREQ and PGND, and the switching frequency can be adjusted from 200KHz to 2MHz.
8	PG	Open-drain indicates that the output voltage of the step-down transformer is normal. When the output is normal, PG stops pulling down.
9	FB	Output voltage feedback pin. The output voltage can be adjusted by configuring the partial voltage ratio between VOUT and PGND.
10	GND	Chip simulates ground pins.
11	SS/TRACK	Soft start and voltage tracking pins. The voltage of this pin is used to set the reference source of the control loop. When internal soft start is selected, the pin should be suspended; When selecting soft start with external control, connect appropriate capacitor between SS/TRACK and PGND; When choosing to use voltage tracing, connect SS/TRK to the voltage source to be traced.
12	EN	Voltage regulator output enable pin, set high enable output. The undervoltage protection of VIN can be set by configuring the external resistor divider.
13,14	VIN	Voltage regulator power input. Use a ceramic capacitor of 2.2 μF or larger as close as possible to the bypass VIN to PGND.
15,16	PGND	Power ground pins, which are connected to VIN with one or more decoupled ceramic capacitors, as close to the pins as possible.
EP	GND	Metal heat sink, connected to PGND.

Technical specifications

Limits apply to operating junction temperatures (T_J) ranging from -40℃ to +125℃ unless otherwise specified. Minimum and maximum limits are specified by test, design or statistical correlation. Typical values represent the most likely parameter specifications when T_J=25℃, for reference only. All voltages are relative to GND.

Table 3.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Characteristics						
V_{IN}	Operating Input Voltage Range		4		60	V
V_{IN_GD}	VIN undervoltage lock	Rising		4		V
		Falling		3.6		V
V_{CCIN_GD}	VCCIN power good	Rising		3.9		V
		Falling		3.5		V
I_{Q_VIN}	VIN Operating quiescent current	V_{IN}=EN=24V, V_{FB}=1.2V V_{CCIN}= 5V, No switch		10	12	uA
I_{Q_VCCIN}	VCCIN Operating quiescent current	V_{IN}=EN=24V, V_{FB}=1.2V V_{CCIN}= 5V, No switch		50	60	uA
I_Q	VIN Equivalent quiescent current	V_{IN}=EN=24V V_{CCIN}= V_{OUT}=5V, No switch		25		uA
I_{SD}	Shutdown quiescent current	EN=0, V_{IN}=60V			2	uA
VCC Characteristics						
V_{CC}	VCC output voltage	VIN=24V	4.8	5.0	5.2	V
V_{CC_GD}	VCC undervoltage protection	Rising		3.5		V
		Falling		3.2		V
I_{SC_VCC1}	VCC short circuit current (VIN supply)	VIN=24V，VCCIN=0V		20		mA
I_{SC_VCC2}	VCC short circuit current (VCCIN supply)	VIN=VCCIN=24V，		20		mA
FB PIN						
V_{FB_acc}	FB feedback voltage		0.99	1.0	1.01	V
V_{FB_GD}	FB good threshold value		0.83	0.85	0.87	V
V_{FB_OV}	FB Over voltage threshold		1.12	1.15	1.18	V
V_{FB_skip}	FB Jump period threshold			1.003		V
I_{FB_leak}	FB The leakage current				30	nA
PWM Related						
R_{DS_HS}	High-side MOSFET ON-resistance	TJ= 25℃		100	160	mΩ
R_{DS_LS}	Low-side MOSFET ON-resistance	TJ= 25℃		80	130	mΩ
I_{Peak_HS}	HS Current limit		3.8	4.2	4.8	A
I_{Peak_LS}	LS Current limit		4	4.5	5	A
I_{ZCD}	LS Current zero			50		mA
$I_{SW.LKG}$	SW Leakage current				1	uA
F_{SW}	Switching frequency	PWM Operation	0.9	1.0	1.1	MHz

	accuracy	R_{FREQ} = 62k Ω				
F_{SW_range}	Switching frequency range	with 1% R_{FREQ}	0.2		2.0	MHz
D_{MAX}	Maximum duty cycle	VIN=12V，VOUT=11.9V	99			%
Tss	Soft start time		200	300	400	us
$T_{HSON.MIN}$	HS Minimum turn-on time			80	110	ns
$T_{HSON.MAX}$	HS Maximum conduction time			8.0		us
$T_{LSON.MIN}$	LS Minimum turn-on time			60	100	ns
tss	Soft start time			400		us
T_{SCP_HOLD}	Trigger time of short circuit protection			3		ms
T_{SCP_HICCUP}	Short circuit protection hiccup waiting time			6		ms
EN PIN						
V_{EN_H}	EN High logic threshold		1.1			V
V_{EN_L}	EN LOW logic threshold				0.5	V
$V_{EN\_UV\_R}$	EN Undervoltage protection rising edge		1.19	1.2	1.21	V
$V_{EN\_UV\_F}$	EN Undervoltage protection falling edge		1.14	1.15	1.16	V
I_{LKG-EN}	EN Input current	EN < 60V			1	uA
Thermal protection characteristic						
T_{OTP-R}	Over temperature protection	T_J Rising		160		℃
T_{OTP-F}	The overtemperature protection is removed	T_J Falling		145		℃
Thermal resistance coefficient						
θ_{JA}	The thermal resistance coefficient from the silicon core to the surrounding air	0 LFPM Air Flow		TBD		℃/W
θ_{JB}	Thermal resistance coefficient between silicon core and PCB surface			TBD		℃/W
θ_{JCtop}	Thermal resistance coefficient of silicon core to upper surface of package			TBD		℃/W
Ψ_{JB}	Thermal resistance coefficient between silicon core and PCB surface			TBD		℃/W

Functional block diagram

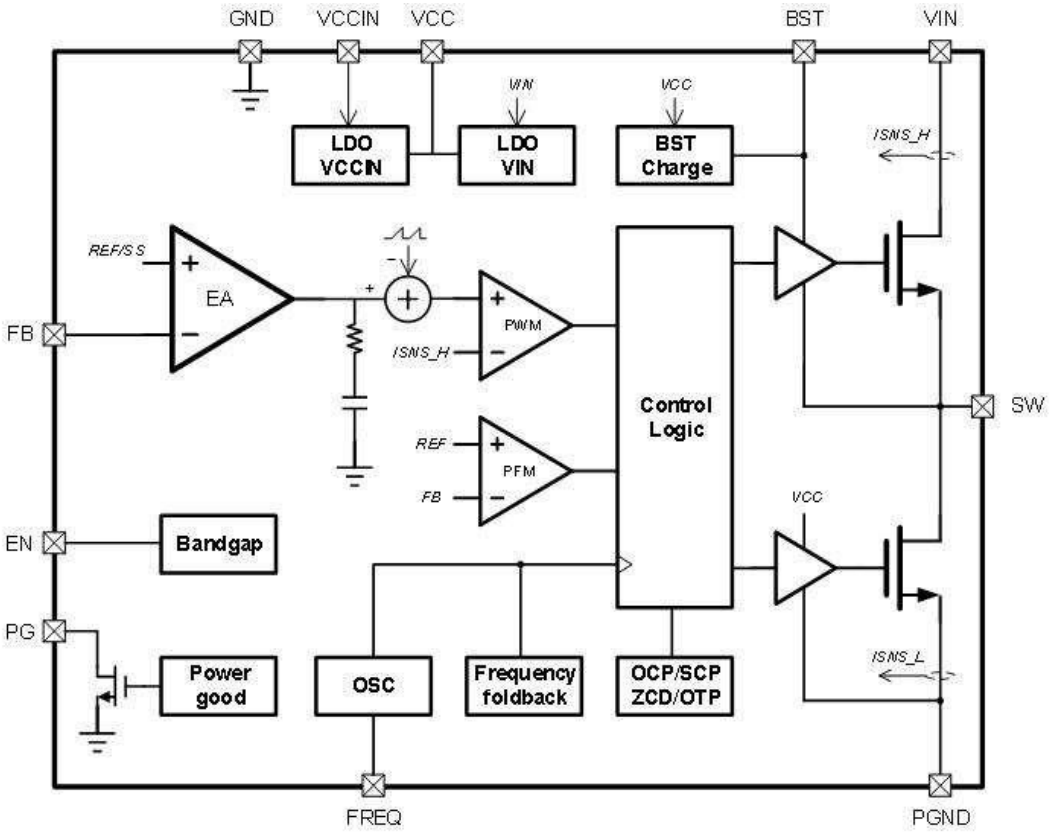


figure. 4 Internal function block diagram

Overview

HT6050A is a high efficiency, high power density synchronous buck converter. The chip has an input voltage range of 4V to 60V, and is internally integrated with upper and lower power Mos tubes, which can output up to 3A load current. And can provide a stable output voltage from 1V to VIN.

HT6050A has SKIP control mode, which combines low static current with high switching frequency to achieve high efficiency over a wide range of load current. Fixed frequency peak current control mode with integrated internal compensation is adopted to shorten design time and require fewer external devices. HT6050A adjusts the switching frequency from 200kHz to 2MHz through an external resistor. The wide switching frequency range allows the chip to be optimized for small volume requirements at higher frequencies or efficient power supplies at lower frequencies. In addition, HT6050A can operate at close to 100% of the maximum duty cycle to achieve the best possible input-output differential pressure. HT6050A integrates a bypass LDO linear power supply, which can be connected to an external low-voltage power supply to generate VCC, further improving the chip's light-load efficiency under high voltage input conditions. The chip provides the automatic detection and switching circuit of bypass LDO. When the bypass LDO is directly connected to VOUT and the VOUT rises above the switching threshold, the internal LDO input power can be seamlessly switched from VIN to VOUT.

HT6050A also offers a variety of other features, including an external resistor to adjust the output voltage, a choice of built-in soft start or external adjustable soft start, an output voltage follow function, and a good sign of power supply. Protection features include periodic peak and trough current limiting, output short-circuit protection in Hiccup mode, input overvoltage protection for hot swap applications, thermal turn-off and self-recovery, and precise input undervoltage protection.

EN enable

EN pin voltage control HT6050A internal VCC LDO linear power supply and synchronous buck converter output VOUT on and off. When V_{EN} is lower than V_{EN_L}, the chip enters the shutdown mode to maintain the low-power standby state. At this time, the maximum input current of the chip will not exceed 2uA.

The EN pin has a precise threshold, V_{EN_UV}, to control the startup and shutdown of HT6050A. When the EN voltage rises above this threshold, the chip output is allowed. In practical applications, two resistors are connected in series between VIN and PGND pins, and the center point of the two resistors is connected to EN pins, and the adjustable input UVLO protection is realized through the two resistors. The UVLO value can be determined by the following formula:

Internal LDO linear power supply, VCC and VCCIN pin

HT6050A integrates an LDO linear power supply to provide VCC power for the control circuit and MOSFET drive. The VCC has a nominal voltage of 5V and the pin must be connected to PGND as close to the pin as possible via a ceramic decoupling capacitor of 1uF-4.7uF. The internal LDO has two inputs: one from VIN and one from VCCIN pins. When THE VCCIN voltage is higher than the switchover threshold, the VCCIN input supplies power to THE LDO. The power loss of LDO can be calculated by the following formula:

The greater the pressure difference between the input and output voltages of LDO, the greater the loss. The VCCIN input is designed to reduce the voltage difference between the input and output voltage of the LDO to reduce power losses and improve efficiency, especially under light load. When VCCIN is not used as LDO linear power input, connect VCCIN directly to PGND.

The output voltage VOUT and FB pin

HT6050A voltage regulation loop will adjust the FB voltage to be the same as the internal reference voltage, and the output voltage can be adjusted by changing the resistance ratio of the upper divider R_{FBT} to the lower divider R_{FBB}. Connect the resistance divider between the output node and ground, with the middle point connected to the FB pin. The steady-state voltage of V_{FB} is usually 1V. R_{FBB} can be calculated by the following formula:

The choice of R_{FBB} depends on the application environment. A large divider resistance can reduce the current flowing over the overvoltage network, but a large resistance makes the feedback loop more susceptible to noise. It is recommended that the R_{FBB} be set to a maximum of 1MΩ . Large precision error and temperature coefficient affect the control precision of output voltage. It is recommended to use a resistor with precision error less than 1% and temperature coefficient less than 100ppm.

The feedback loop should be kept away from the interference of PCB noise. Refer to the PCB layout for reference.

internal compensation and CFF

HT6050A internal compensation makes the chip stable over the entire operating frequency and output voltage range. Depending on the output voltage, the phase margin of the compensation loop may be low. It is recommended that an external feedforward capacitor, C_{FF}, be connected in parallel with an upper divider, $R_{FBT,}$ for optimal transient performance. See figure 5 for details.

The feedforward capacitor C_{FF} is in parallel with R_{FBT}, and zero is added before the crossing frequency of the control loop to improve the phase margin. The zero frequency can be obtained by the following formula:

$$\frac{1}{2}$$

At the same time, poles are introduced, and the frequency of poles is:

$$\frac{1}{2 \quad //}$$

Different output capacitor combination designs require different C_{FF}. Different types of capacitors have different equivalent series resistance (ESR). Ceramic capacitors have minimum ESR and highest C_{FF} requirements. Electrolytic capacitors have larger ESR, and the zero frequency produced by ESR will be low enough to increase

the phase prior to frequency crossing. Designs using large ESR capacitors at the output may not require any $C_{FF,}$ and the zero ESR frequency is as follows: $\frac{1}{2}$

Application information: Feature Description

Power supply normal mark (Power Good)

PG pin is connected to the drain of an internal MOSFET. The PG pin needs to be pulled up to the VCC or external power supply by an external resistor. The voltage detected by the PG pin shall not exceed 12V. A resistance divider may be used to divide voltage from higher voltages. Pull-up resistors typically range from 10kΩ to 100kΩ. When the FB voltage is within the normal range of the power supply, the PG internal MOSFET is off and the PG pin is in a high level state. Conversely, when the FB voltage exceeds the normal output tolerance range, usually +15% above the internal reference voltage or -15% below, the PG pin internal MOSFET is turned on and the PG pin voltage is pulled down to indicate a power supply failure. To prevent burrs from affecting THE PG function, there is a 320us delay for both the PG pin pull up and pull down.

Soft start and output voltage tracking function

HT6050A allows internal soft start or external soft start. The SS/TRK pins should be suspended when internal soft start is selected, and HT6050A uses internal soft start control to output oblique waves, usually starting to a stable output voltage around 300us. In applications with large output capacitors, high output voltages, or other special requirements, a C_{SS} capacitor can be connected to this pin to AGND to extend soft start time. Extending the soft start time further reduces the current required to charge the output capacitor and provide the output load. HT6050A has an internal 2.6uA constant current source to charge the C_{SS} capacitor, so the external soft start time can be calculated by the following formula:

HT6050A can use this pin to follow the output voltage to the external power supply. When this function is required, connect the SS/TRK pin to the voltage source to be tracked, and the V_{FB} will follow the voltage V_{SS} applied to the SS/TRK pin. When the V_{SS} is greater than 1V, the V_{FB} is controlled at an internal reference voltage of 1V.

HT6050A can be started with pre-biased output. When the inductance current reaches zero, the lower tube is turned off to avoid negative current conduction. This mode of operation is also called diode simulation mode. With a pre-biased output voltage, HT6050A waits until the soft-start ramp allows adjustment above the pre-biased voltage, and then follows the soft-start ramp to the adjustment level.

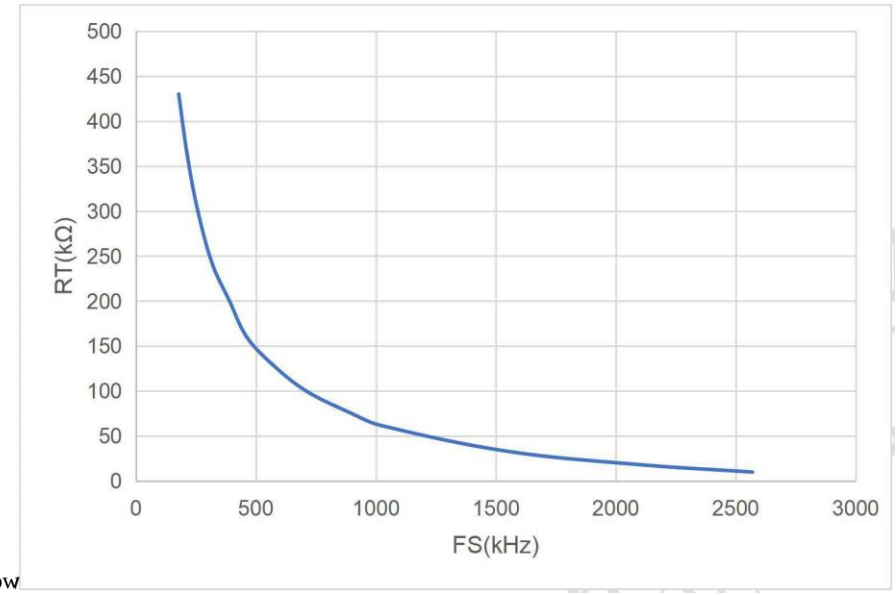
Switching frequency and FREQ pin

The switching frequency of HT6050A can be determined by the external resistor R_T connected between FREQ pins and AGND, which ranges from 200kHz to 2.5MHz. R_T can be calculated by the following formula:

( ) $\frac{81053}{}$ 21

Application information: Feature Description

The relation curve between R_T resistance and switching frequency is shown in the figure below



For common switching frequencies, R_T Settings can be referred to the following table

R_T(kΩ)	Fs(kHz)
10	2500
18	2100
33	1500
62	1000
160	500
200	400
470	200

BST and SW pin

HT6050A requires a small ceramic capacitor between the BST and SW pins to provide the gate drive voltage for the high-side MOSFET. When the high side MOSFET is off and the low side MOSFET is on, the C_{BST} capacitor charges. The ceramic capacitor shall have a maximum of 0.47uF and be connected between BST and SW for proper operation. Class X7R or X5R dielectric ceramic capacitors are recommended because of their stable temperature and voltage characteristics. Ceramic capacitors shall be rated at 16V or higher.

Low Drop-Out mode

When the input voltage approaches the set output voltage, HT6050A enters the Low drop-out mode. At this point, the switching time of a single period of the high-side power tube is allowed to exceed the set switching period, and the switching time is automatically adjusted with the input voltage to maintain the control of the output voltage. When the input voltage is lower than the set output voltage, the maximum conduction time of the high-side power tube is limited to $T_{HSON.MAX}$. At this time, the low-side power tube will temporarily conduct $T_{LSON.MIN}$ to realize charging of C_{BST}. Ensure that the C_{BST} has enough voltage to maintain the normal operation of the high side power tube drive circuit.

Overcurrent protection and short circuit protection

HT6050A prevents overcurrent conditions by periodic limits on peak and trough values of inductive current. If the overcurrent condition persists, the hiccup mode will be triggered to prevent the chip from overheating.

High - side MOSFET overcurrent protection is achieved by the characteristics of peak current control mode. The output of the error amplifier after subtracting the oblique wave compensation for each switching period is compared with the current of the high side power tube sampled, please refer to the functional block diagram for details. Therefore, the peak current of the high-side power tube is restricted by the maximum output of the error amplifier, so as to achieve the ability of periodic peak current limitation

HT6050A detects the current of the low-side power tube and compares it with the valley bottom current limiting threshold during low-side MOSFET conduction. When the current of the low-side power tube is higher than the bottom current limiting threshold, the high-side power tube is not allowed to run until the low-side power tube is lower than the bottom current limiting threshold.

HT6050A enters Hiccup mode when the high-side power tube current triggers the error amplifier limit and the power supply normal indicator is pulled down. At this point, the chip will shut down the output and hold for 5ms, then the chip will try to restart. If the overcurrent or short circuit fault state still exists, the hiccup will be repeated until the fault state is over. Hiccup mode reduces power consumption under severe overcurrent or short circuit conditions and prevents overheating from damaging the chip.

Over temperature protection

The thermal overload protection circuit limits the junction temperature to below 160℃ (typical value). Under extreme conditions (high ambient temperature and/or high power consumption), when junction temperature begins to rise above 160℃, overtemperature protection is activated and the system will forcibly shut down the regulator output. When the junction temperature drops below 145℃, the OTP state will be unlocked, the regulator output will be turned on again, and the output current will return to normal operating value. Thermal overload protection is designed to protect the device from transient accidental overload conditions.

The device has a guaranteed operating junction temperature range of -40℃ to 125℃. High junction temperature will reduce the working life; The device life is shortened when the junction temperature is 125℃ for a long time. Please note that the maximum ambient temperature consistent with these specifications depends on the specific operating conditions as well as the PCB layout, package thermal rating, and other environmental factors.

Junction temperature (T_J, unit:℃) is calculated according to the ambient temperature (T_A, unit:℃) and power consumption (P_D, unit: W). The calculation formula is as follows:

( )

(unit:℃/W) is the thermal resistance of packaging.

input undervoltage locked

When VIN voltage falls below the UVLO drop threshold, UVLO protection is triggered, shutting down the regulator output. The rise threshold of the UVLO is about 4V, and when VIN reaches the voltage above this, the controller will enter the soft start process after removing the UVLO.

SKIP pulse mode

HT6050A built-in pulse hopping circuit; In light load, the circuit is closed; Switch only when necessary to keep the output voltage within the specified range. This reduces switching losses and allows the driver to remain efficient under light loads.

In pulse-jump mode, when the output voltage falls below a specified value, HT6050A enters PWM mode and stays for several oscillator cycles to bring the output voltage up to a specified range. During the waiting time between bursts of pulses, the power switch is switched off and the output capacitor provides all the load current. The output voltage ripple in this mode is larger than that in PWM mode because the output voltage will drop and recover irregularly.

Fully functional application circuit diagram

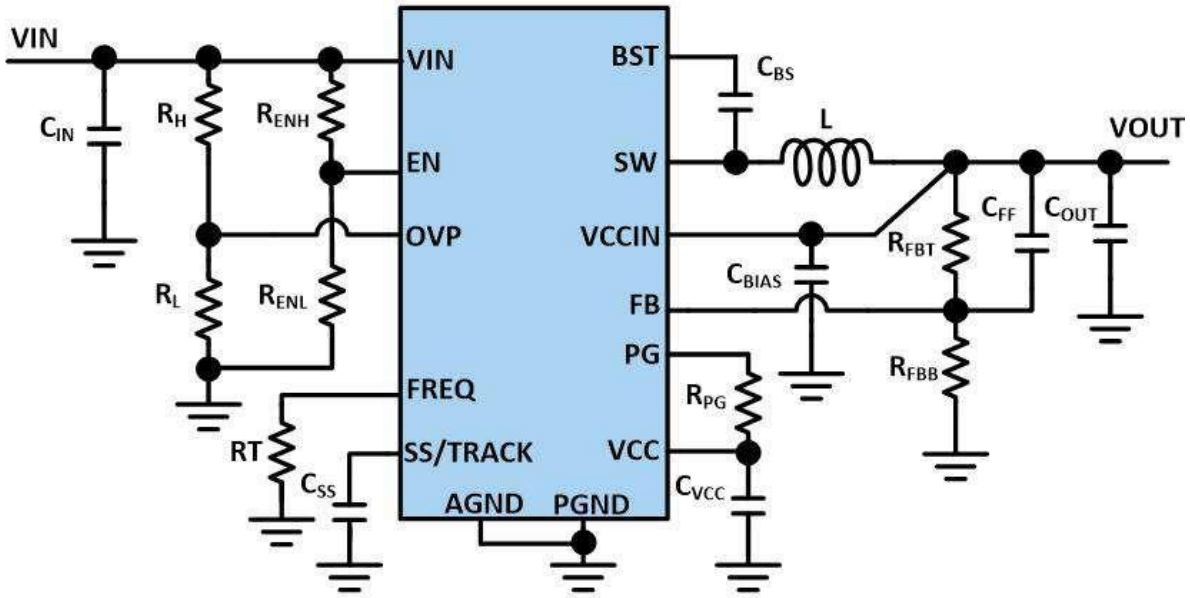


Figure 5. A Typical application topology in DC-DC buck mode

NOTE:

(1) It is recommended to use 10uF X7R or X5R ceramic capacitor for input capacitor, and place it as close as possible to power input pins 4 and 5

(2) For C_{BST}, please select a ceramic capacitor with a voltage withstand of more than 16V and place it as close to pins 1 and 6 as possible

Table of external devices for typical applications

R_{FREQ}(kΩ)	V_{OUT}(V)	V_{IN_Range} (V)	C_{OUT}(uF)(3)	L(uH)(2)	R_{FBT}(kΩ)(5)	R_{FBB}(kΩ)(5)	C_{ff}(pF)(6)
Fs=2MHz							
18.7kΩ	3.3	4-15(1)	47	2.2	100	43.2	47
	5	5-24(1)	47	2.2	100	24.9	47
	12	12-60(4)	22	8.2	100	9.09	NA
	24	24-60(4)	22	15	100	4.32	NA
Fs=1MHz							
64.9kΩ	1	4-9(1)	100	2.2	Short	Open	Short
	3.3	4-30(1)	100	6.8	100	43.2	47
	5	5-60	100	8.2	100	24.9	47
	12	12-60	22	18	100	9.09	NA
	24	24-60	22	27	100	4.32	NA
Fs=400kHz							
200kΩ	1	4-21(1)	200	4.7	Short	Open	Short
	3.3	4-60	100	10	100	43.2	47
	5	5-60	100	10	100	24.9	47
	12	12-60	22	22	100	9.09	NA
	24	24-60	22	47	100	4.32	NA

NOTE：

1) The maximum input voltage is limited by the minimum turn-on time T_{ON_MIN}.
2) The inductance value is calculated based on the typical V_{IN}=24V.
3) All C_{OUT} capacitors are values after derating. More capacitors need to be added when ceramic capacitors are used.
4) At high frequencies and limited by temperature protection, full load current may not be available at higher voltages.
5) For R_{FBT} not 1MΩ design, adjust C_{ff} so that C_{ff} X R_{FBT} unchanged, and adjust R_{FBT}/R_{FBB} unchanged.
6) In the case of large ESR output capacitance, there is sufficient phase margin and C_{ff} is not required.

Output voltage setting

The output voltage VOUT is determined by the divider resistance between VOUT and PGND of FB pin. The resistance value can be selected according to the following formula:

_____

is the internal reference voltage. The upper part resistance R_{FBT} generally chooses resistance not greater than 1MΩ , too large resistance value will weaken the anti-interference ability of the feedback circuit, too small resistance value will increase the static current, reduce the light load efficiency.

Set the switching frequency resistance

Switching frequency Fs is determined by external resistance R_T between FREQ pin and AGND. R_T resistance can be calculated according to the following formula. 1% precision resistance is recommended.

( ) 81053 21

Input capacitance selection

In typical applications, a 4.7uF to 10uF X7R or X5R ceramic capacitor with an adequate voltage rating is recommended. To compensate for the derating caused by dc bias of the ceramic capacitor, it is recommended that the rated voltage be twice the maximum input voltage. It is also recommended to use a small package capacitor as close to VIN and PGND pins as possible to absorb high frequency switching noise, such as 0603 package, 0.1uF ceramic capacitor.

Inductance selection

The selection of inductance needs to consider the following aspects:

(1) Select inductor to provide the desired current ripple. It is recommended that the current ripple be about 20%-40% of the current maximum output current, and the inductance calculation formula is as follows:

(1 / ,)

is the switching frequency, is the LED current, and constant K is the percentage of inductance current ripple.

For HT6050A, the optimal inductance range for most typical applications is 2.2μH to 15μH.

(2) To ensure circuit safety, the saturation current rating of the inductor must be greater than the peak current at full load. It is recommended that the saturation current of the inductor exceed the peak current at normal operation by 30%-40%. The peak current of inductance can be calculated according to the following formula:

(1 / ,)
2

Output capacitance selection

HT6050A allows a wide range of output capacitors. To ensure cost and small volume, select an appropriate output capacitor. In practical applications, output capacitance will directly affect voltage overshoot/undershoot and output voltage ripple in transient response to output current. When the load transient changes, the output capacitor needs to supply the charge before the loop adjustment is completed, and the transient voltage change value I can be calculated by the following formula:

I

I represents the jump value of load current, and ESR represents the equivalent series resistance value of output capacitance.

The output voltage ripple is mainly composed of two parts: one is caused by the inductance current ripple flowing through the ESR of the output capacitor, the other is caused by the inductance current ripple charging and discharging of the output capacitor.

8

represents inductance ripple current, represents MOSFET switching frequency

In order to maintain small output voltage overshoot or undershoot and reduce output ripple during transient changes, capacitors with large capacitance and small ESR are required, which also increases cost and volume. It is critical to select the appropriate output capacitance.

C_{VCC} capacitance

The VCC pin is the output of HT6050A's internal LDO, which is used to power HT6050A's internal control circuit and drive the two internally integrated MOSFETs. The input to this LDO comes from VIN or VCCIN (see internal function block diagram for details). To ensure voltage stability, it is recommended that a 1uF-4.7uF ceramic capacitor be placed as close to VCC and PGND pins as possible, and the rated voltage is recommended to be above 10V.

C_{VCCIN} capacitance

This pin is an input to the internal LDO. When the VCCIN pin is not connected, the input to the LDO is connected internally to VIN. Due to the nature of LDO, the pressure difference between input and output can affect LDO efficiency. For applications with output voltages above 5V, the VCCIN pin can be connected to the output voltage for higher light-load efficiency. For this method, it is recommended to place a 1uF ceramic capacitor close to the VCCIN and PGND as the input capacitor for the internal LDO.

C_{BST} capacitance

C_{BST} capacitor is a bootstrap capacitor in HT6050A application, used to drive high side power tube. In order to ensure voltage stability, it is recommended to place a 0.1uF-1uF ceramic capacitor close to the BST and SW pins with rated voltage above 16V.

C_{SS} Soft starting capacitance

With the SS pin dangling, HT6050A will adopt internal soft start time. To obtain a longer soft start time, C_{SS} capacitor can be connected to SS pin, and its capacitance value can be obtained from the following formula:

$$\frac{\quad}{\quad}$$

is the soft start charging current, is the internal reference voltage, and is the target soft start time, whose value should not be less than the internal soft start time.

Undervoltage lock (UVLO) setting

HT6050A can adjust input undervoltage lock (UVLO) using the external partial voltage resistor network consisting of R_{ENH} and R_{ENL}. R_{ENH} is connected between VIN pin and EN pin. R_{ENL} is connected between the EN pin and the GND pin. The UVLO value will be determined by the following formula:

$$\left(1 \quad \frac{\quad}{\quad}\right)$$

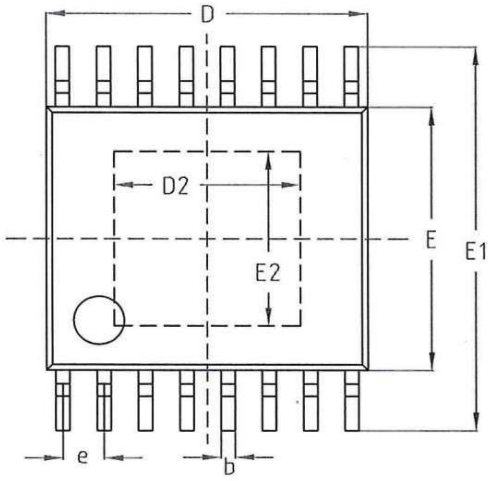
indicates the threshold for the EN function. Note that the set must be higher than the built-in under-voltage lock value 4V on the VIN pin.

R_{PG} setting

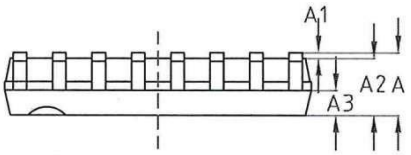
The PG pin needs to be pulled up to the VCC or an external voltage source through an external resistor. The recommended pull-up resistance value of the pin ranges from 10kΩ to 100kΩ. It should be noted that the pull-up power supply of PG pin should not exceed 6V. Therefore, if the pull-up power supply exceeds the limit, it is recommended to apply a resistance partial voltage between PG pin and PGND.

ETSSOP16L

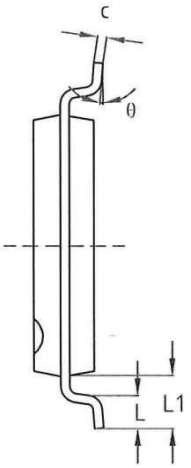
TOP VIEW
正视图



SIDE VIEW
侧视图



SIDE VIEW
侧视图



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
c	0.13	-	0.17
D	4.90	5.00	5.10
E	4.30	4.40	4.50
E1	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00REF		
L	0.45	0.60	0.75
θ	0°	-	8°

Size(mm) / LF size(mil)	D2	E2
118*91	2.80REF	2.10REF

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Switching Controllers ***category:***

Click to view products by HTCSEMI ***manufacturer:***

Other Similar products are found below :

NCP1218AD65R2G NCP1244BD065R2G NCP1336ADR2G NCP6153MNTWG NCP81101BMNTXG NCP81205MNTXG SJE6600 AZ7500BMTR-E1 SG3845DM NCP1250BP65G NCP4204MNTXG NCP6132AMNR2G NCP81102MNTXG NCP81206MNTXG NCP1240AD065R2G NCP1240FD065R2G NCP1361BABAYSNT1G NCP1230P100G NX2124CSTR SG2845M NCP1366BABAYDR2G NCP81101MNTXG NCP81174NMNTXG NCP4308DMTTWG NCP4308AMTTWG NCP1366AABAYDR2G NCP1251FSN65T1G NCP1246BLD065R2G MB39A136PFT-G-BND-ERE1 NCP1256BSN100T1G LV5768V-A-TLM-E NCP1365BABCYDR2G NCP1365AABCYDR2G NCP1246ALD065R2G AZ494AP-E1 CR1510-10 NCP4205MNTXG ISL69158IRAZ-T7A XRP6141ELTR-F RY8017 LP6260SQVF LP6298QVF ISL6121LIB ISL6225CA ISL6244HRZ ISL6268CAZ ISL6315IRZ ISL6420AIAZ-TK ISL6420AIRZ ISL6420IAZ