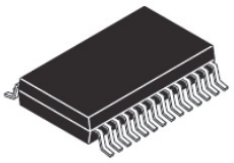
LVDS serializer/decoder transmitter

General Description

designed to transmit and receive serial data over FR-4PCB backplanes, balanced copper cables and unshielded twisted pair. The HT651023B transforms 10-bit wide word into a single high speed LVDS serialdata stream with embedded clock. On the other hand, The HT651224B receives the serial data stream and transforms it back into a 10-bit wide parallel word and recovers parallel clock. With HTCSEMI high performance architecture, the chipset can transmit and receive wide-range word rates from 10MHz to 90MHz. Including overhead, this translates into a serial data rate between 100-Mbps and 900-Mbps payloadencoded throughput.A synchronization mode is available to establish the link between chipset upon power up, while chipset internally generates SYNC patterns or the HT651224B can be allowed to synchronize to random data. By using the synchronization mode, the chipset links within specified short time.When no data link is required, the chipset can be set into power-down mode. Alternatively, a mode isavailable to place the output pins in the high-impedance state without losing PLL lock.

FEATURES

- 100MBPS TO 900 MBPS SERIALIZER/DESERIALIZER
- LOCK INDICATION AND SYNCHRONIZATION MODE FOR FASTER LOCK
- NO EXTERNAL COMPONENTS REQUIRED FOR PLL
- PROGRAMMABLE EDGE TRIGGER ON CLOCK
- CHIPSET POWER CONSUMPTION < 500 mW (TYP) AT 90MHz
- INDUSTRIAL TEMPERATURE RANGE
- HIGH ESD CAPABILITY (4000V HBM)
- 28-PIN SSOP PB-FREE PACKAGE



SSOP28 S SUFFIX
HT651023BRSZ
HT651224BRSZ

APPLICATIONS

- BACKPLANE INTERCONNECT
- WIRELESS BASE STATION
- FIBER OPTIC TRANSCERVER

FUNCTIONAL BLOCK DIAGRAM

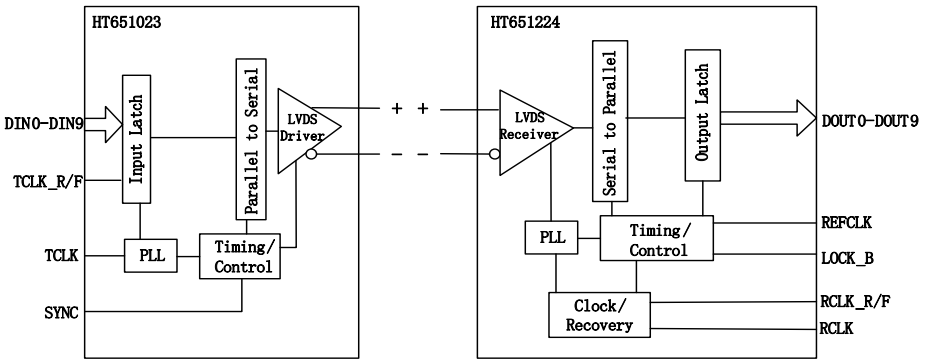


Figure 1. Functional Description

FUNCTIONAL DESCRIPTION

The HT651023B and HT651224B form a 10-bit serializer/deserializer chipset designed to transmit data over FR-4 PCB backplanes, balanced copper cables and unshielded twisted pair at clock rates from 10 MHz to 90 MHz. The chipset has five states of operation: initialization mode, synchronization mode, data transmission mode, power-down mode, and high-impedance mode. The following sections describe each state of operation.

INITIALIZATION MODE

Initialization of both devices must occur before data transmission. Initialization refers to synchronization of the serializer and deserializer PLLs to local clocks, which may be the same or separate.

For the serializer, the local clock is the transmit clock (TCLK) provided by an external device. For the deserializer, a local clock must be applied to the REFCLK pin.

SYNCHRONIZATION MODE

To receive valid data, the deserializer PLL must synchronize to the serializer. Synchronization can be accomplished by one of two ways:

- **Rapid Synchronization:** The serializer sends the preset SYNC patterns, which consists of six ones and six zeros switching at the input clock rate. The transmission of such SYNC patterns enables the deserializer to lock to the serializer signal within a deterministic time frame. This transmission of SYNC patterns can be triggered by applying the input on the serializer's SYNC input. Upon receiving valid pulse (wider than 6 clock cycles) from SYNC pin, the serializer sends 1026 cycles of SYNC pattern.

  When the deserializer detects edge transitions at the LVDS input, it always attempts to lock to the embedded clock information. LOCK_B output of the deserializer will go from high to low until the deserializer locks to the LVDS data. When LOCK_B is low, the deserializer outputs represent incoming LVDS data.
- **Random-Lock Synchronization:** The deserializer can lock to a data stream without the serializer sending SYNC patterns. This allows the HT651224B to operate in open-loop applications. At some applications, the deserializer's such ability is more important, like: hot insertion into a running backplane. The data stream is essentially random in the open-loop or hot-insertion case. Therefore, the exact lock time cannot be predicted because lock time varies due to data stream characteristics. The initial phase relation between the incoming data and the REFCLK is the key factor on this lock time when the deserializer powers up.

Some special data pattern in the data stream can also affect lock time. If a specific pattern is repetitive, the deserializer could enter false lock—falsely recognizing the data pattern as the start/stop bits. This is referred to as Repetitive Multitransition (RMT); see Figure 2 for RMT examples. Circuit within the deserializer can detect this false lock. Upon detection, the LOCK_B output will not becoming active until the specific pattern changes. Notice that the deserializer will not be affected by RMT pattern if the deserializer is in lock . The deserializer will go into lock only when it finds a unique four consecutive cycles of data boundary (stop/start bits) at the same position. The deserializer stays in lock until it cannot detect the same data boundary (stop/start bits) for four consecutive cycles. Then the deserializer goes out of lock and re-establishes lock. In the event of loss of synchronization, the LOCK_B pin output goes high and the outputs (including RCLK) enter a high-impedance state.

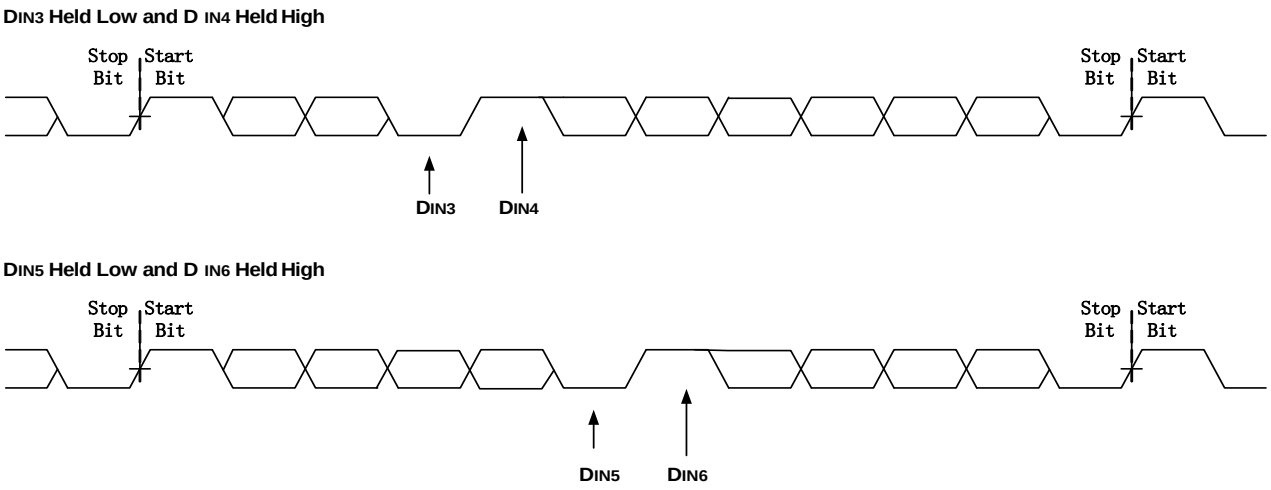


Figure 2. RMT Pattern Examples

DATA TRANSMISSION MODE

After initialization and synchronization, the serializer accepts parallel data from inputs DIN0-DIN9. The TCLK is used to latch the incoming data and the TCLK_R/F pin selects the edge of TCLK to strobe incoming data. TCLK_R/F high selects the rising edge and low selects the falling edge. The data at DIN0-DIN9 is ignored and 1026 cycles of SYNC pattern are sent when the SYNC input is high for six TCLK cycles.

The serializer transmits serialized data and appended clock bits (10+2 bits) from the serial data output (DOP, DON) at 12 times the TCLK frequency. If TCLK is 90 MHZ, the serial rate is 90 x 12 =1080 Mbps and the useful data rate is 90 X 10 =900Mbps because there is only 10 bits input data. The data rate of TCLK must be in the range of 10 MHz to 90 MHz for device limitation.

When DEN is high and SYNC is low, the serializer outputs transmit data. When DEN is low, the serializer outputs enter the high-impedance state.

Once the deserializer has synchronized to the serializer, the LOCK_B pin transitions low and the DOUT data is valid. The DOUT0-DOUT9 data is strobed out by RCLK. The RCLK edge is selected by RCLK_R/F input. The DOUT0-DOUT9, LOCK_B and RCLK outputs can drive three CMOS input gates (total 15-pF load) with an 90-MHZ clock.

POWER DOWN MODE

The serializer and deserializer use the power-down state to reduce power consumption. The deserializer enters power down when PDB is low. When PDB is low, the serializer enters power down state. At this mode, the PLL stops and the outputs enter a high-impedance state, which limits supply current within the milliampere range. To exit power down state, you must drive the PDB pin high.

FAILSAFE BIASING FOR THE HT651224B

The HT651224B has an input threshold sensitivity of ±50 mV. This allows for greater differential noise margin for the HT651224B. This increased sensitivity of HT651224B can cause unintentional locking by picking up noise as signal when HT651224B's input is not being driven. For example, this may occur when the input cable is disconnected. The HT651224B has an on-chip fail-safe circuit that drives the differential inputs and LOCK signal high.

POWER DECOUPLE FOR APPLICATION

The application of HT651023B/HT651224B is more sensitive to fluctuations in the power supply. Therefore, proper decoupling plays a very important role in application. There is always a better result, if a 1μF capacitor is applied at power supply.

PIN CONFIGURATION

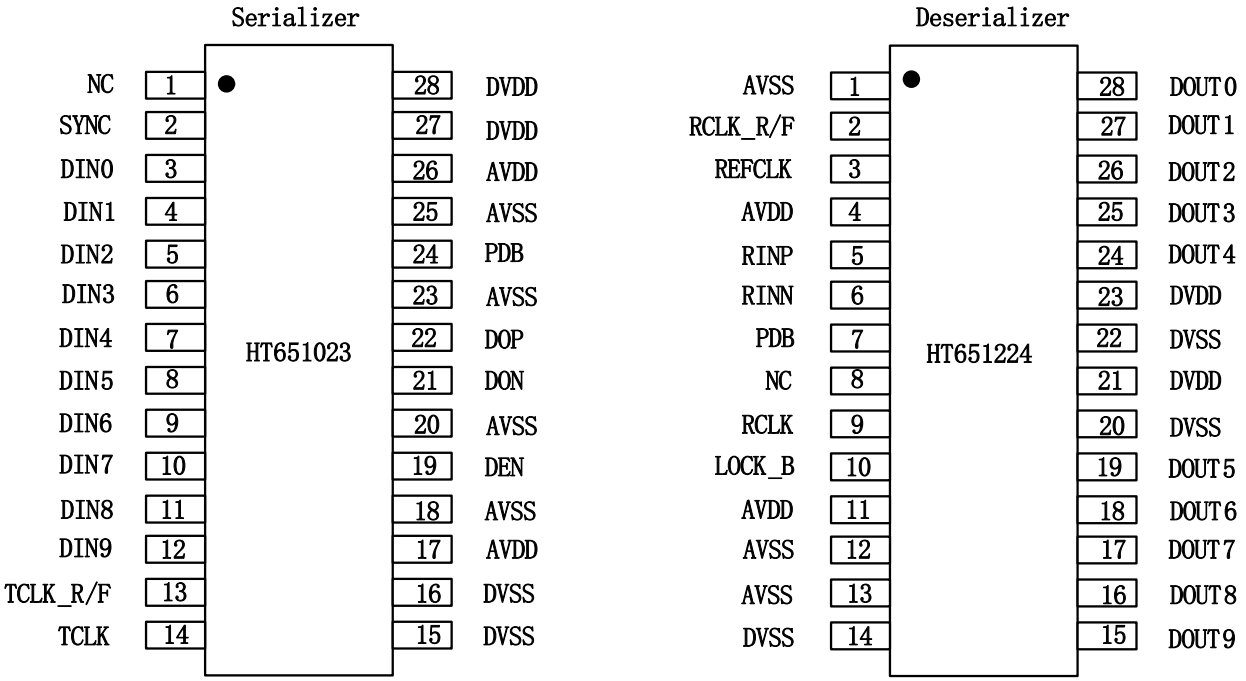


Figure 3. Pin Configuration

Table2. Pin Function Descriptions

Pin No.	Name	Function Descriptions
SERIALIZER(HT651023B)		
1	**NC**	No Connection
2	**SYNC**	high for 6 cycles of TCLK: Serializer initiates transmission of 1026 SYNC patterns until SYNC be
3-12	**DIN0-DIN9**	Parallel data inputs
13	**TCLK_R/F**	High selects a TCLK rising-edge strobe, low selects a TCLK falling-edge data strobe
14	**TCLK**	Reference clock input. TCLK provides the reference clock to the internal PLL and strobes parallel data into
15,16	**DVSS**	Digital circuit ground
17,26	**AVDD**	Analog circuit power supply
18,20,23,25	**AVSS**	Analog circuit ground
19	**DEN**	High enables serial data output. Low puts the LVDS serial output into the high-impedance state
21	**DON**	Inverting LVDS differential output
22	**DOP**	Non-inverting LVDS differential output
24	**PDB**	Low puts the device into a low-power mode and turns off the internal PLL and places the outputs into
27,28	**DVDD**	Digital circuit power supply
DESERIALIZER(HT651224B)		
1,12,13	**AVSS**	Analog circuit ground
2	**RCLK_R/F**	High selects an RCLK rising-edge data strobe, low selects an RCLK falling-edge data strobe
3	**REFCLK**	Reference clock input. TCLK provides the reference clock to the internal PLL
4,11	**AVDD**	Analog circuit power supply
5	**RINP**	Non-inverting LVDS differential input
6	**RINN**	Inverting LVDS differential input
7	**PDB**	Low puts the device into a low-power mode and turns off the internal PLL and places the DOUT0-DOUT9,
8	**NC**	No Connection
9	**RCLK**	Recovered clock. Use RCLK to strobe DOUT0-DOUT9
10	**LOCK_B**	Goes to low when the internal PLL locks onto the embedded clock edge
14,20,22	**DVSS**	Digital circuit ground
28-24,19-15	**DOUT0-DOUT**	Parallel data outputs
21,23	**DVDD**	Digital circuit power supply

Absolution Maximum Ratings

Characteristics	Value	Unit
VDD to VSS	-0.3 to 4	V
LVTTL input voltage	−0.3 to (VCC + 0.3)	V
LVTTL output voltage	−0.3 to (VCC + 0.3)	V
LVDS receiver input voltage	−0.3 to 3.9	V
LVDS driver output voltage	−0.3 to 3.9	V
Electrostatic discharge (HBM)	4000	V
Storage Temperature Range	-60 to 150	°C
Operation Temperature Range	-40 to 85	°C
Junction Temperature	150	°C

Recommended Operating Conditions

Characteristics	Min	Typ	Max	Unit
Voltage Supply Range	3.0	3.3	3.6	V
Receiver input voltage range	0		2.4	V
VCM Receiver input common mode range	$V_{ID}/2$		2.4-($V_{ID}/2$)	V
Supply noise voltage			100	mV_{P-P}
Operating Temperature Range	-40	25	85	°C

ELECTRONIC CHARACTERISTICS

(VDD = 3.0V to 3.6 V, VSS=0V, Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER		MIN	TYP	MAX	UNITS	Condition
SERIALIZER LVCMOS/LVTTL DC SPECIFICATIONS						
V_{IL}	Low-level input voltage	VSS		0.8	V	
V_{IH}	High-level input voltage	2		VDD	V	
DESERIALIZER LVCMOS/LVTTL DC SPECIFICATIONS						
VIL	Low-level input voltage	VSS		0.8	V	
VIH	High-level input voltage	2		VDD	V	
VOH	High-level output voltage		3	VCC	V	IOH = −5 mA
VOL	Low-level output voltage	VSS	0.2	0.4	V	IOL = 5 mA
IOS	Output short-circuit current	-15	-47	-80	mA	VOUT = 0 V
IOZ	High-impedance output current	-10	±1	10	uA	
SERIALIZER LVDS DC SPECIFICATIONS (Apply to Pins DOP and DON)						
VOD	Output differential voltage DOP-DON	350	450		mV	
DVOD	Output differential voltage unbalance			35	mV	
VOS	Offset voltage	1.1	1.2	1.3	V	
DVOS	Offset voltage unbalance		5	35	mV	
IOS	Output short circuit current		-10	-90	mA	
CO	Output single-ended capacitance			1±20%	pF	
DESERIALIZER LVDS DC SPECIFICATIONS (Apply to Pins RINP and RINN)						
VTH	Differential threshold high voltage			50	mV	
VTL	Differential threshold low voltage	-50			mV	
CI	Input single-ended capacitance			0.5±20%	pF	
SERIALIZER SUPPLY CURRENT (Applies to Pins DVDD and AVDD)						
I_{CCD}	Serializer supply current, worst case		20	25	mA	f = 10 MHz, RL = 27 Ω
			50	55	mA	f = 90 MHz, RL = 27 Ω
I_{CCXD}	Serializer supply current, power down			1	mA	
DESERIALIZER SUPPLY CURRENT (applies to pins DVDD and AVDD)						
I_{CCR}	Deserializer supply current, worst case		15	35	mA	f = 10 MHz, CL = 15 pF
			80	95	mA	f = 90 MHz, CL = 15 pF
I_{CCXR}	Deserializer supply current, power down			1	mA	

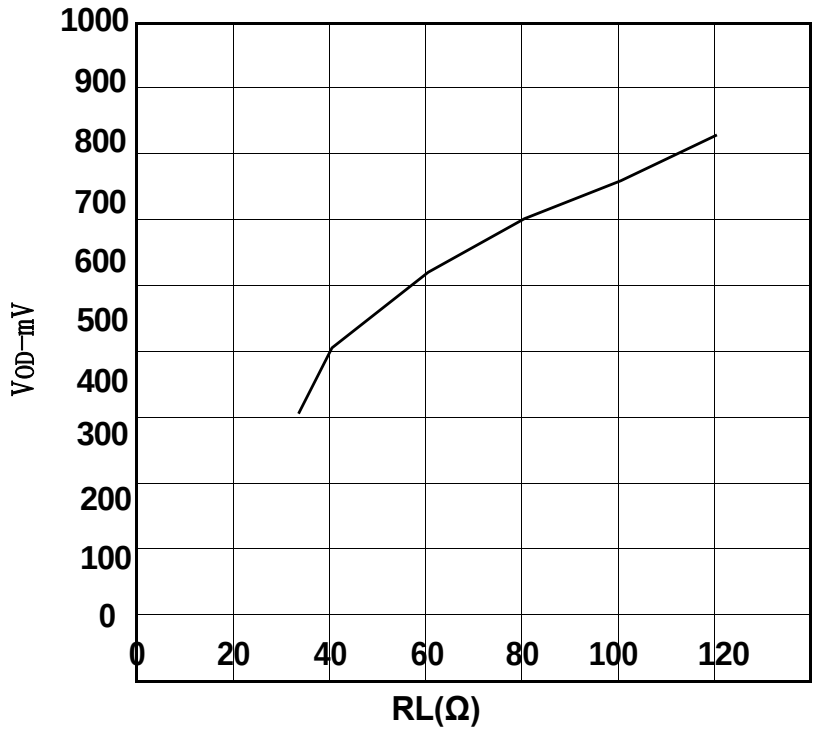


Figure 4. Typical V_{OD} Curve

SERIALIZER TIMING REQUIREMENTS FOR TCLK

(VDD = 3.0V to 3.6 V, VSS=0V, Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER		MIN	TYP	MAX	UNITS	condition
t_{TCP}	Transmit clock period	11.1	T	100	ns	
t_{TCIH}	Transmit clock high time	0.4T	0.5T	0.6T	ns	
t_{TCIL}	Transmit clock low time	0.4T	0.5T	0.6T	ns	
$t_{t(CLK)}$	TCLK input transition time		3	6	ns	
t_{JIT}	TCLK input jitter			150	ps(RMS)	
	Frequency tolerance	-100		+100	ppm	

SERIALIZER SWITCHING CHARACTERISTICS

(VDD = 3.0V to 3.6 V, VSS=0V, Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER		MIN	TYP	MAX	UNITS	condition
$t_{TLH(L)}$	LVDS low-to-high transition time		0.2	0.4	ns	RL = 27 Ω, CL = 10 pF to VSS
$t_{LTHL(L)}$	LVDS high-to-low transition time		0.25	0.4	ns	
$t_{SU(DI)}$	DIN0−DIN9 setup to TCLK	0.5			ns	
$t_{H(DI)}$	DIN0−DIN9 hold from TCLK	4			ns	
t_W	SYNC pulse duration	$6xt_{TCP}$			ns	
t_{PLD}	Serializer PLL lock time	$1026xt_{TCP}$			ns	
t_{DJIT}	Deterministic jitter			200	ps	
t_{RJIT}	Random jitter		10	20	ps	

DESERIALIZER TIMING REQUIREMENTS FOR REFCLK

(VDD = 3.0V to 3.6 V, VSS=0V, Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER		MIN	TYP	MAX	UNITS	condition
t_{RFCP}	REFCLK period	11.1	T	100	ns	
t_{RFDC}	REFCLK duty cycle	30%	50%	70%	ns	
$t_{t(RF)}$	REFCLK input transition time		3	6	ns	
	Frequency tolerance	-100		+100	ppm	

DESERIALIZER SWITCHING CHARACTERISTICS

(VDD = 3.0V to 3.6 V, VSS=0V, Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER		PIN	MIN	TYP	MAX	UNITS	condition
t_{RCP}	Receiver out clock period	RCLK	11.1	T	100	ns	$t_{RCP=}$ t_{TCP}
$t_{TLH(C)}$	Low-to-high transition time	ROUT0-ROUT9		1.2	2.5	ns	
$t_{THL(C)}$	High-to-low transition time			1.2	2.5	ns	
t_{ROS}	DOUTx data valid before		0.4x t_{RCP}	0.5x t_{RCP}		ns	
t_{ROH}	DOUTx data valid after RCLK		-0.4x t_{RCP}	-0.5x t_{RCP}		ns	
t_{RDC}	RCLK duty cycle		40%	50%	60%		

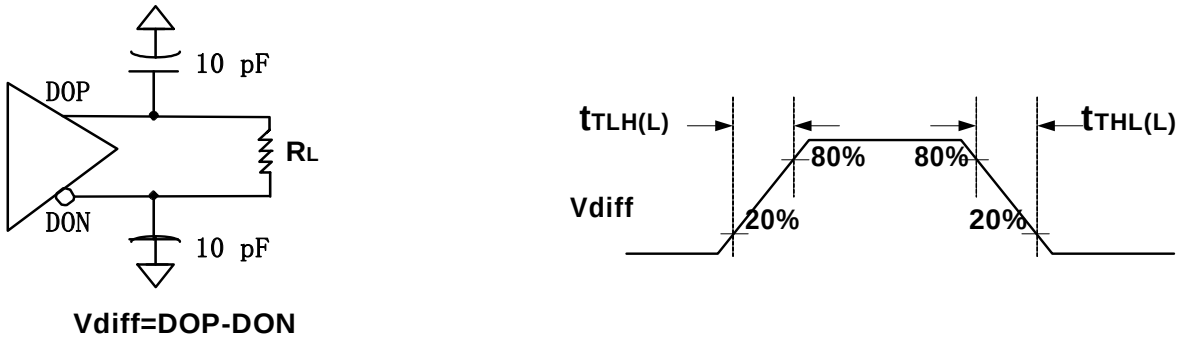


Figure 5. Serializer LVDS Output Load and Transition Times

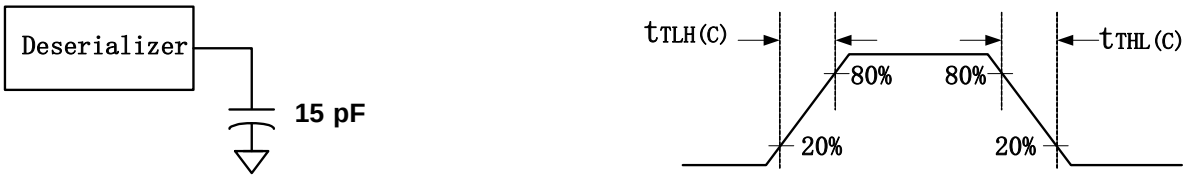


Figure 6. Deserializer CMOS Output Load and Transition Times

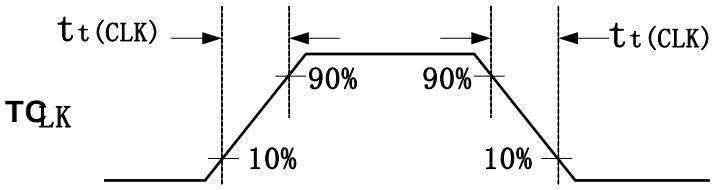


Figure 7. Serializer Input Clock Transition Time

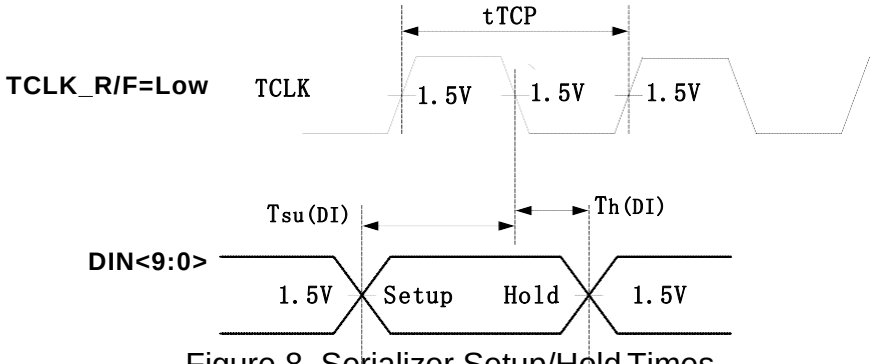


Figure 8. Serializer Setup/Hold Times

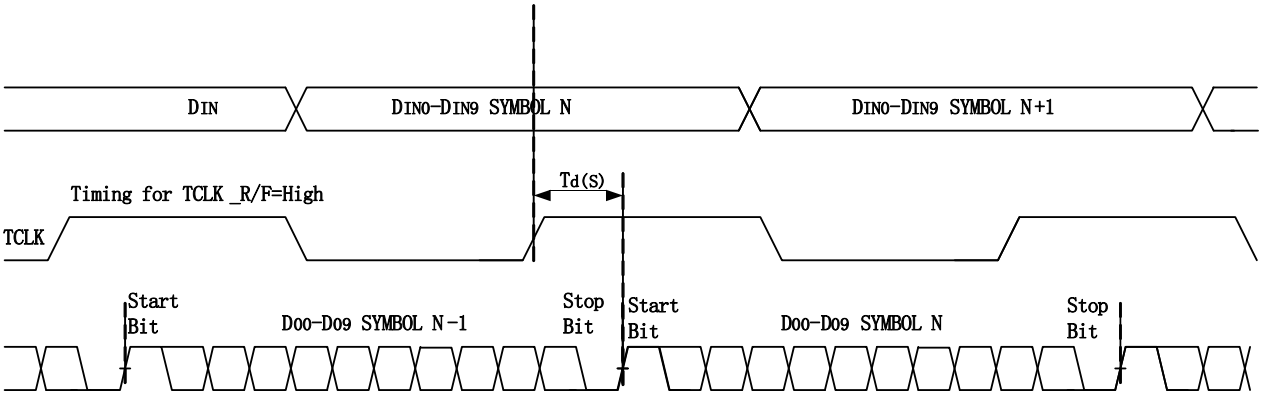


Figure 9. Serializer Delay

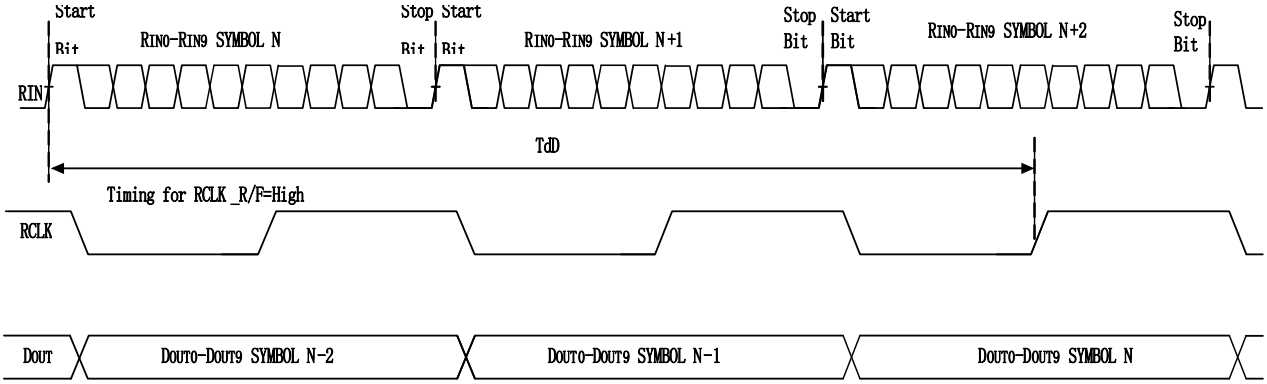


Figure 10. Deserializer Delay

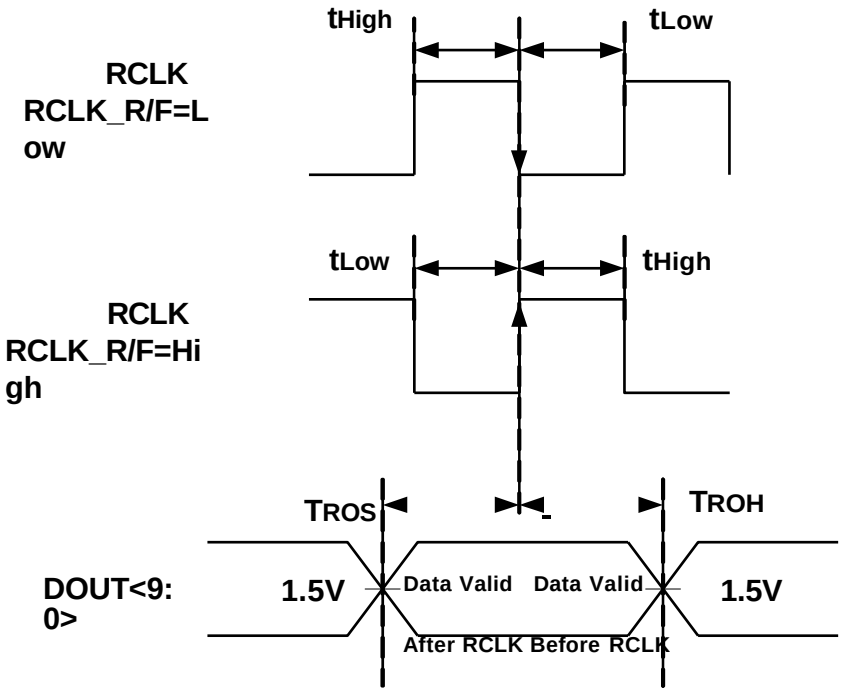


Figure 11. Deserializer Data Valid Out Times

APPLICATION SCHEME

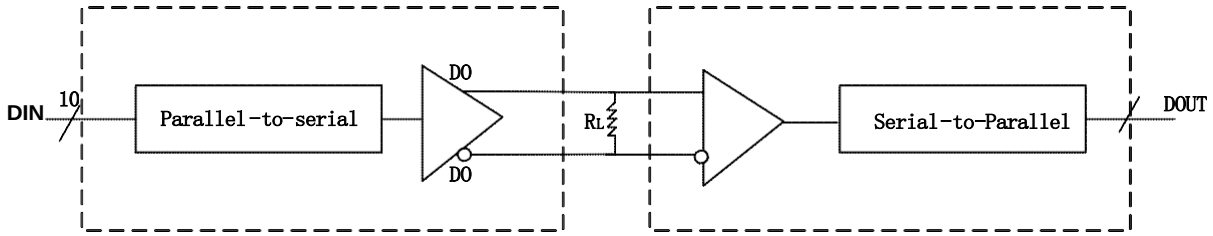


Figure 12. Single-Terminated Point-to-Point Connection

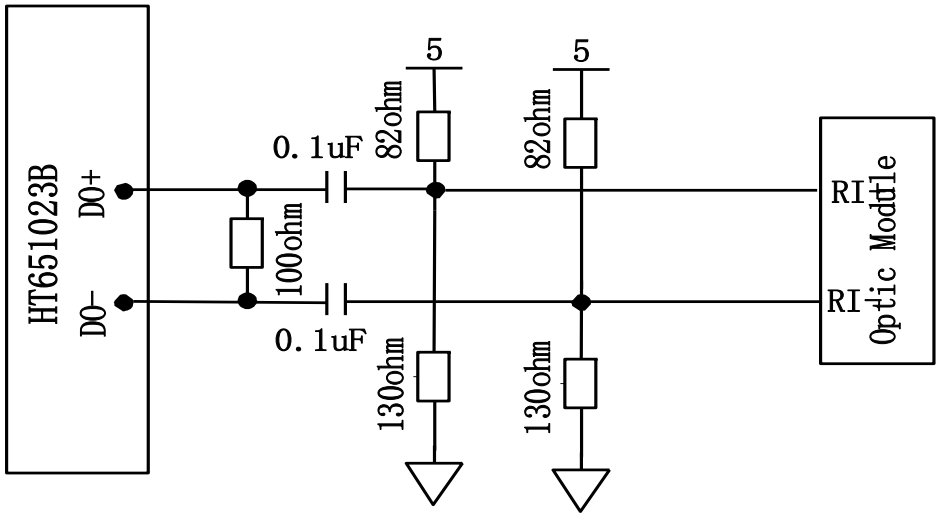


Figure 13. Typical Optic Transmission Application Scheme (Transmission Side)

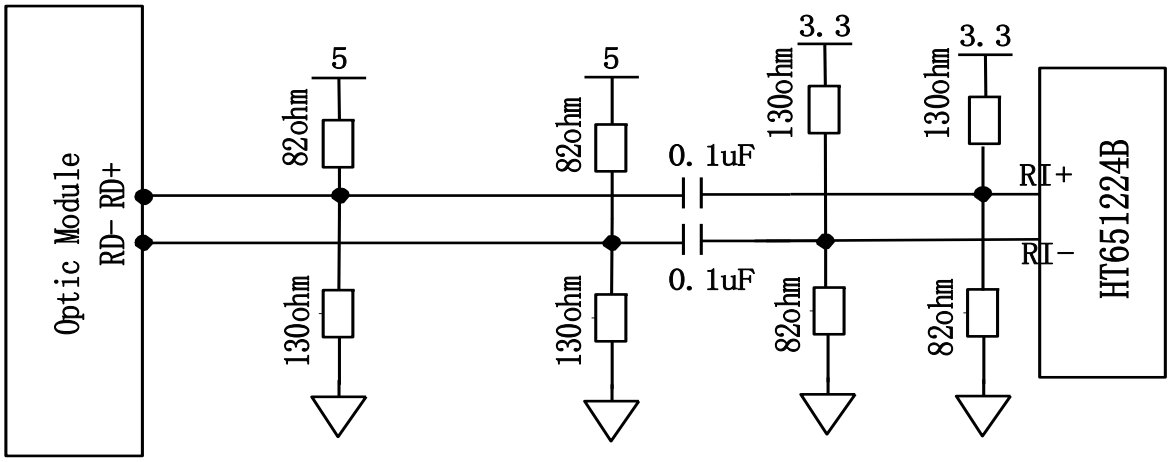
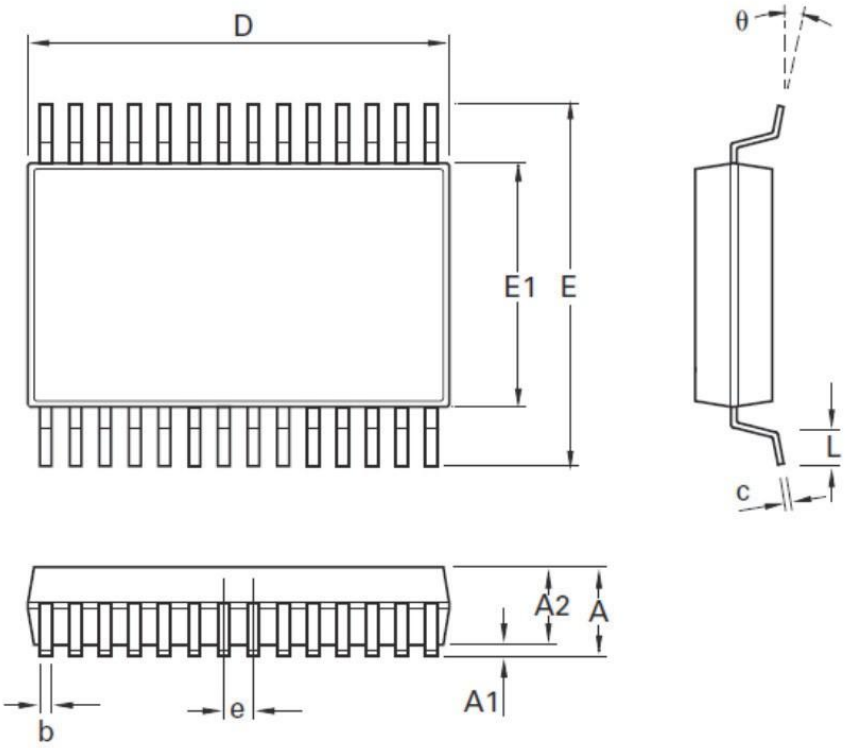


Figure 14. Typical Optic Transmission Application Scheme (Reception Side)

Package Information

SOP-8

DIMENSIONS			
REF.	mm		
	MIN.	TYP.	MAX.
A	1.70	-	2.00
A1	0.05	-	0.15
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	9.90	10.20	10.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e	0.65BSC		
θ	0°	-	8°
L	0.55	-	0.95



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