Low-Power, Rail-to-Rail Output, 12-Bit Serial InputDIGITAL-TO-ANALOG CONVERTER

(compatible to DAC7512)

FEATURES

Single 12-bit DAC
6-lead SOT-23 and 8-lead MSOP packages
Micropower operation: 140 µA @ 5 V
Power-down to 200 nA @ 5 V, 50 nA @ 3 V
2.7 V to 5.5 V power supply
Guaranteed monotonic by design
Reference derived from power supply
Power-on reset to zero volts
Three power-down functions
Low power serial interface with Schmitt-triggered inputs
On-chip output buffer amplifier, rail-to-rail operation
$\overline{\text{SYNC}}$ interrupt facility

APPLICATIONS

Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators

GENERAL DESCRIPTION

The HT7512A[1] is a single, 12-bit buffered voltage out digital-to- analog converter (DAC) that operates from a single 2.7 V to
5.5 V supply consuming 115 µA at 3 V. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The HT7512A utilizes a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™ and digital signal processing (DSP) interface standards.

The reference for HT7512A is derived from the power supply inputs and thus gives the widest dynamic output range. The part incorporates a power-on reset circuit that ensures that the DAC output powers up to zero volts and remains there until a valid write takes place to the device. The part contains a power-down feature that reduces the current consumption of the device to 200 nA at 5 V and provides software selectable output loads while in power-down mode. The part is put into power-down mode over the serial interface.

The low power consumption of this part in normal operation makes it ideally suited to portable, battery-operated equipment. The power consumption is 0.7 mW at 5 V reducing to 1 µW in power-down mode.

FUNCTIONAL BLOCK DIAGRAM

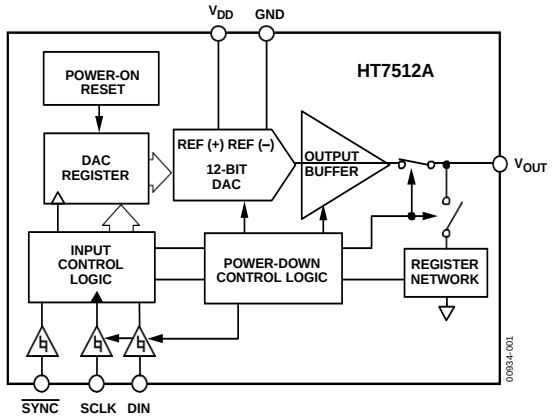


Figure 1.

PRODUCT HIGHLIGHTS

1. Available in 6-lead SOT-23 and 8-lead MSOP packages.
2. Low power, single-supply operation. This part operates from a single 2.7 V to 5.5 V supply and typically consumes 0.35 mW at 3 V and 0.7 mW at 5 V, making it ideal for battery-powered applications.
3. The on-chip output buffer amplifier allows the output of the DAC to swing rail-to-rail with a slew rate of 1 V/µs.
4. Reference derived from the power supply.
5. High speed serial interface with clock speeds up to 30 MHz. Designed for very low power consumption. The interface only powers up during a write cycle.
6. Power-down capability. When powered down, the DAC typically consumes 50 nA at 3 V and 200 nA at 5 V.

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[2]					
Resolution	12			Bits	
Relative Accuracy			±16	LSB	See Figure 5
Differential Nonlinearity			±1	LSB	Guaranteed monotonic by design (see Figure 6)
Zero-Code Error		5	40	mV	All zeroes loaded to DAC register (see Figure 9)
Full-Scale Error		−0.15	−1.25	% of FSR	All ones loaded to DAC register (see Figure 9)
Gain Error			±1.25	% of FSR	
Zero-Code Error Drift		−20		µV/°C	
Gain Temperature Coefficient		−5		ppm of FSR/°C	
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Output Voltage Settling Time		8	10	µs	1/4 scale to 3/4 scale change (400 hex to C00 hex) R_L = 2 kΩ, 0 pF < C_L < 200 pF (see Figure 19)
		12		µs	R_L = 2 kΩ, C_L = 500 pF
Slew Rate		1		V/µs	
Capacitive Load Stability		470		pF	R_L = ∞
		1000		pF	R_L = 2 kΩ
Digital-to-Analog Glitch Impulse		20		nV-s	1 LSB change around major carry (see Figure 22)
Digital Feedthrough		0.5		nV-s	
DC Output Impedance		1		Ω	
Short Circuit Current		50		mA	V_{DD} = 5 V
		20		mA	V_{DD} = 3 V
Power-Up Time		2.5		µs	Coming out of power-down mode, V_{DD} = 5 V
		5		µs	Coming out of power-down mode, V_{DD} = 3 V
LOGIC INPUTS[3]					
Input Current			±1	µA	
V_{INL}, Input Low Voltage			0.8	V	V_{DD} = 5 V
V_{INL}, Input Low Voltage			0.6	V	V_{DD} = 3 V
V_{INH}, Input High Voltage	2.4			V	V_{DD} = 5 V
V_{INH}, Input High Voltage	2.1			V	V_{DD} = 3 V
Pin Capacitance			3	pF	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD} (Normal Mode)					DAC active and excluding load current
V_{DD} = 4.5 V to 5.5 V		140	250	µA	V_{IH} = V_{DD} and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		115	200	µA	V_{IH} = V_{DD} and V_{IL} = GND
I_{DD} (All Power-Down Modes)					
V_{DD} = 4.5 V to 5.5 V		0.2	1	µA	V_{IH} = V_{DD} and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		0.05	1	µA	V_{IH} = V_{DD} and V_{IL} = GND
POWER EFFICIENCY					
I_{OUT}/I_{DD}		93		%	I_{LOAD} = 2 mA, V_{DD} = 5 V

[1] Temperature range is as follows: B Version: −40°C to +105°C.
[2] Linearity calculated using a reduced code range of 48 to 4047; output unloaded.
[3] Guaranteed by design and characterization, not production tested.

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	Limit at T_{MIN}, T_{MAX}			
Parameter[1, 2]	V_{DD} = 2.7 V to 3.6 V	V_{DD} = 3.6 V to 5.5 V	Unit	Description
t_1[3]	50	33	ns min	SCLK cycle time
t_2	13	13	ns min	SCLK high time
t_3	22.5	13	ns min	SCLK low time
t_4	0	0	ns min	SYNC to SCLK rising edge setup time
t_5	5	5	ns min	Data setup time
t_6	4.5	4.5	ns min	Data hold time
t_7	0	0	ns min	SCLK falling edge to SYNC rising edge
t_8	50	33	ns min	Minimum SYNC high time

[1] All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[2] See Figure 2.
[3] Maximum SCLK frequency is 30 MHz at V_{DD} = 3.6 V to 5.5 V and 20 MHz at V_{DD} = 2.7 V to 3.6 V.

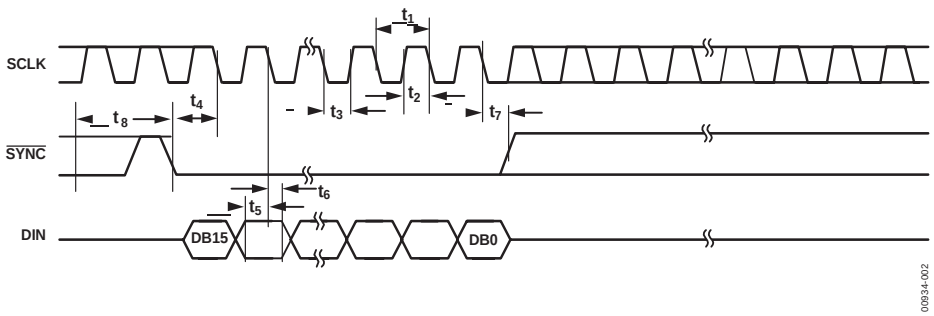


Figure 2. Serial Write Operation

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

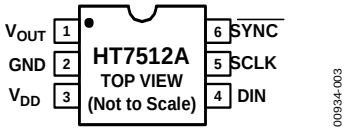


Figure 3. SOT-23 Pin Configuration

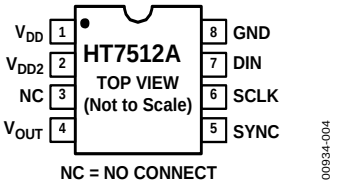


Figure 4. MSOP Pin Configuration

Note:MSOP8 VDD and VDD2 必须短接在一起。

Table 4. Pin Function Descriptions

SOT-23 Pin No.	MSOP Pin No.	Mnemonic	Description
1	4	V_{OUT}	Analog Output Voltage from DAC. The output amplifier has rail-to-rail operation.
2	8	GND	Ground Reference Point for All Circuitry on the Part.
3	1	V_{DD}	Power Supply Input. These parts can be operated from 2.5 V to 5.5 V and V_{DD} should be decoupled to GND.
4	7	DIN	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
5	6	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz.
6	5	$\overline{SYNC}$	Level Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When SYNC goes low, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 16th clock cycle unless $\overline{SYNC}$ is taken high before this edge, in which case the rising edge of SYNC acts as an interrupt and the write sequence is ignored by the DAC.
	2, 3	NC	No Internal Connection， VDD and VDD2 must be shorted together

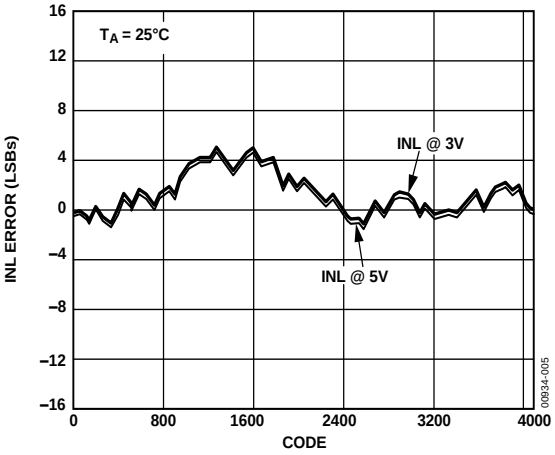


Figure 5. Typical INL Plot

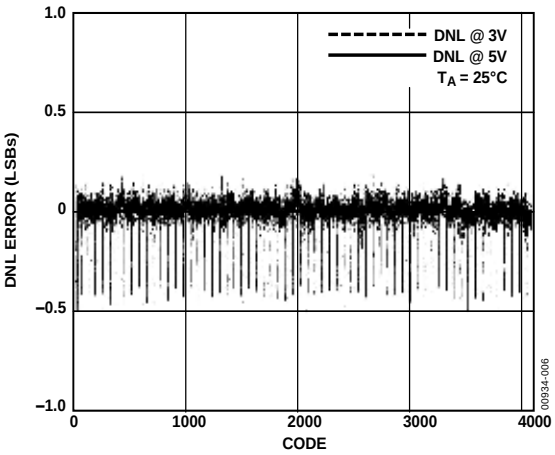


Figure 6. Typical DNL Plot

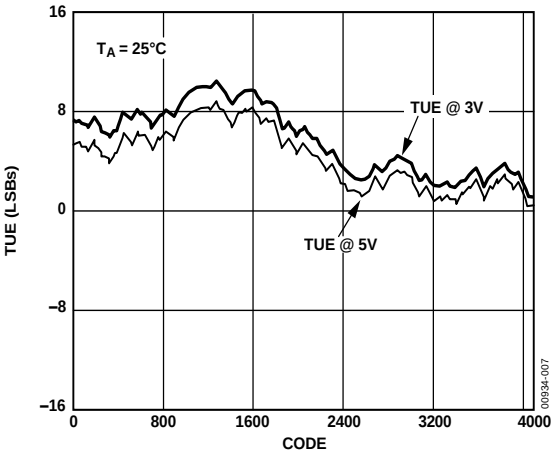


Figure 7. Typical Total Unadjusted Error Plot

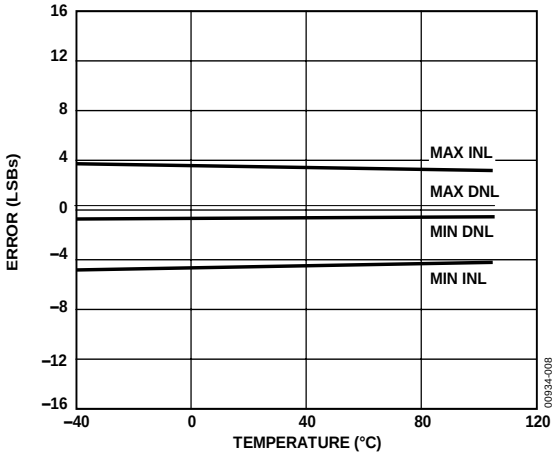


Figure 8. INL Error and DNL Error vs. Temperature

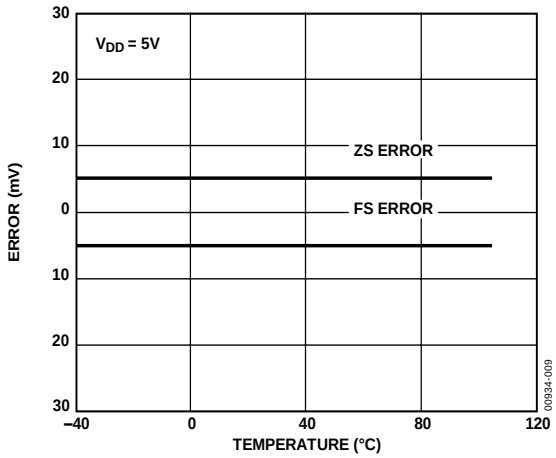


Figure 9. Zero-Scale Error and Full-Scale Error vs. Temperature

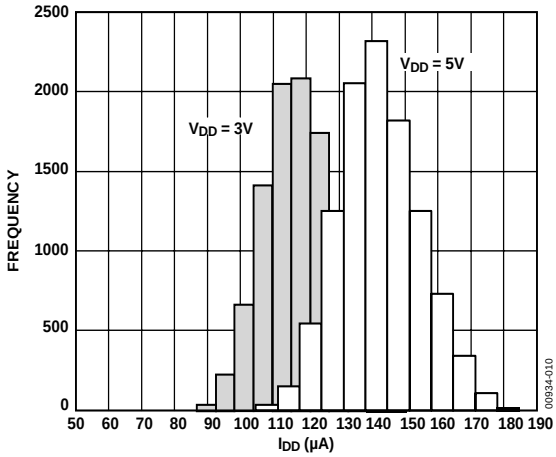


Figure 10. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

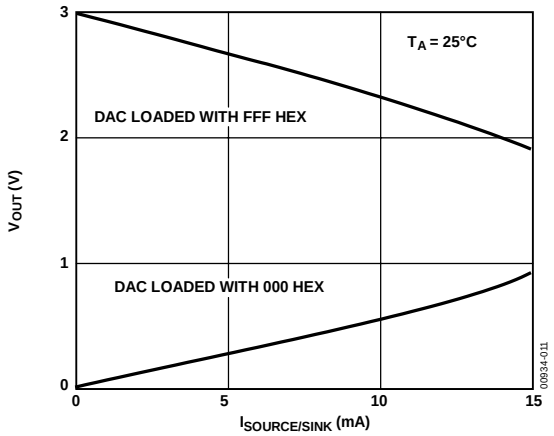


Figure 11. Source and Sink Current Capability with V_{DD} = 3 V

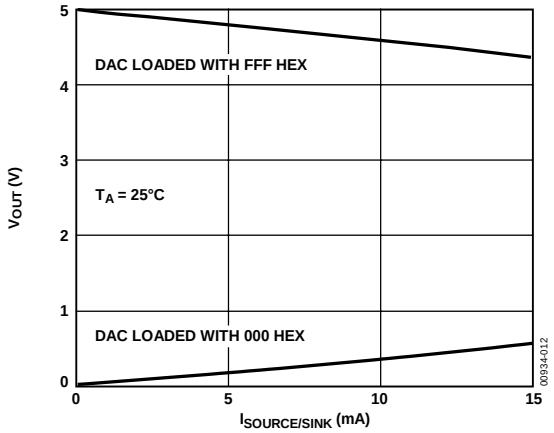


Figure 12. Source and Sink Current Capability with V_{DD} = 5 V

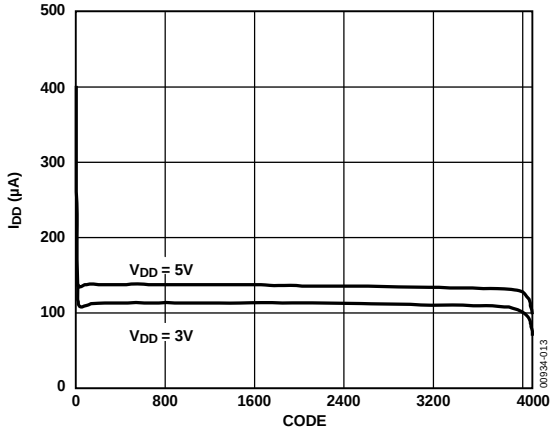


Figure 13. Supply Current vs. Code

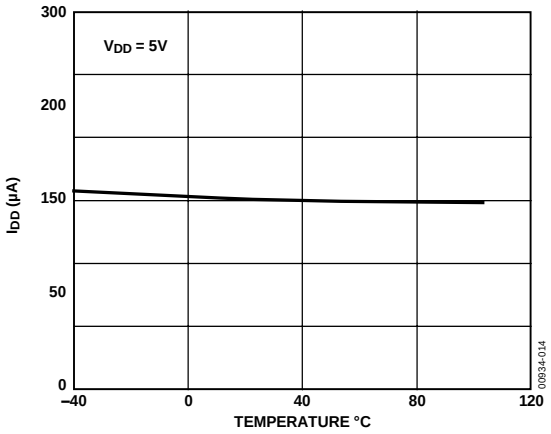


Figure 14. Supply Current vs. Temperature

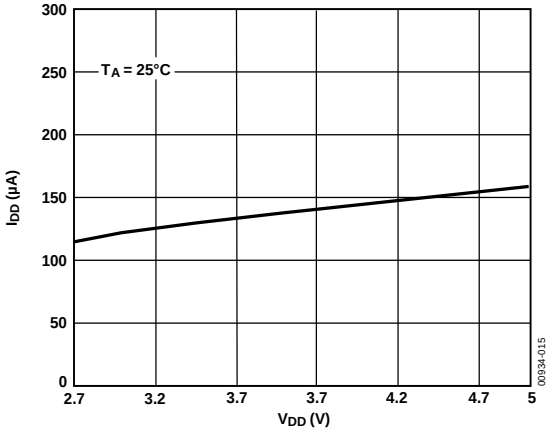


Figure 15. Supply Current vs. Supply Voltage

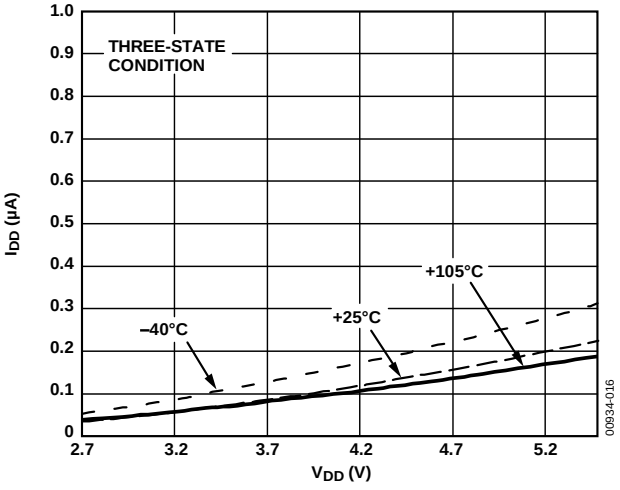


Figure 16. Power-Down Current vs. Supply Voltage

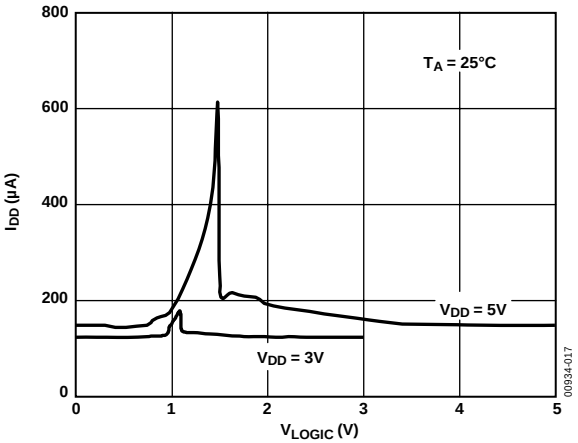
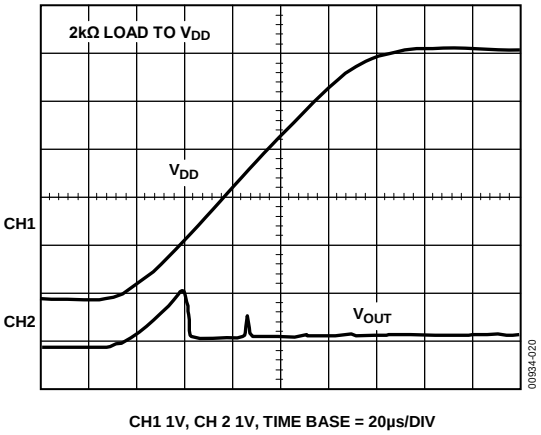
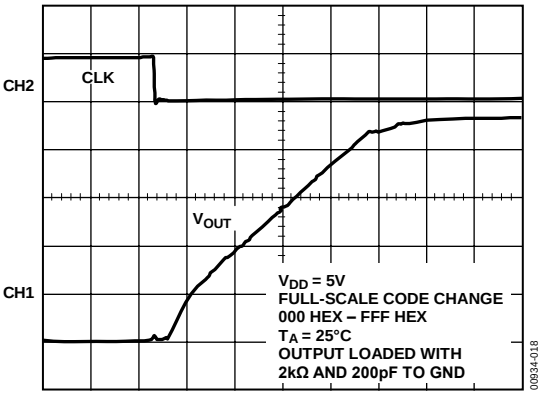


Figure 17. Supply Current vs. Logic Input Voltage



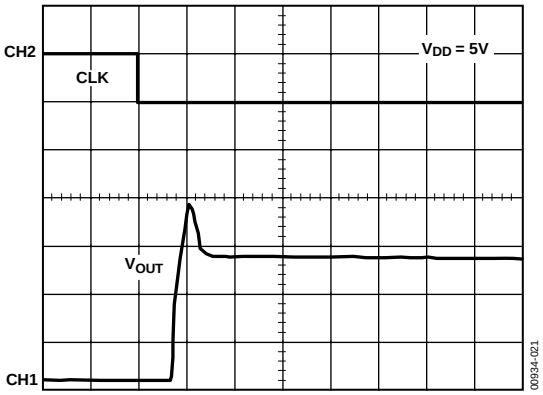
CH1 1V, CH 2 1V, TIME BASE = 20µs/DIV

Figure 20. Power-On Reset to 0 V



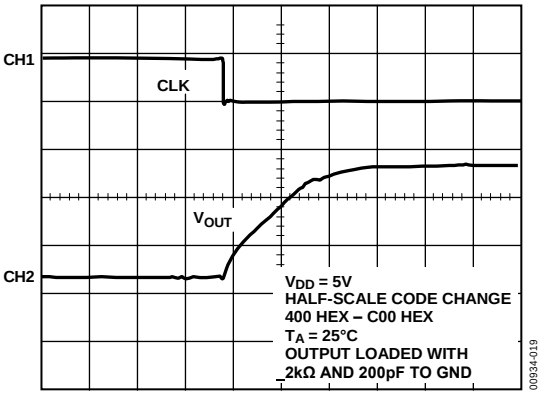
CH1 1V, CH2 5V, TIME BASE = 1µs/DIV

Figure 18. Full-Scale Settling Time



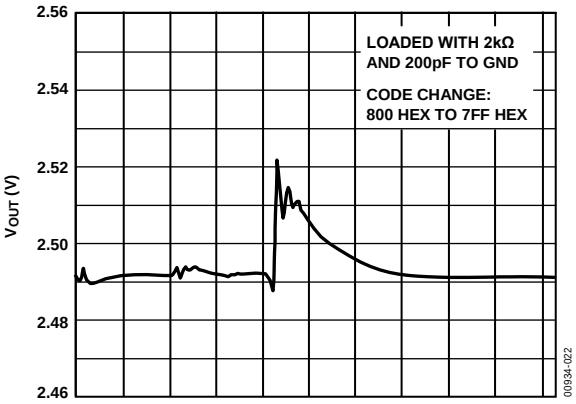
CH1 1V, CH2 5V, TIME BASE = 5µs/DIV

Figure 21. Exiting Power-Down (800 Hex Loaded)



CH1 1V, CH2 5V, TIME BASE = 1µs/DIV

Figure 19. Half-Scale Settling Time



500ns/DIV

Figure 22. Digital-to-Analog Glitch Impulse

THEORY OF OPERATION

D/A SECTION

The HT7512A DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Because there is no reference input pin, the power supply (V_{DD}) acts as the reference. Figure 23 shows a block diagram of the DAC architecture.

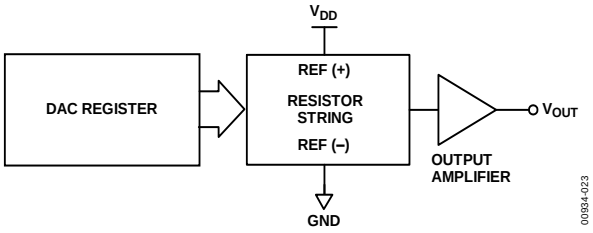


Figure 23. DAC Architecture

Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = V_{DD} \times \left(\frac{D}{4096} \right)$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 4095.

RESISTOR STRING

The resistor string section is shown in Figure 24. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

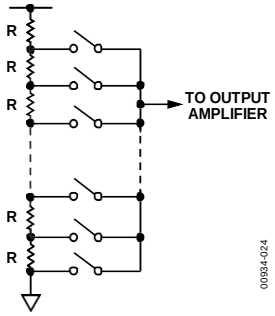


Figure 24. Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output that gives an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 11 and Figure 12. The slew rate is 1 V/µs with a half-scale settling time of 8 µs with the output unloaded.

SERIAL INTERFACE

The HT7512A has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN) that is compatible with SPI®, QSPI™, and MICROWIRE™ interface standards as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line is clocked into the 16-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the HT7512A compatible with high speed DSPs. On the 16th falling clock edge, the last data bit is clocked in and the programmed function is executed (that is, a change in DAC register contents and/or a change in the mode of operation). At this stage, the SYNC line can be kept low or be brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. Because the SYNC buffer draws more current when V_{IN} = 2.4 V than it does when V_{IN} = 0.8 V, $\overline{\text{SYNC}}$ should be idled low between write sequences for even lower power operation of the part. As previously mentioned, SYNC must be brought high again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 16 bits wide (see Figure 25). The first two bits are "don't cares." The next two are control bits that control which mode of operation the part is in (normal mode or any one of three power-down modes). There is a more complete description of the various modes in the Power-Down Modes section. The next twelve bits are the data bits. These are transferred to the DAC register on the 16th falling edge of SCLK.

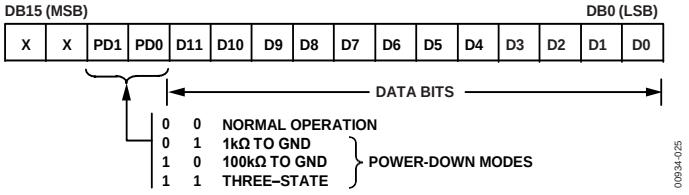


Figure 25. Input Register Contents

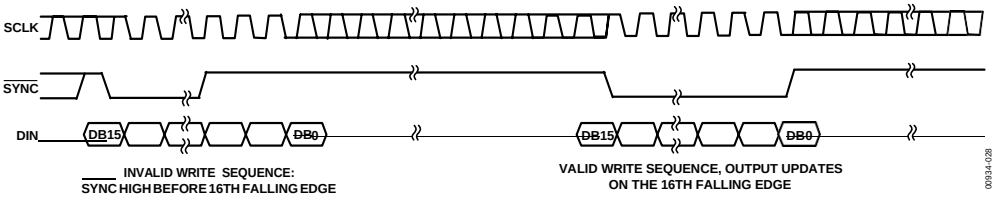


Figure 26. $\overline{\text{SYNC}}$ Interrupt Facility

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, if SYNC is brought high before the 16th falling edge, then this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 26).

POWER-ON RESET

The HT7512A contains a power-on reset circuit that controls the output voltage during power-up. The DAC register is filled with zeros and the output voltage is 0 V. It remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

POWER-DOWN MODES

The HT7512A contains four separate modes of operation. These modes are software-programmable by setting two bits (DB13 and DB12) in the control register. Table 5 shows how the state of the bits corresponds to the mode of operation of the device.

Table 5. Modes of Operation for the HT7512A

DB13	DB12	Operating Mode
0	0	Normal Operation
		Power-Down Modes
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-State

When both bits are set to 0, the part works with its normal power consumption of 140 µA at 5 V. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options: the output is connected internally to GND through a 1 kΩ resistor, the output is connected internally to GND through a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 27.

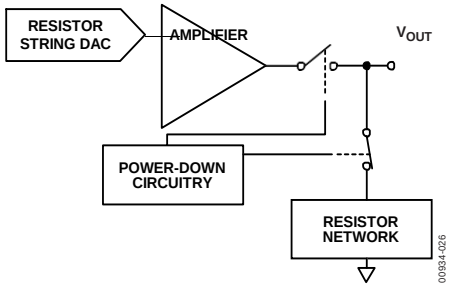


Figure 27. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 µs for V_{DD} = 5 V and 5 µs for V_{DD} = 3 V (see Figure 21).

MICROPROCESSOR INTERFACING

HT7512A TO ADSP-2101/ADSP-2103 INTERFACE

Figure 28 shows a serial interface between the and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in the serial port (SPORT) transmit alternate framing mode. The ADSP-2101/ADSP-2103 SPORT are programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, and 16-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.

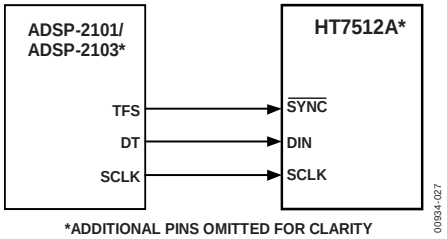


Figure 28. HT7512A to ADSP-2101/ADSP-2103 Interface

HT7512A TO 68HC11/68L11 INTERFACE

Figure 29 shows a serial interface between the HT7512A and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the HT7512A, while the MOSI output drives the serial data line of the DAC. The SYNC signal is derived from a port line (PC7). For correct operation of this interface, the 68HC11/68L11 should be configured so that the CPOL bit is a 0 and the CPHA bit is a 1. When data is to the DAC, the SYNC line is taken low (PC7). When the 68HC11/68L11 are configured, data appearing on the MOSI output is valid on the falling edge of SCK as shown in Figure 29.

Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the HT7512A, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC and PC7 is taken high at the end of this procedure.

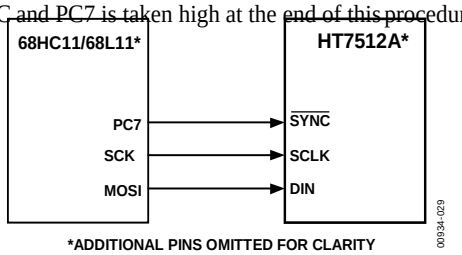


Figure 29. HT7512A to 68HC11/68L11 Interface

HT7512A TO 80C51/80L51 INTERFACE

Figure 30 shows a serial interface between the HT7512A and the 80C51/80L51 microcontrollers. TXD of the 80C51/80L51 drives SCLK of the HT7512A, while RXD drives the serial data line of the part. The SYNC signal is again derived from a bit programmable pin on the port. In this case, port line P3.3 is used. When data is to be transmitted to the HT7512A, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/ 80L51 output the serial data in a format that has the LSB first. The HT7512A requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine should consider this.

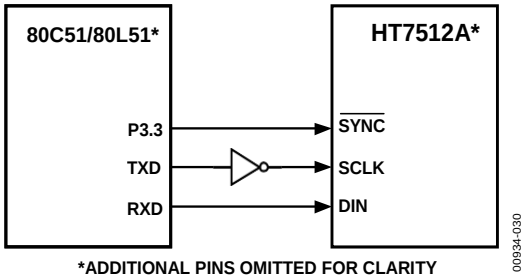


Figure 30. HT7512A to 80C51/80L51 Interface

HT7512A TO MICROWIRE INTERFACE

Figure 31 shows an interface between the HT7512A and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the HT7512A on the rising edge of the SK.

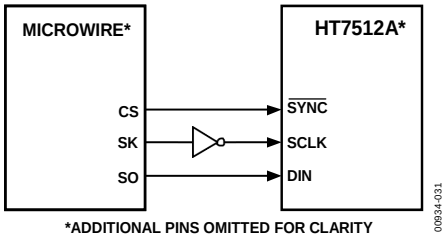


Figure 31. HT7512A to MICROWIRE Interface

APPLICATIONS

USING REF19X AS A POWER SUPPLY FOR HT7512A

Because the supply current required by the HT7512A is extremely low, an alternative option is to use a REF19x voltage reference (REF195 for 5 V or REF193 for 3 V) to supply the required voltage to the part (see Figure 32). This is especially useful if the power supply is noisy or if the system supply voltages are at some value other than 5 V or 3 V (such as 15 V). The REF19x outputs a steady supply voltage for the HT7512A. If the low dropout REF195 is used, the current it needs to supply to the HT7512A is 140 μA. This is with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is:

140 μA + (5 V/5 kΩ) = 1.14 mA

The load regulation of the REF195 is typically 2 ppm/mA, which results in an error of 2.3 ppm (11.5 μV) for the 1.14 mA current drawn from it. This corresponds to a 0.009 LSB error.

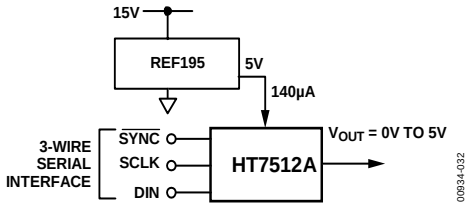


Figure 32. REF195 as Power Supply to HT7512A

BIPOLAR OPERATION USING THE HT7512A

The HT7512A is designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 33. The circuit below gives an output voltage range of ±5 V. Rail-to-rail
operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left(V_{DD} \times \frac{D}{4096} \times \frac{R1 + R2}{R1}\right) - V_{DD} \times \frac{R2}{R1}$$

where D represents the input code in decimal (0 to 4095).

With V_{DD} = 5 V, R1 = R2 = 10 kΩ:

$$V_O = \frac{10 \times D}{4096} - 5\ V$$

This is an output voltage range of ±5 V with 000 hex corresponding to a −5 V output and FFF hex corresponding to a +5 V output.

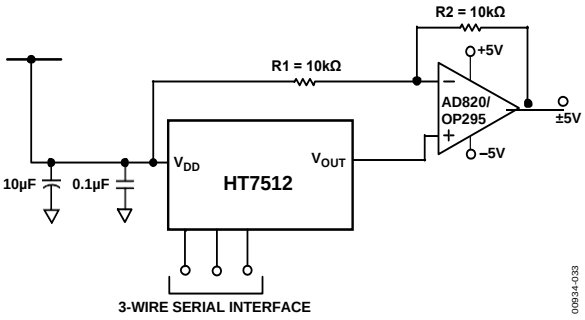


Figure 33. Bipolar Operation with the HT7512A

USING HT7512A WITH AN OPTO-ISOLATED INTERFACE

For process control applications in industrial environments, it is often necessary to use an opto-isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that can occur in the area where the DAC is functioning. Opto-isolators provide isolation in excess of 3 kV. Because the HT7512A uses a 3-wire serial logic interface, it requires only three opto-isolators to provide the required isolation (see Figure 34). The power supply to the part also needs to be isolated. This is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the HT7512A.

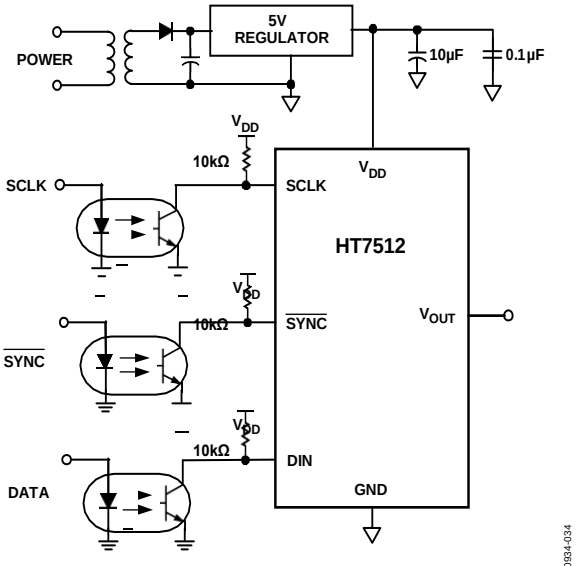
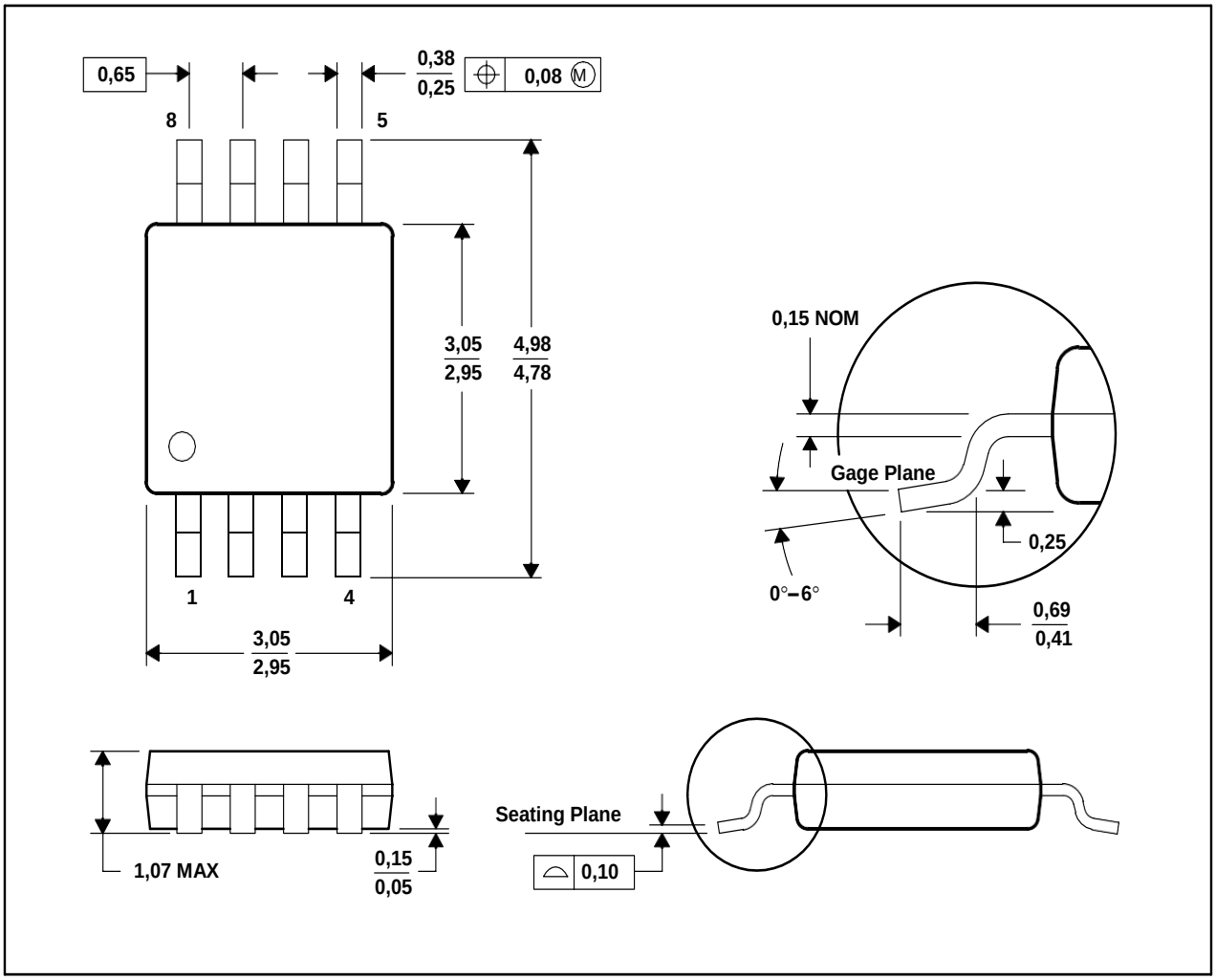


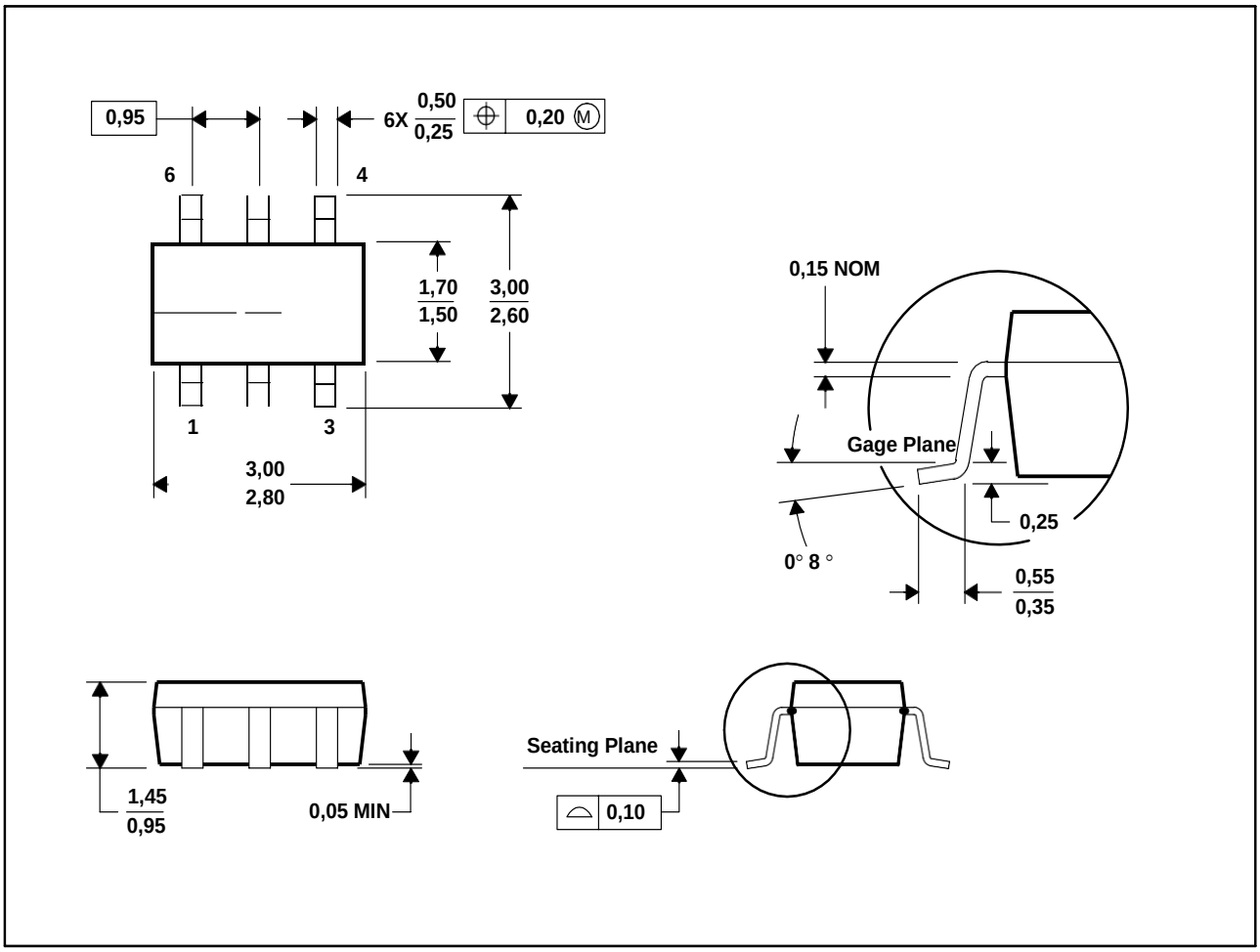
Figure 34. HT7512A with An Opto-Isolated Interface

MSOP8



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

SOT23-6



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.

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