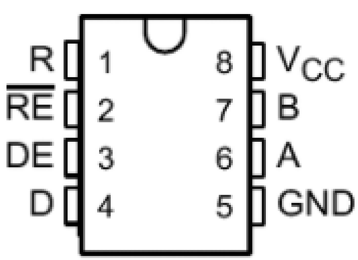
Differential Bus Transceivers

FEATURES

- **Bidirectional Transceivers**
- **Meet or Exceed the Requirements of ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Driver and Receiver Outputs**
- **Individual Driver and Receiver Enables**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **± 60-mA Max Driver Output Capability**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **12-kΩ Min Receiver Input Impedance**
- **± 200-mV Receiver Input Sensitivity**
- **50-mV Typ Receiver Input Hysteresis**
- **Operate From Single 5-V Supply**



HT65176ARZ,HT75176ARZ
HT65176ANZ,HT75176ANZ

DESCRIPTION

The HT65176 and HT75176 differential bus transceivers are integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27.

The HT65176 and HT75176 devices combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The driver is designed for up to 60 mA of sink or source current. The driver features positive and negative current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The HT65176 and HT75176 devices can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

Function Tables

Driver (1)

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

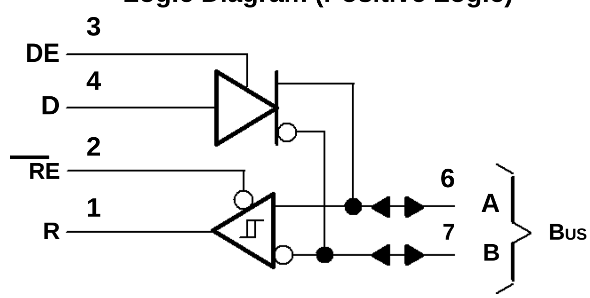
(1) H = high level,
L = low level,
? = indeterminate,
X = irrelevant,
Z = high impedance (off)

Receiver(1)

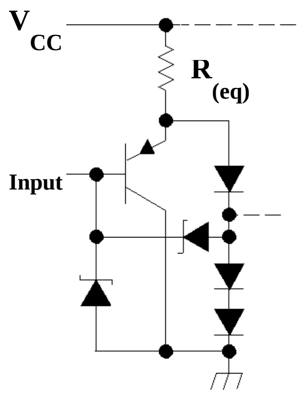
DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	?

(1) H = high level,
L = low level,
? = indeterminate,
X = irrelevant,
Z = high impedance (off)

Logic Diagram (Positive Logic)



EQUIVALENT OF EACH INPUT

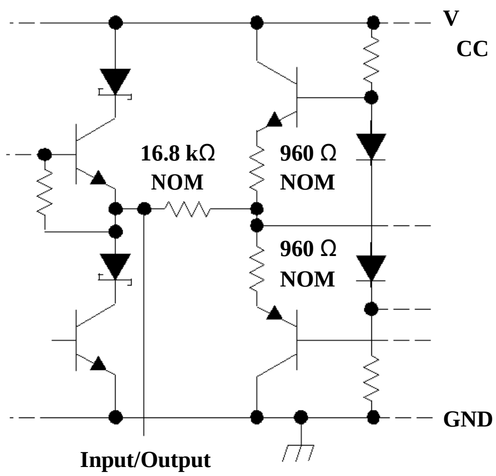


Driver input: R(eq) = 3 kΩ NOM

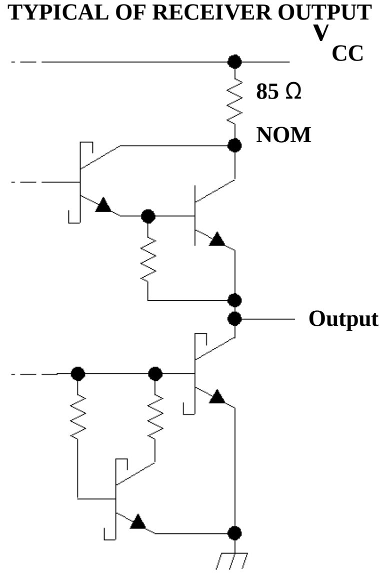
Enable inputs: R(eq) = 8 kΩ NOM

R(eq) = Equivalent Resistor

TYPICAL OF A AND B I/O PORTS



TYPICAL OF RECEIVER OUTPUT



Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[2]			7	V
	Voltage range at any bus terminal		–10	15	V
V_I	Enable input voltage			5.5	V
θ_{JA}	Package thermal impedance[3][4]	D package		97	°C/W
		P package		85	
		PS package		95	
T_J	Operating virtual junction temperature			150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
(3) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)				12	V
					–7	
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage[1]				±12	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	µA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature	HT65176	–40		105	°C
		HT75176	0		70	

(1) Differential input/output bus voltage is measured at the noninverting terminal A, with respect to the inverting terminal B.

Driver Section

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5	3.6	6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, see Figure 1		1/2 V_{OD1} or 2[3]			V
		R_L = 54 Ω, see Figure 1		1.5	2.5	5	
V_{OD3}	Differential output voltage	See [4]		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage[5]	R_L = 54 Ω or 100 Ω, see Figure 1				±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω, see Figure 1				+3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage[5]	R_L = 54 Ω or 100 Ω, see Figure 1				±0.2	V
I_O	Output current	Output disabled[6]	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	μA
I_{OS}	Short-circuit output current	V_O = –7 V				–250	mA
		V_O = 0				–150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

(1) The power-off measurement in ANSI Standard TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
(4) See ANSI Standard TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.
(5) $\|V_{OD}\|$ and $\|V_{OC}\|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(6) This applies for both power on and off; refer to ANSI Standard TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

Switching Characteristics

V_{CC} = 5 V, R_L = 110 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω, see Figure 3		15	22	ns
$t_{t(OD)}$	Differential-output transition time	R_L = 54 Ω, see Figure 3		20	30	ns
t_{PZH}	Output enable time to high level	See Figure 4		85	120	ns
t_{PZL}	Output enable time to low level	See Figure 5		40	60	ns
t_{PHZ}	Output disable time from high level	See Figure 4		150	250	ns
t_{PLZ}	Output disable time from low level	See Figure 5		20	30	ns

Symbol Equivalents

DATA SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (test termination measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\bar{V}_t\|\|$	$\|\|V_t\| - \|\bar{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \bar{V}_{os}\|$	$\|V_{os} - \bar{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

Receiver Section

Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[(1)]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V, I_O = –0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V, I_O = 8 mA		–0.2[(2)]			V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Enable Input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –400 μA, see Figure 2		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA, see Figure 2				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V[(3)]	V_I = 12 V			1	mA
			V_I = –7 V			–0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				–100	μA
r_I	Input resistance	V_I = 12 V		12			kΩ
I_{OS}	Short-circuit output current			–15		–85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for both power on and power off. Refer to EIA Standard TIA/EIA-485-A for exact conditions.

Switching Characteristics

V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 to 3 V, see Figure 6		21	35	ns
t_{PHL}	Propagation delay time, high- to low-level output			23	35	
t_{PZH}	Output enable time to high level	See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level			12	20	
t_{PHZ}	Output disable time from high level	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	

Parameter Measurement Information

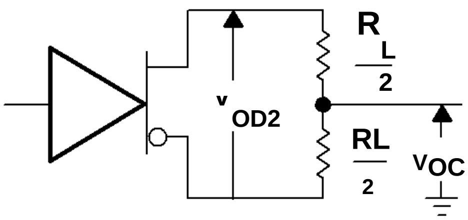


Figure 1. Driver V_{OD} and V_{OC}

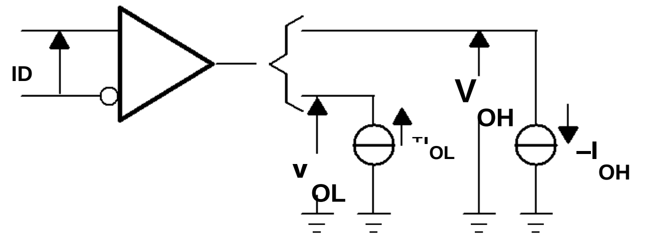
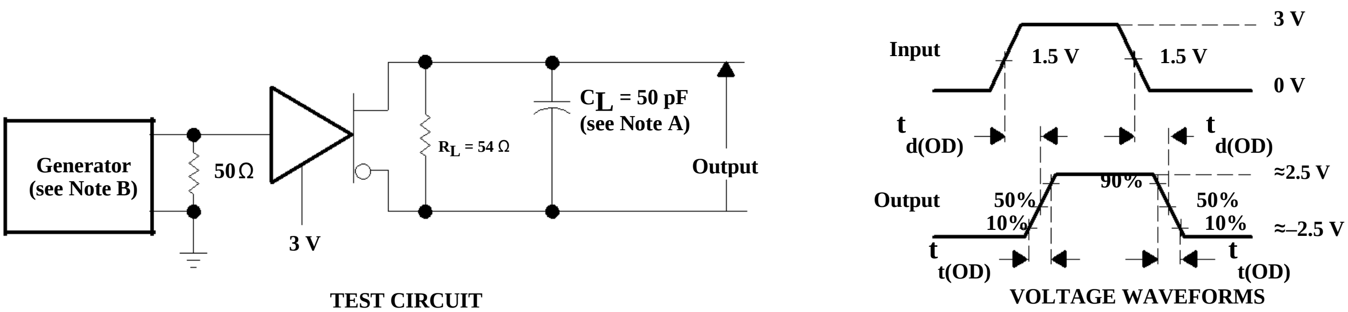


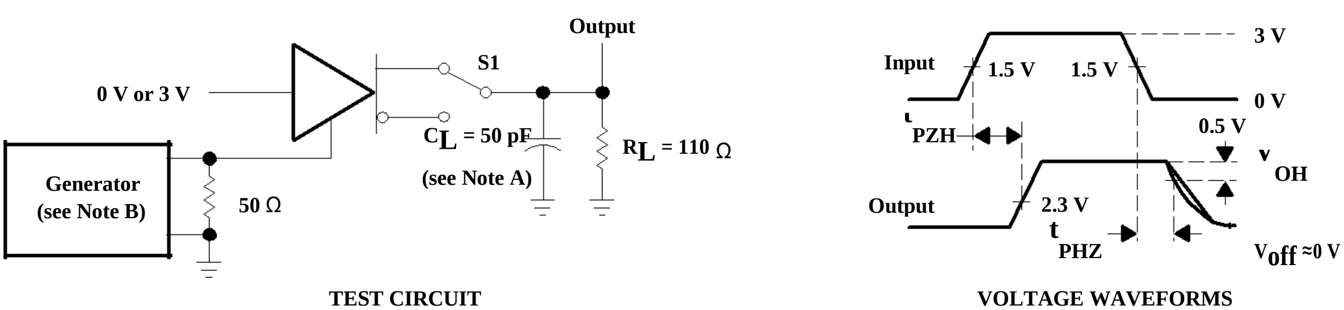
Figure 2. Receiver V_{OH} and V_{OL}



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.

Figure 3. Driver Test Circuit and Voltage Waveforms

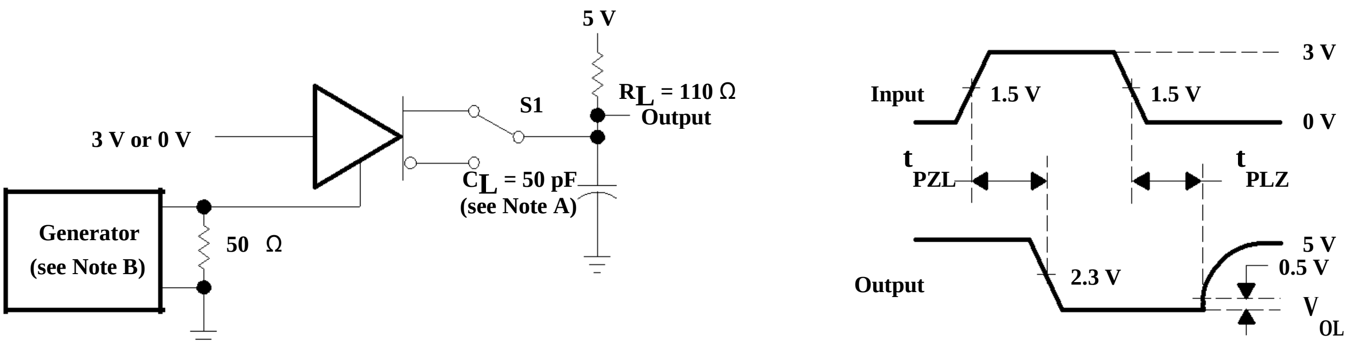


A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.

Figure 4. Driver Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



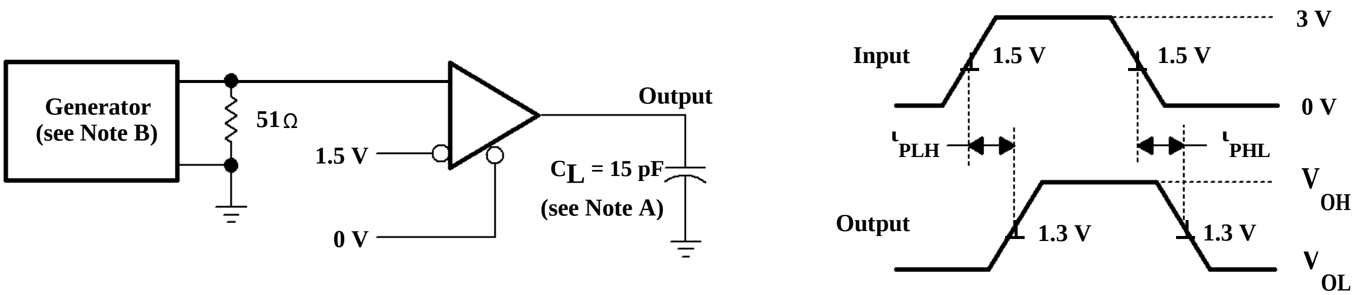
TEST CIRCUIT

VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.

Figure 5. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

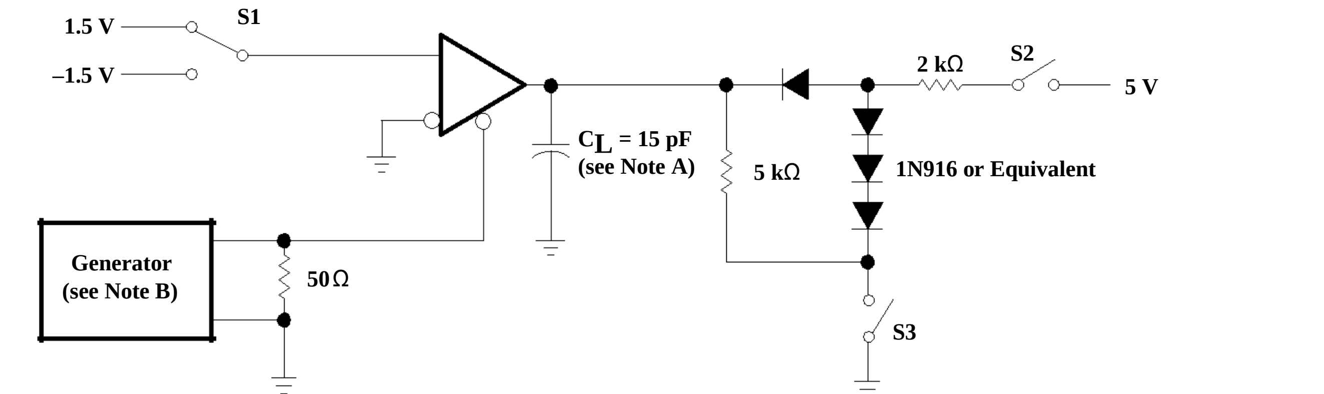
VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

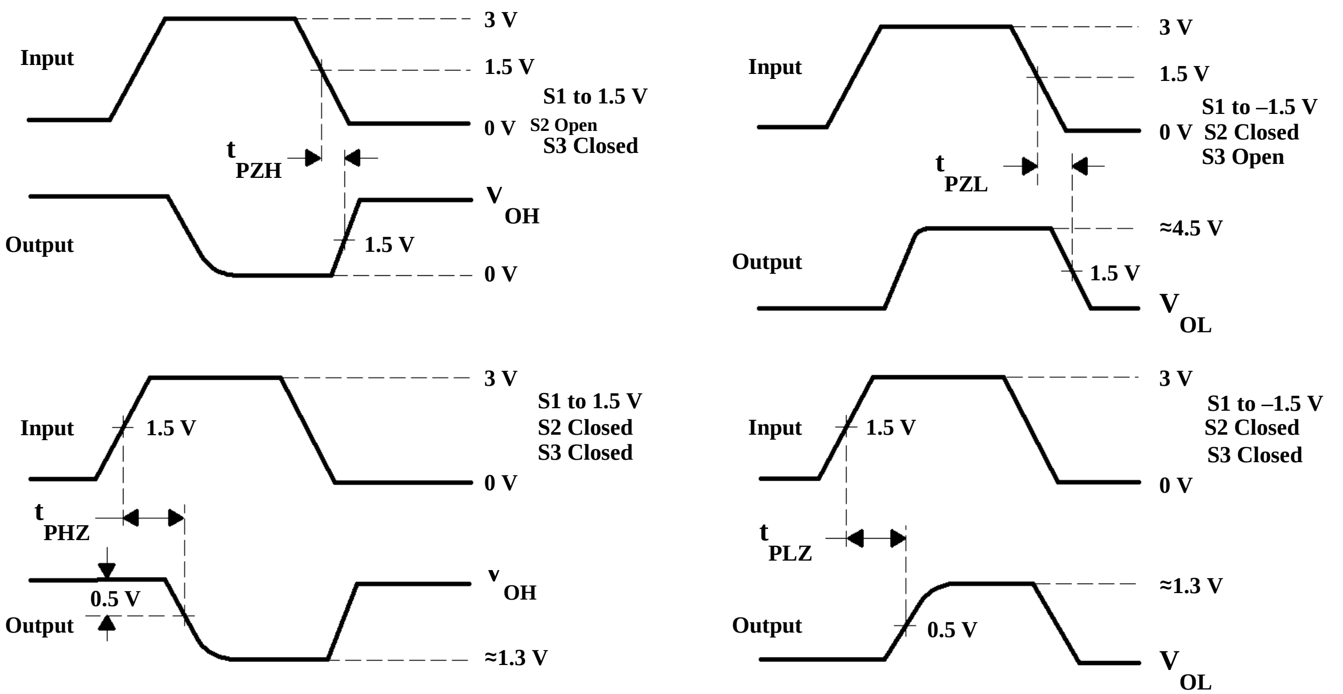
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.

Figure 6. Receiver Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 7. Receiver Test Circuit and Voltage Waveforms

Typical Characteristics

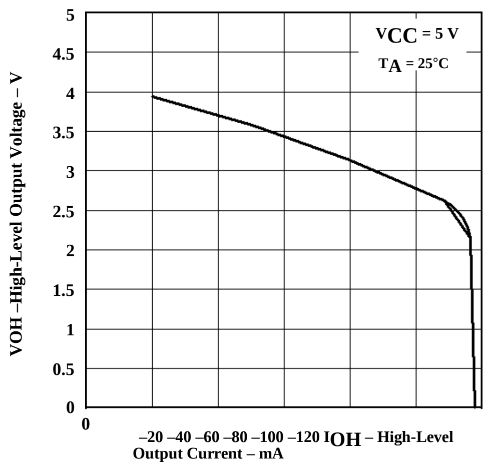


Figure 8. Driver High-Level Output Voltage vs High-Level Output Current

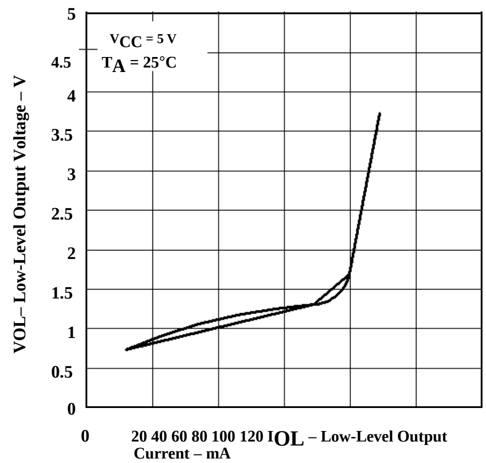


Figure 9. Driver Low-Level Output Voltage vs Low-Level Output Current

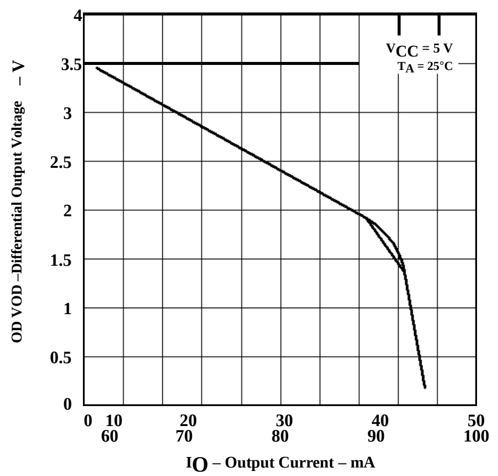


Figure 10. Driver Differential Output Voltage vs Output Current

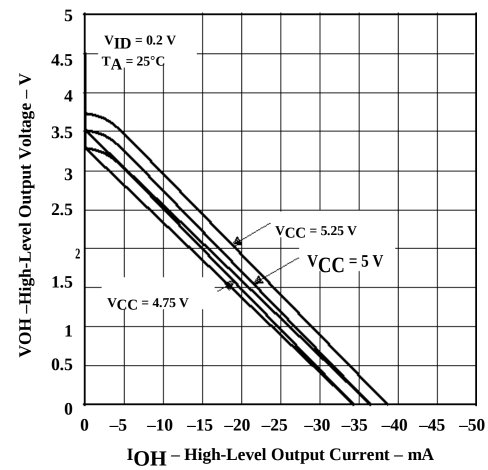
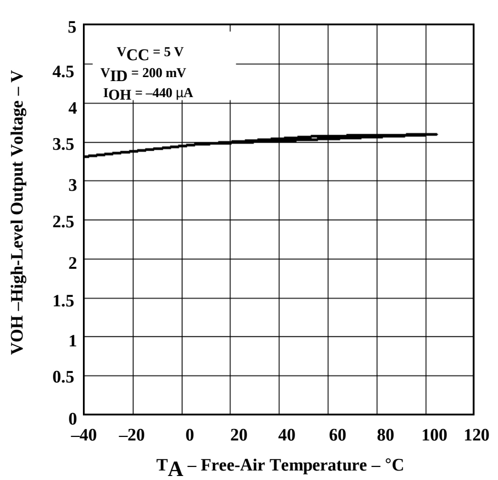
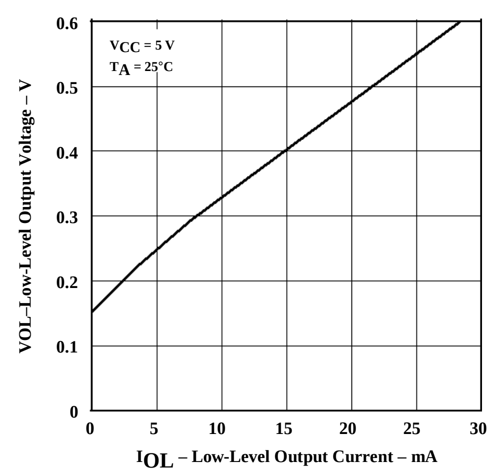


Figure 11. Receiver High-Level Output Voltage vs High-Level Output Current





Typical Characteristics (continued)

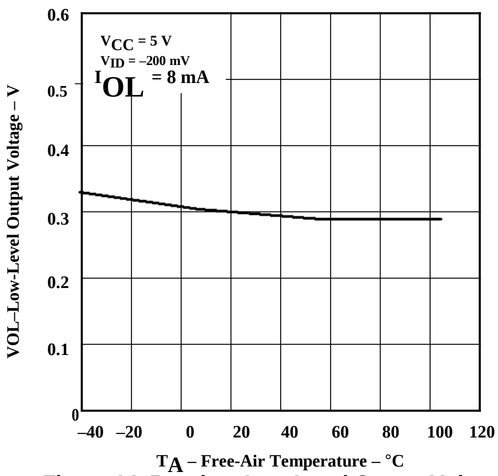


Figure 14. Receiver Low-Level Output Voltage
vs
Free-Air Temperature

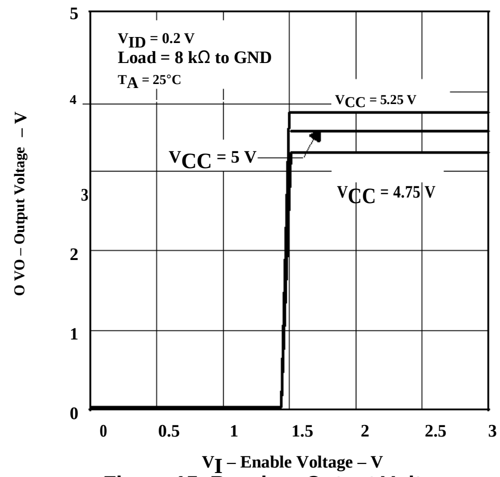


Figure 15. Receiver Output Voltage
vs
Enable Voltage

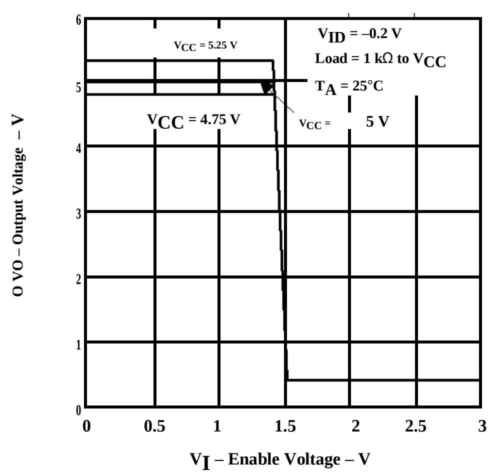
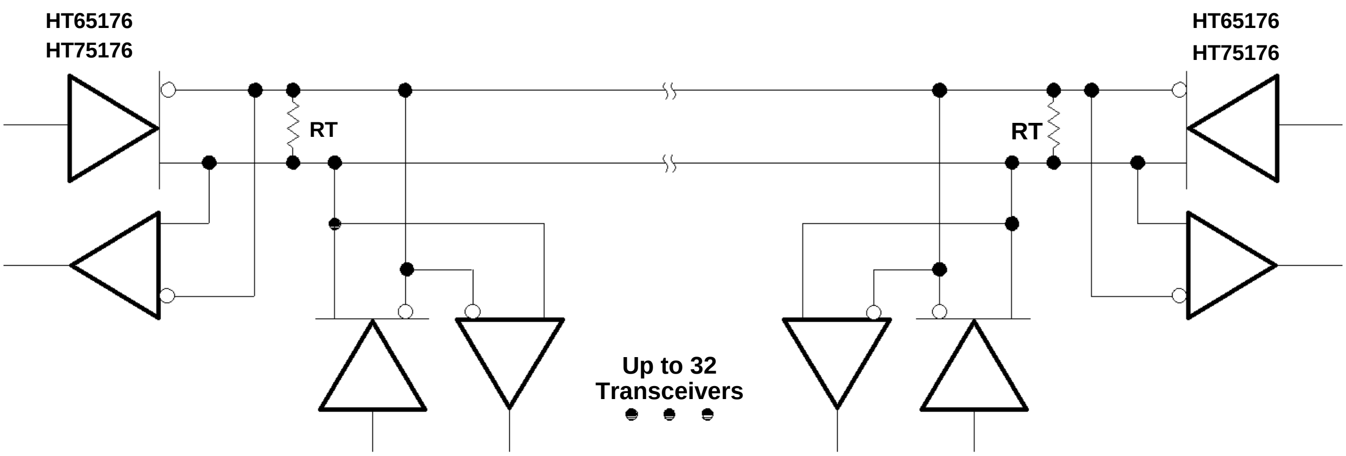


Figure 16. Receiver Output Voltage
vs
Enable Voltage

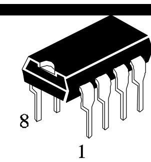
APPLICATION INFORMATION

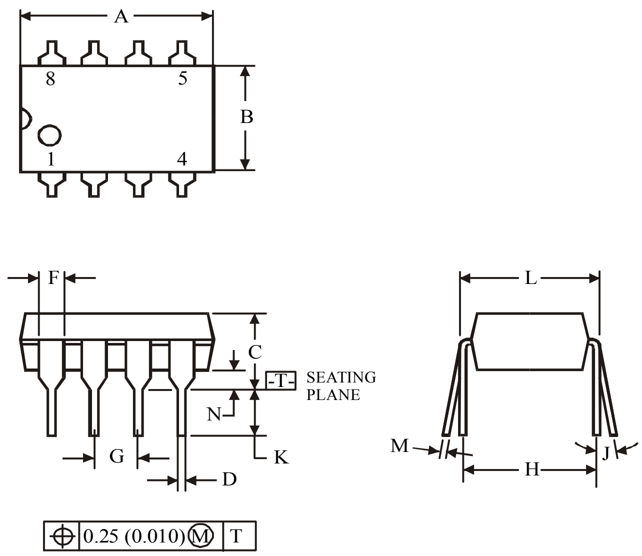


The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 17. Typical Application Circuit

(DIP8)



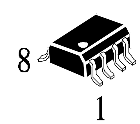


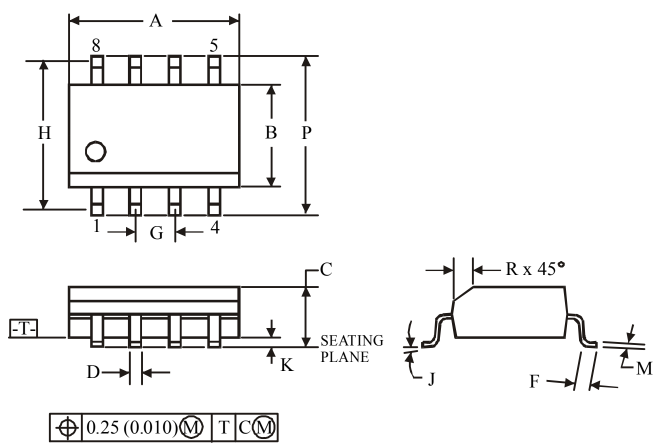
	Dimension, mm	
Symbol	MIN	MAX
A	8.51	10.16
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

(SOP8)





	Dimension, mm	
Symbol	MIN	MAX
A	4.8	5
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side
   for A; for B ‑ 0.25 mm (0.010) per side.