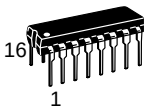
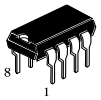
Chopper Stabilized Operational Amplifier

Features

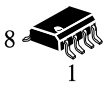
- Low Input Offset Voltage: 0.7μV Typ
- Low Input Offset Voltage Drift: 0.05μV/°C Max
- Low Input Bias Current: 10pA Max
- High Impedance Differential CMOS Inputs: $10^{12}\Omega$
- High Open Loop Voltage Gain: 120dB Min.
- Low Input Noise Voltage: 2.0μVp-p
- High Slew Rate: 2.5V/μsec.
- Low Power Operation: 20mW
- Output Clamp Speeds Recovery Time
- Compensated Internally for Stable Unity Gain Operation
- Direct Replacement for ICL7650
- Available in 8-Pin Plastic DIP and 14-Pin Plastic DIP Packages



DIP16 D SUFFIX HT7650ANDZ



DIP8−8 N SUFFIX HT7650ANZ



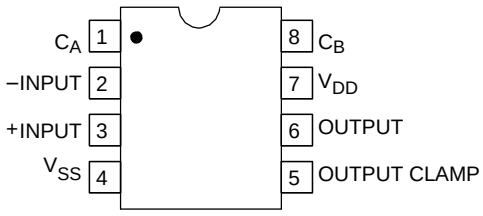
SOP−8 R SUFFIX HT7650ARZ

Applications

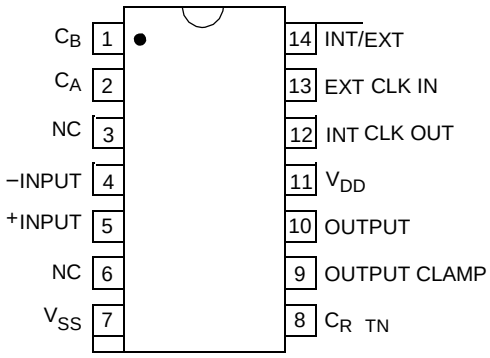
- Instrumentation
- Medical Instrumentation
- Embedded Control
- Temperature Sensor Amplifier
- Strain Gage Amplifier

Package Type

8-Pin DIP/SOP



14-Pin DIP



NC = NO INTERNAL CONNECTION

General Description

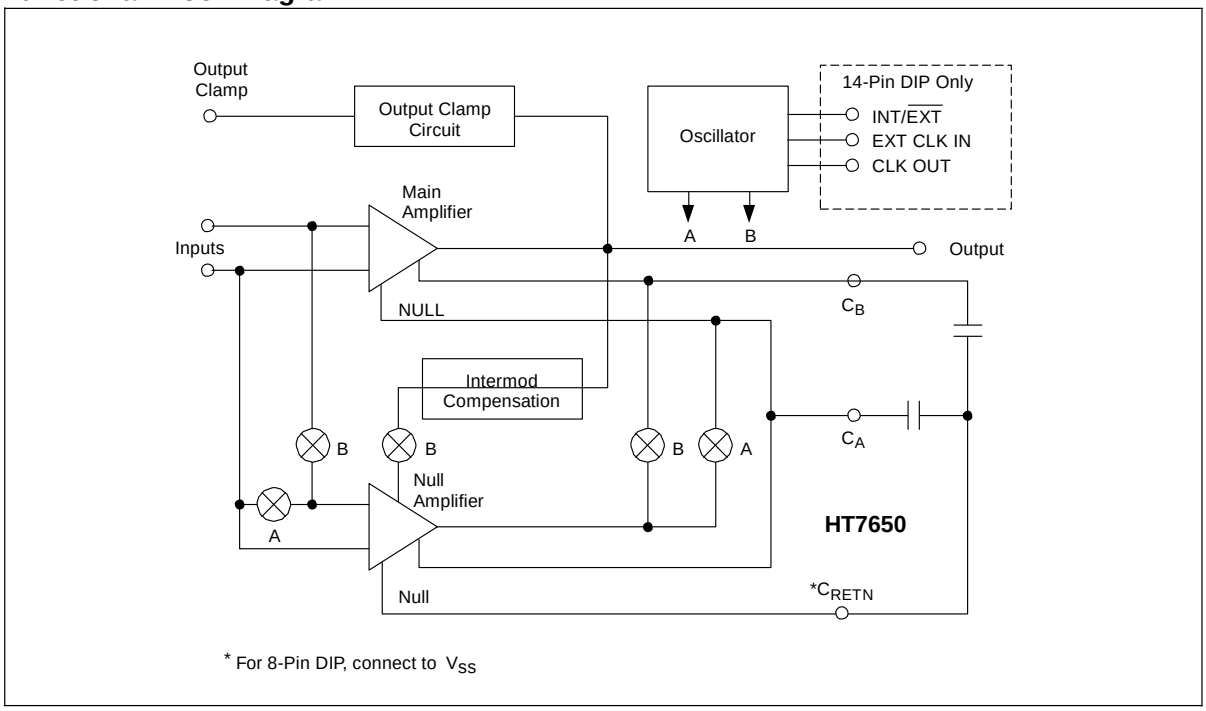
The HT7650 CMOS chopper stabilized operational amplifier practically removes offset voltage error terms from system error calculations. The 5μV maximum V_{OS} specification, for example, represents a 15 times improvement over the industry standard OP07E. The 50nV/°C offset drift specification is over 25 times lower than the OP07E. The increased performance eliminates V_{OS} trim procedures, periodic potentiometer adjustment and the reliability problems caused by damaged trimmers.

The HT7650 performance advantages are achieved without the additional manufacturing complexity and cost incurred with laser or "zener zap" V_{OS} trim techniques.

The HT7650 nulling scheme corrects both DC V_{OS} errors and V_{OS} drift errors with temperature. A nulling amplifier alternately corrects its own V_{OS} errors and the main amplifier V_{OS} error. Offset nulling voltages are stored on two user supplied external capacitors. The capacitors connect to the internal amplifier V_{OS} null points. The main amplifier input signal is never switched. Switching spikes are not present at the HT7650 output.

The 14-pin dual-in-line package (DIP) has an external oscillator input to drive the nulling circuitry for optimum noise performance. Both the 8 and 14-pin DIPs have an output voltage clamp circuit to minimize overload recovery time.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Total Supply Voltage (V_{DD} to V_{SS}) .....+18V
Input Voltage ..... (V_{DD} +0.3V) to (V_{SS} – 0.3V)
Storage Temperature Range ..... -65°C to +150°C
Voltage on Oscillator Control Pins.....V_{DD} to V_{SS}
Duration of Output Short Circuit ..... Indefinite
Current Into Any Pin..... 10mA
While Operating (**Note 3**)..... 100µA
Package Power Dissipation ($T_A \leq$ 70°C)
8-Pin Plastic DIP 730mW
14-Pin Plastic DIP 800mW
Operating Temperature Range
C Device ..... 0°C to +70°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods my affect device reliability.

TC7652 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V_{DD} = +5V, V_{SS} = -5V, C_A = C_B = 0.1µF, T_A = +25°C, unless otherwise indicated.

Symbol	Parameter	Min.	Typ	Max	Units	Test Conditions
Input						
V_{OS}	Input Offset Voltage	— —	±0.7 ±1.0	±5 —	— µV	T_A = +25°C Over Operating Temp Range
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Temperature Coefficient	—	0.01	0.05	µV/°C	Operating Temperature Range
	Offset Voltage vs. Time	—	100	—	nV/mont	
I_{BIAS}	Input Bias Current	— — —	1.5 35 100	10 150 400	pA pA pA	T_A = +25°C 0°C ≤ T_A ≤ +70°C -25°C ≤ T_A ≤ +85°C
I_{OS}	Input Offset Current	—	0.5	—	pA	
e_{NP-P}	Input Noise Voltage	—	2	—	μV_{P-P}	R_S = 100Ω, 0 to 10Hz
I_N	Input Noise Current	—	0.01	—	pA/√Hz	f= 10Hz
R_{IN}	Input Resistance	—	10^{12}		Ω	
CMVR	Common Mode Voltage Range	-5	-5.2 to +2	+1.6	V	
CMRR	Common Mode Rejection Ratio	120	130	—	dB	CMVR = -5V to +1.5V
Output						
A	Large Signal Voltage Gain	120	130	—	dB	R_L = 10kΩ
V_{OUT}	Output Voltage Swing (**Note 2**)	±4.7 —	±4.85 ±4.95	— —	V V	R_L = 10kΩ R_L = 100kΩ
	Clamp ON Current	25	70	200	µA	R_L = 100kΩ (**Note 1**)
	Clamp OFF Current	—	1	—	pA	-4V < V_{OUT} < +4V (**Note 1**)
Dynamic						
B_W	Unity Gain Bandwidth	—	2.0	—	MHz	Unity Gain (+1)
S_R	Slew Rate	—	2.5	—	V/µsec	C_L = 50pF, R_L = 10kΩ
t_R	Rise Time	—	0.2	—	µsec	
	Overshoot	—	20	—	%	
f_{CH}	Internal Chopping Frequency	120	200	375	Hz	Pins 12–14 Open (DIP)
Supply						
V_{DD}, V_{SS}	Operating Supply Range	4.5	—	16	V	
I_S	Supply Current	—	2	3.5	mA	No Load
PSRR	Power Supply Rejection Ratio	120	130		dB	V_S = ±3V to ±8V

Note 1: See "Output Clamp" discussion.
2: Output clamp not connected. See typical characteristics curves for output swing versus clamp current characteristics.
3: Limiting input current to 100µA is recommended to avoid latch-up problems.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number		Symbol	Description
8-pin DIP	14-pin DIP		
1,8	2,1	C_A, C_B	Nulling capacitor pins
2	4	-INPUT	Inverting Input
3	5	+INPUT	Non-inverting Input
4	7	V_{SS}	Negative Power Supply
5	9	OUTPUT CLAMP	Output Voltage Clamp
6	10	OUTPUT	Output
7	11	V_{DD}	Positive Power Supply
—	3,6	NC	No internal connection
—	8	C_{RETN}	Capacitor current return pin
—	12	INT CLK OUT	Internal Clock Output
—	13	EXT CLK IN	External Clock Input
—	14	INT/EXT	Select Internal or External Clock

3.1 DETAILED DESCRIPTION

3.2 Theory of Operation

Figure 3-1 shows the major elements of the HT7650. There are two amplifiers (the main amplifier and the nulling amplifier), and both have offset null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. Two external capacitors provide the required storage of the nulling potentials and the necessary nulling loop time constants. The nulling arrangement operates over the full common mode and power supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR and A_{VOL}.

Careful balancing of the input switches minimizes chopper frequency charge injection at the input terminals, and the feed forward type injection into the compensation capacitor that can cause output spikes in this type of circuit.

The circuit's offset voltage compensation is easily shown. With the nulling inputs shorted, a voltage almost identical to the nulling amplifier offset voltage is stored on C_A. The effective offset voltage at the null amplifier input is:

EQUATION 3-1:

$$V_{OSE} = \frac{1}{A_N + 1} V_{OSN}$$

After the nulling amplifier is zeroed, the main amplifier is zeroed; the A switches open and B switches close.

The output voltage equation is:

EQUATION 3-2:

$$V_{OUT} = A_M[V_{OSM} + (V^+ - V^-) + A_N(V^+ - V^-) + A_N V_{OSE}]$$

EQUATION 3-3:

$$V_{OUT} = A_M A_N\left[(V^+ - V^-) + \frac{V_{OSM} + V_{OSN}}{A_N}\right]$$

As desired, the device offset voltages are reduced by the high open loop gain of the nulling amplifier.

3.3 Output Stage/Loading

The output circuit is a high impedance stage (approximately 18kΩ). With loads less than this, the chopper amplifier behaves in some ways like a trans-conductance amplifier whose open-loop gain is proportional to load resistance. For example, the open loop gain will be 17dB lower with a 1kΩ load than with a 10kΩ load. If the amplifier is used strictly for DC, the lower gain is of little consequence, since the DC gain is typically greater than 120dB, even with a 1kΩ load. In wideband applications, the best frequency response will be achieved with a load resistor of 10kΩ or higher. This results in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° in the transi-

tion region, where the main amplifier takes over from the null amplifier. The clock frequency sets the transition region.

3.4 Intermodulation

Previous chopper stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier results in a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies, and causing disturbances to the gain and phase versus frequency characteristics near the chopping frequency. These effects are substantially reduced in the HT7650 by feeding the nulling circuit with a dynamic current corresponding to the compensation capacitor current in such a way as to cancel that portion of the input signal due to a finite AC gain. The intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

FIGURE 3-1: HT7650 CONTAINS A NULLING AND MAIN AMPLIFIER. OFFSET CORRECTION VOLTAGES ARE STORED ON TWO EXTERNAL CAPACITORS.

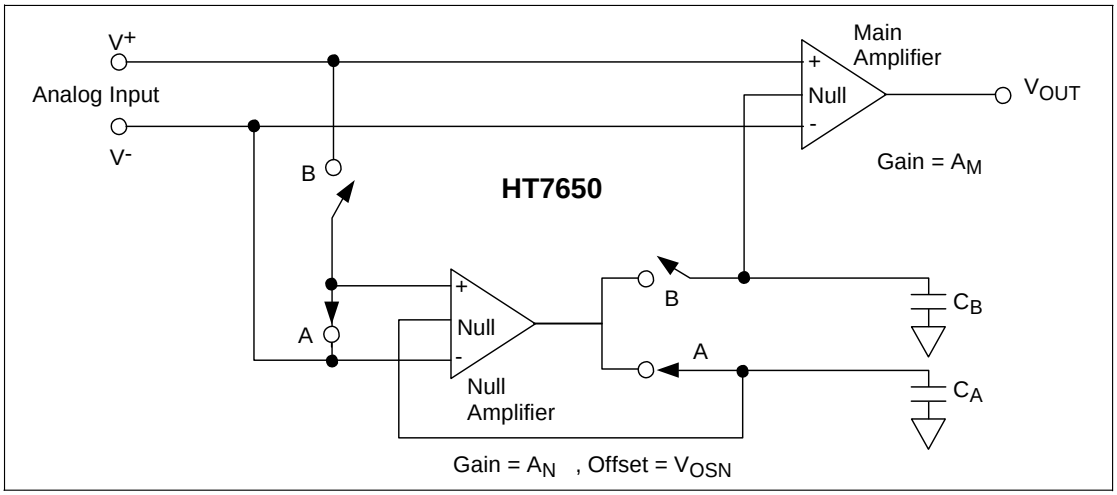
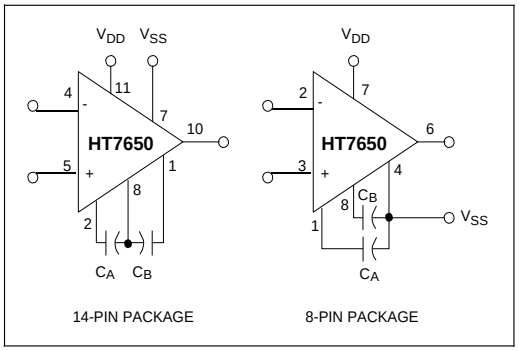


FIGURE 3-2: NULLING CAPACITOR CONNECTION



3.4 Nulling Capacitor Connection

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_{SS} (Pin 4) on the 8-pin packages and to capacitor return (C_{RETN}, Pin 8) on the 14-pin packages. The common connection should be made through a separate PC trace or wire to avoid voltage drops. The capacitors outside foil, if possible, should be connected to C_{RETN} or V_{SS}.

3.5 Clock Operation

The internal oscillator is set for a 200Hz nominal chopping frequency on both the 8- and 14-pin DIPs. With the 14-pin DIP HT7650, the 200 Hz internal chopping frequency is available at the internal clock output (Pin 12). A 400Hz nominal signal will be present at the external clock input pin (Pin 13) with INT/EXT high or open. This is the internal clock signal before a divide-by-two operation.

The 14-pin DIP device can be driven by an external clock. The INT/EXT input (Pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used, INT/EXT must be tied to V_{SS} (Pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (Pin 13).

The external clock amplitude should swing between V_{DD} and ground for power supplies up to ±6V and between V^+ and V^+ -6V for higher supply voltages.

At low frequencies the external clock duty cycle is not critical, since an internal divide-by-two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50% to 80% external clock

positive duty cycle is desired for frequencies above 500Hz to ensure transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is LOW during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitors pins are very low. At 25°C a typical HT7650 will drift less than 10μV/sec.

3.6 Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the HT7650 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

FIGURE 3-3: INTERNAL CLAMP CIRCUIT

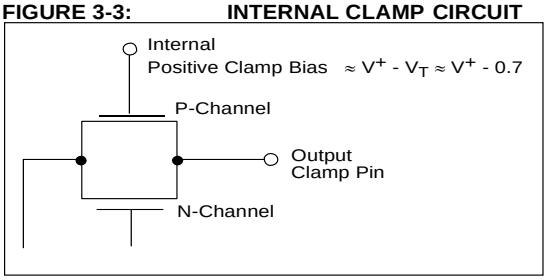


FIGURE 3-4: NON-INVERTING AMPLIFIER WITH OPTIONAL CLAMP

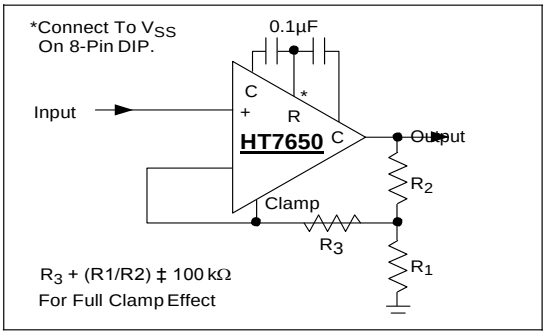
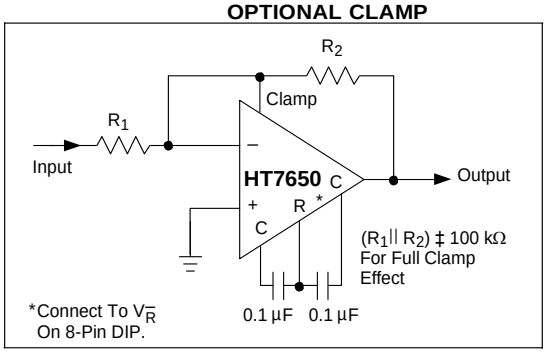


FIGURE 3-5: INVERTING AMPLIFIER WITH OPTIONAL CLAMP



The output clamp circuit is shown in Figure 3-3, with typical inverting and non-inverting circuit connections shown in Figures 3-4 and 3-5. Output voltage versus clamp circuit current characteristics are shown in the typical operating curves. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100kΩ.

3.7 Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1mA to avoid latch-up.

3.8 Thermoelectric Potentials

Precision DC measurements are ultimately limited by thermoelectric potentials developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages, typically around 0.1μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the benefits extremely-low offset voltages provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially those caused by power dissipating elements in the system. Low thermoelectric co-efficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High impedance loads are preferable, and separation from surrounding heat dissipating elements is advised.

3.9 Pin Compatibility

On the 8-pin mini-DIP HT7650, the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or are used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, the replacement of the offset null potentiometer between pins 1 and 8 by two capacitors from the pins to V_{SS} will convert the OP05/07 pin configurations for HT7650 operation. For LM108 devices, the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pinouts are modified similarly by removing any circuit connections to Pin 5. On the HT7650, Pin 5 is the output clamp connection.

Other operational amplifiers may use this pin as an offset or compensation point.

The minor modifications needed to retrofit a HT7650 into existing sockets operating at reduced power supply voltages make prototyping and circuit verification straightforward.

3.10 Input Guarding

High impedance, low leakage CMOS inputs allow the HT7650 to make measurements of high-impedance sources. Stray leakage paths can increase input currents and decrease input resistance unless inputs are guarded. A guard is a conductive PC trace surrounding the input terminals. The ring connects to a low impedance point at the same potential as the inputs. Stray leakages are absorbed by the low impedance ring. The equal potential between ring and inputs prevents input leakage currents. Typical guard connections are shown in Figure 3-6.

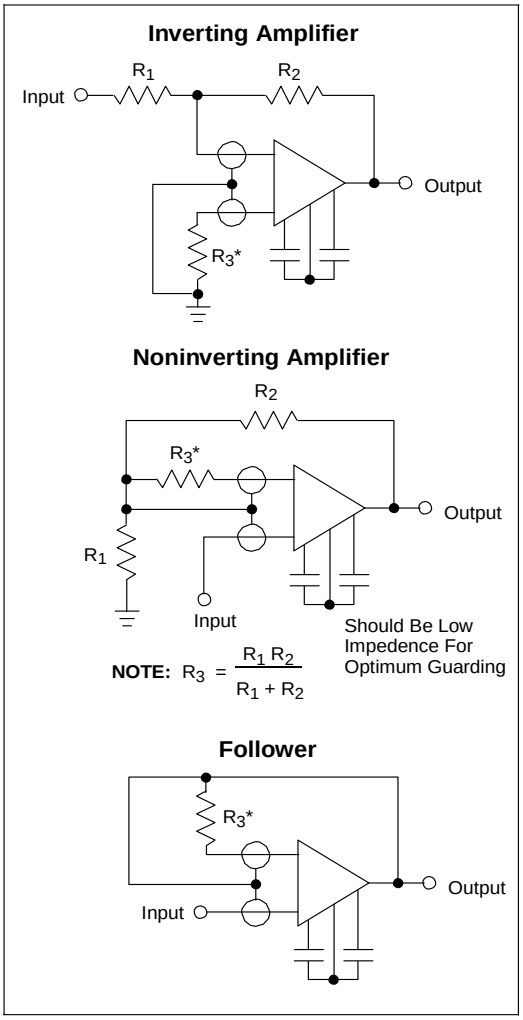
The 14-pin DIP configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are unused.

In applications requiring low leakage currents, boards should be cleaned thoroughly and blown dry after soldering. Protective coatings will prevent future board contamination.

3.11 Component Selection

The two required capacitors, C_A and C_B, have optimum values, depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1μF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock, if used. High quality film type capacitors (such as Mylar) are preferred; ceramic or other lower grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1μV.

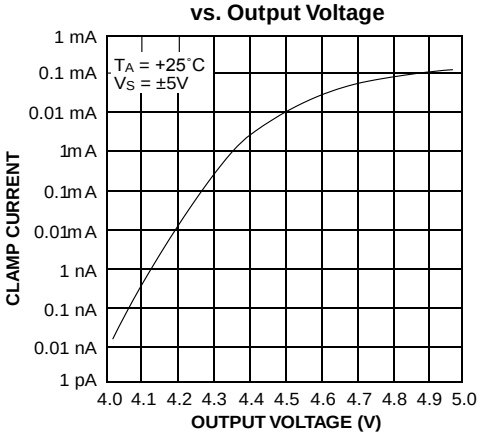
FIGURE 3-6: INPUT GUARD CONNECTION



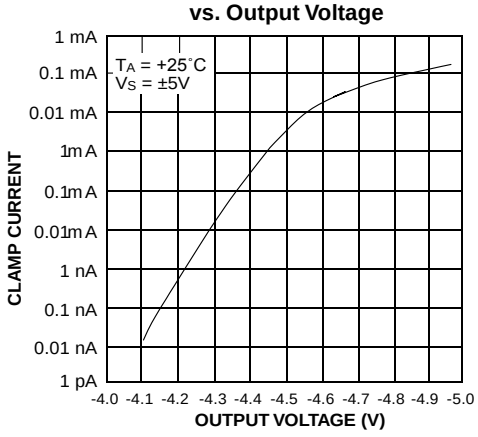
4.0 TYPICAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

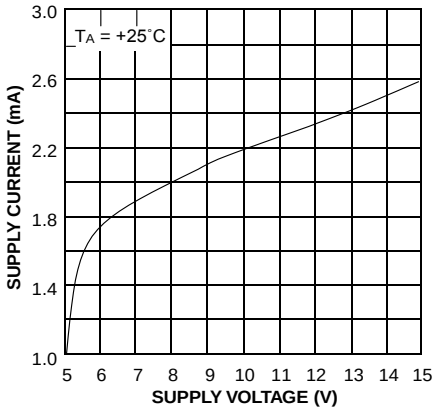
Positive Clamp Current vs. Output Voltage



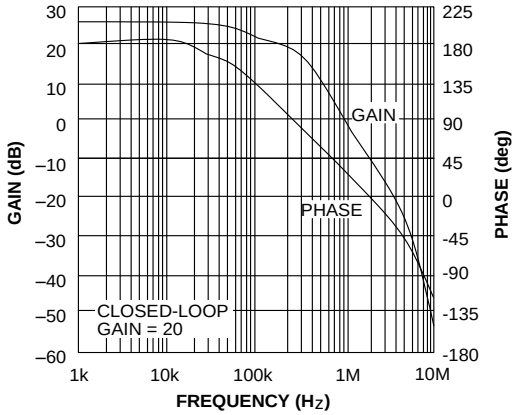
Negative Clamp Current vs. Output Voltage



Supply Current vs. Supply Voltage

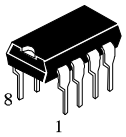


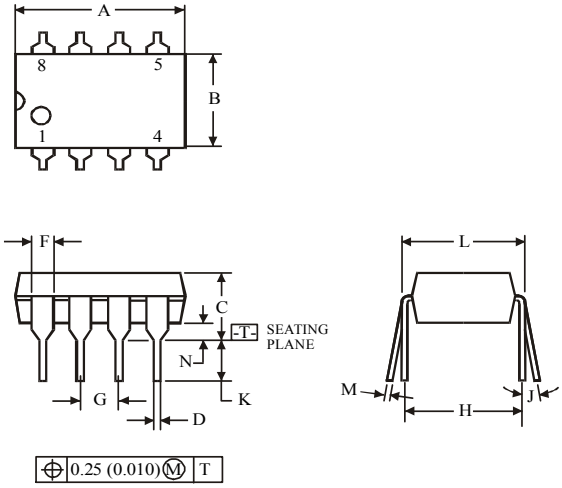
Gain/Phase vs. Frequency



Package Dimensions

DIP8



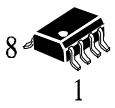


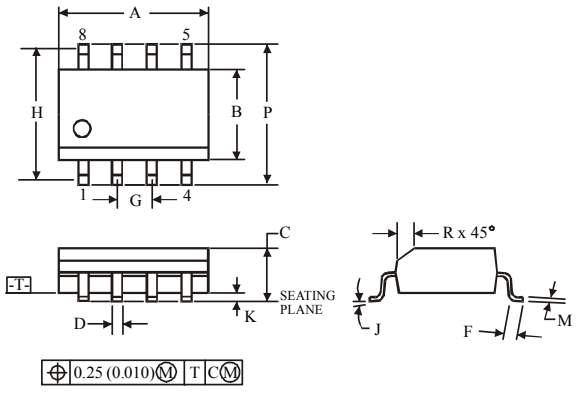
	Dimension, mm	
Symbol	**MIN**	**MAX**
A	8.51	10.16
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

SOPP8





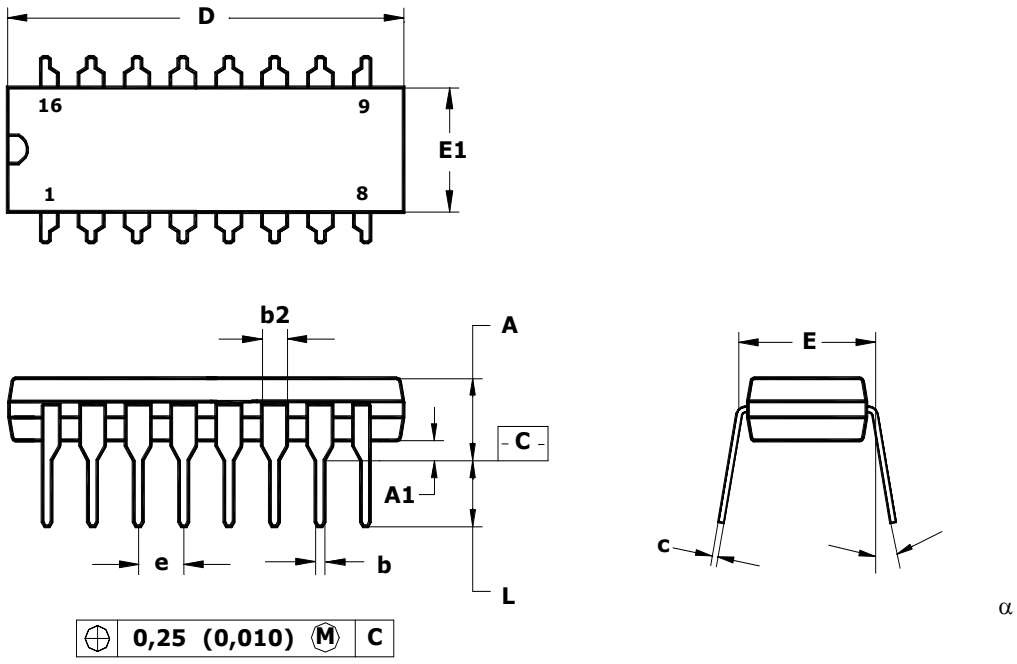
	Dimension, mm	
Symbol	**MIN**	**MAX**
A	4.8	5
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side
   for A; for B – 0.25 mm (0.010) per side.

Package Dimensions

DIP16



Note **-** Dimensions D, E1 do not include the fin value, which should not exceed 0.25 mm (0.010) per side.

	D	E1	A	b	b2	e	α	L	E	c	A1
mm											
min	18.93	6.07	—	0.36	1.14	2.54	0°	2.93	7.62	0.20	0.38
max	19.43	7.11	5.33	0.56	1.78		15°	3.81	8.26	0.36	—
Inches											
min	0.355	0.240	—	0.014	0.045	0.1	0°	0.115	0.300	0.008	0.015
max	0.400	0.280	0.210	0.022	0.070		15°	0.150	0.325	0.014	—

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