

# IC card interface

## 1 FEATURES

- IC card interface
- 3 or 5 V supply for the IC ( $V_{DD}$  and GND)
- Three specifically protected half-duplex bidirectional buffered I/O lines to card contacts C4, C7 and C8
- DC/DC converter for  $V_{CC}$  generation separately powered from a  $5\text{ V} \pm 20\%$  supply ( $V_{DDP}$  and PGND)
- 3 or  $5\text{ V} \pm 5\%$  regulated card supply voltage ( $V_{CC}$ ) with appropriate decoupling has the following capabilities:
  - $I_{CC} < 80\text{ mA}$  at  $V_{DDP} = 4\text{ to }6.5\text{ V}$
  - Handles current spikes of 40 nAs up to 20 MHz
  - Controls rise and fall times
  - Filtered overload detection at approximately 120 mA
- Thermal and short-circuit protection on all card contacts
- Automatic activation and deactivation sequences; initiated by software or by hardware in the event of a short-circuit, card take-off, overheating,  $V_{DD}$  or  $V_{DDP}$  drop-out
- Enhanced ESD protection on card side ( $>6\text{ kV}$ )
- 26 MHz integrated crystal oscillator
- Clock generation for cards up to 20 MHz (divided by 1, 2, 4 or 8 through CLKDIV1 and CLKDIV2 signals) with synchronous frequency changes
- Non-inverted control of RST via pin RSTIN
- ISO 7816, GSM11.11 and EMV (payment systems) compatibility
- Supply supervisor for spike-killing during power-on and power-off and Power-on reset (threshold fixed internally or externally by a resistor bridge); not for HT8024A
- Built-in debounce on card presence contacts
- One multiplexed status signal  $\overline{\text{OFF}}$ .

## 2 APPLICATIONS

- IC card readers for banking
- Electronic payment
- Identification
- Pay TV.

## 3 GENERAL DESCRIPTION

The HT8024A is a complete and cost-efficient analog interface for asynchronous 3 or 5 V smart cards. It can be placed between the card and the microcontroller to perform all supply, protection and control functions. Very few external components are required.

## 4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE	
	NAME	DESCRIPTION
HT8024ARWZ	SOP28	plastic small outline package; 28 leads; body width 7.5 mm
HT8024ARTZ	TSSOP28	plastic small outline package; 28 leads; body width 4.4 mm

**5 QUICK REFERENCE DATA**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Power supplies</b>						
V <sub>DD</sub>	supply voltage		2.7	–	6.5	V
V <sub>DDP</sub>	DC/DC converter supply voltage	V <sub>CC</sub> = 5 V;  I <sub>CC</sub>   < 80 mA	4.0	5.0	6.5	V
		V <sub>CC</sub> = 5 V;  I <sub>CC</sub>   < 20 mA	3.0	–	6.5	V
I <sub>DD</sub>	supply current	V <sub>DD</sub> = 3.3 V; f <sub>XTAL</sub> = 10 MHz card inactive	–	–	1.2	mA
		card active; f <sub>CLK</sub> = f <sub>XTAL</sub> ; C <sub>L</sub> = 30 pF	–	–	1.5	mA
I <sub>DDP</sub>	DC/DC converter supply current	V <sub>DDP</sub> = 5 V; f <sub>XTAL</sub> = 10 MHz inactive mode	–	–	0.1	mA
		active mode; f <sub>CLK</sub> = f <sub>XTAL</sub> ; C <sub>L</sub> = 30 pF;  I <sub>CC</sub>   = 0	–	–	10	mA
<b>Card supply</b>						
V <sub>CC</sub>	card supply voltage (including ripple voltage)	5 V card card active;  I <sub>CC</sub>   < 80 mA DC	4.75	5.0	5.25	V
		card active; current pulses I <sub>p</sub> = 40 nAs	4.65	5.0	5.25	V
		3 V card card active;  I <sub>CC</sub>   < 65 mA DC	2.85	3.0	3.15	V
		card active; current pulses I <sub>p</sub> = 40 nAs	2.76	3.0	3.20	V
V <sub>CC(ripple)(p-p)</sub>	ripple voltage on V <sub>CC</sub> (peak-to-peak value)	f <sub>ripple</sub> = 20 kHz to 200 MHz	–	–	350	mV
I <sub>CC</sub>	card supply current	V <sub>CC</sub> = 0 to 5 V	–	–	80	mA
		V <sub>CC</sub> = 0 to 3 V	–	–	65	mA
<b>General</b>						
t <sub>de</sub>	deactivation time		50	80	100	μs
P <sub>tot</sub>	total power dissipation	continuous operation; T <sub>amb</sub> = –25 to +85 °C	–	–	0.56	W
T <sub>amb</sub>	ambient temperature		–25	–	+85	°C

**6 BLOCK DIAGRAM**

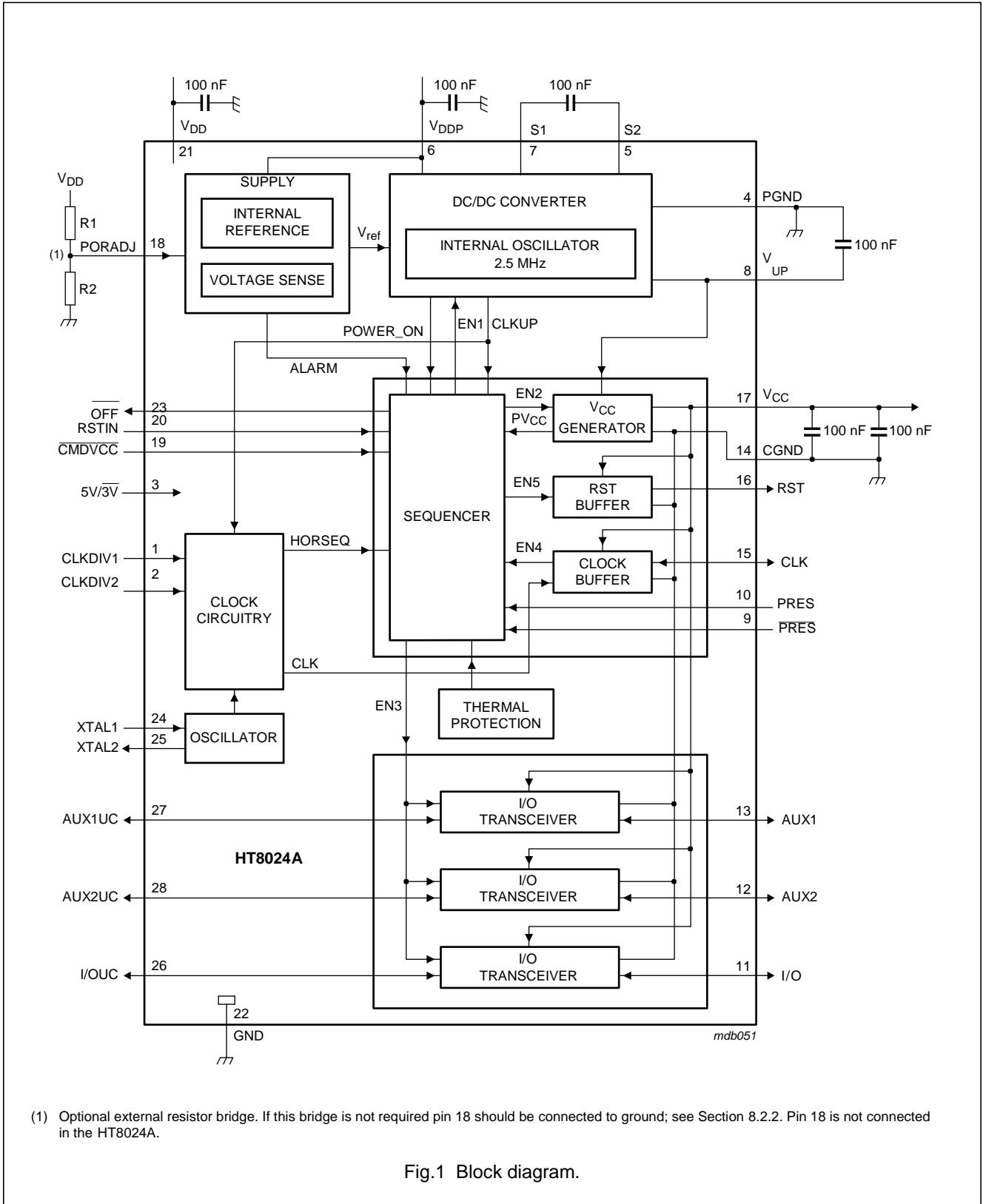


Fig.1 Block diagram.

**7 PINNING**

SYMBOL	PIN	TYPE	DESCRIPTION
CLKDIV1	1	I	CLK frequency selection input 1
CLKDIV2	2	I	CLK frequency selection input 2
5V/3V	3	I	card supply voltage selection input; $V_{CC} = 5\text{ V}$ (HIGH) or $V_{CC} = 3\text{ V}$ (LOW)
PGND	4	S	DC/DC converter power supply ground
S2	5	I/O	DC/DC converter capacitor; connected between pins S1 and S2; $C = 100\text{ nF}$ with $ESR < 100\text{ m}\Omega$
$V_{DDP}$	6	S	DC/DC converter power supply voltage
S1	7	I/O	DC/DC converter capacitor; connected between pins S1 and S2; $C = 100\text{ nF}$ with $ESR < 100\text{ m}\Omega$
$V_{UP}$	8	I/O	DC/DC converter output decoupling capacitor connection; $C = 100\text{ nF}$ with $ESR < 100\text{ m}\Omega$ must be connected between $V_{UP}$ and PGND
PRES	9	I	card presence contact input (active LOW); if PRES or PRES is active, the card is considered 'present' and a built-in debounce feature of 8 ms (typ.) is activated
PRES	10	I	card presence contact input (active HIGH); if PRES or PRES is active, the card is considered 'present' and a built-in debounce feature of 8 ms (typ.) is activated
I/O	11	I/O	data line to/from card reader contact C7; integrated 11 k $\Omega$ pull-up resistor to $V_{CC}$
AUX2	12	I/O	data line to/from card reader contact C8; integrated 11 k $\Omega$ pull-up resistor to $V_{CC}$
AUX1	13	I/O	data line to/from card reader contact C4; integrated 11 k $\Omega$ pull-up resistor to $V_{CC}$
CGND	14	S	card signal ground
CLK	15	I/O	card clock to/from card reader contact C3
RST	16	O	card reset output from card reader contact C2
$V_{CC}$	17	S	card supply voltage to card reader contact C1; decoupled to CGND via $2 \times 100\text{ nF}$ or $100 + 220\text{ nF}$ capacitors with $ESR < 100\text{ m}\Omega$ ; note 1
PORADJ	18	I	Power-on reset threshold adjustment input for changing the reset threshold with an external resistor bridge; doubles the width of the POR pulse when used; this pin is not connected for the HT8024A
CMDVCC	19	I	input from the host to start activation sequence (active LOW)
RSTIN	20	I	card reset input from the host
$V_{DD}$	21	S	supply voltage
GND	22	S	ground
OFF	23	O	NMOS interrupt output to the host (active LOW); 20 k $\Omega$ integrated pull-up resistor to $V_{DD}$
XTAL1	24	I	crystal connection or input for external clock
XTAL2	25	O	crystal connection (leave open-circuit if external clock source is used)
I/OUC	26	I/O	host data I/O line; integrated 11 k $\Omega$ pull-up resistor to $V_{DD}$
AUX1UC	27	I/O	auxiliary data line to/from the host; integrated 11 k $\Omega$ pull-up resistor to $V_{DD}$
AUX2UC	28	I/O	auxiliary data line to/from the host; integrated 11 k $\Omega$ pull-up resistor to $V_{DD}$

**Note**

1. The noise margin on  $V_{CC}$  will be higher with the 220 nF capacitor.

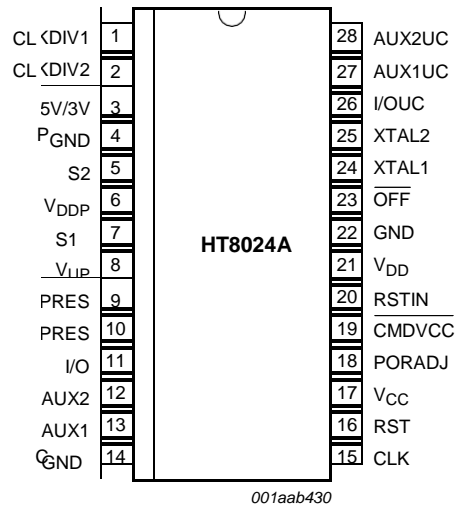


Fig.2 Pin configuration HT8024A.

## 8 FUNCTIONAL DESCRIPTION

Throughout this document it is assumed that the reader is familiar with ISO7816 terminology.

### 8.1 Power supply

The supply pins for the IC are  $V_{DD}$  and GND.  $V_{DD}$  should be in the range of 2.7 to 6.5 V. All signals interfacing with the system controller are referred to  $V_{DD}$ , therefore  $V_{DD}$  should also supply the system controller. All card reader contacts remain inactive during power-on or power-off.

The internal circuits are maintained in the reset state until  $V_{DD}$  reaches  $V_{th2} + V_{hys2}$  and for the duration of the internal Power-on reset pulse,  $t_w$  (see Fig.5). When  $V_{DD}$  falls below  $V_{th2}$ , an automatic deactivation of the contacts is performed.

A DC/DC converter is incorporated to generate the 5 or 3 V card supply voltage ( $V_{CC}$ ). The DC/DC converter should be supplied separately by  $V_{DDP}$  and PGND. Due to the possibility of large transient currents, the two 100 nF capacitors of the DC/DC converter should be located as near as possible to the IC and have an ESR less than 100 m $\Omega$ .

The DC/DC converter functions as a voltage doubler or a voltage follower according to the respective values of  $V_{CC}$  and  $V_{DDP}$  (both have thresholds with a hysteresis of 100 mV).

The DC/DC converter function changes as follows:

- $V_{CC} = 5$  V and  $V_{DDP} > 5.8$  V; voltage follower
- $V_{CC} = 5$  V and  $V_{DDP} < 5.7$  V; voltage doubler
- $V_{CC} = 3$  V and  $V_{DDP} > 4.1$  V; voltage follower
- $V_{CC} = 3$  V and  $V_{DDP} < 4.0$  V; voltage doubler.

Supply voltages  $V_{DD}$  and  $V_{DDP}$  may be applied to the IC in any sequence.

After powering the device,  $\overline{OFF}$  remains LOW until  $\overline{CMDVCC}$  is set HIGH.

During power off,  $\overline{OFF}$  falls LOW when  $V_{DD}$  is below the falling threshold voltage.

### 8.2 Voltage supervisor

#### 8.2.1 WITHOUT EXTERNAL DIVIDER ON PIN PORADJ (OR WITH HT8024A)

The voltage supervisor surveys the  $V_{DD}$  supply. A defined reset pulse of approximately 8 ms ( $t_w$ ) is used internally to keep the IC inactive during power-on or power-off of the  $V_{DD}$  supply (see Fig.5).

As long as  $V_{DD}$  is less than  $V_{th2} + V_{hys2}$ , the IC remains inactive whatever the levels on the command lines. This state also lasts for the duration of  $t_w$  after  $V_{DD}$  has reached a level higher than  $V_{th2} + V_{hys2}$ .

When  $V_{DD}$  falls below  $V_{th2}$ , a deactivation sequence of the contacts is performed.

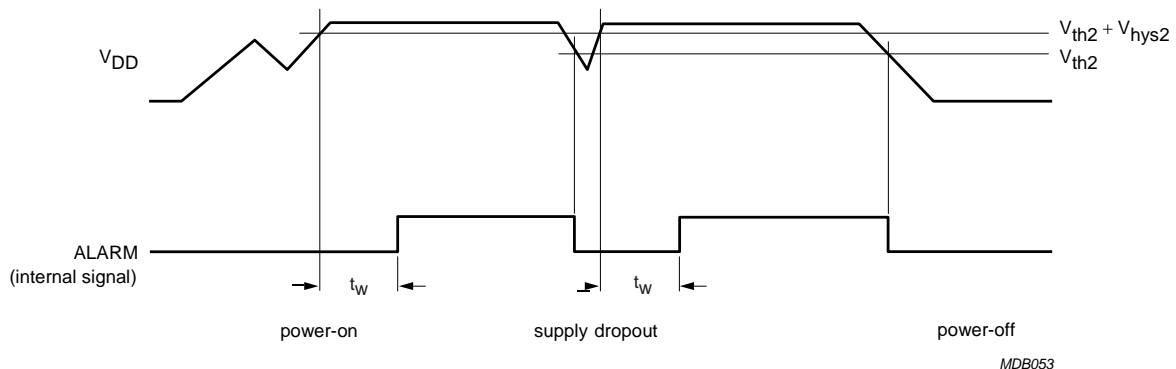


Fig.3 Voltage supervisor.

### 8.2.2 WITH AN EXTERNAL DIVIDER ON PIN PORADJ (NOT FOR THE HT8024A)

If an external resistor bridge is connected to pin PORADJ (R1 and R2 in Fig.1), then the following occurs:

- The internal threshold voltage  $V_{th2}$  is overridden by the external voltage and by the hysteresis, therefore:

$$V_{th2(ext)(rise)} = \left(1 + \frac{R1}{R2}\right) \times \left(V_{bridge} + \frac{V_{hys(ext)}}{2}\right)$$

$$V_{th2(ext)(fall)} = \left(1 + \frac{R1}{R2}\right) \times \left(V_{bridge} - \frac{V_{hys(ext)}}{2}\right)$$

where  $V_{bridge} = 1.25 \text{ V typ.}$  and  $V_{hys(ext)} = 60 \text{ mV typ.}$

- The reset pulse width  $t_W$  is doubled to approximately 16 ms.

Input PORADJ is biased internally with a pull-down current source of  $4 \mu\text{A}$  which is removed when the voltage on pin PORADJ exceeds 1 V. This ensures that after detection of the external bridge by the IC during power-on, the input current on pin PORADJ does not cause inaccuracy of the bridge voltage.

The minimum threshold voltage should be higher than 2 V.

The maximum threshold voltage may be up to  $V_{DD}$ .

### 8.2.3 APPLICATION EXAMPLES

The voltage supervisor is used as Power-on reset and as supply dropout detection during a card session.

Supply dropout detection is to ensure that a proper deactivation sequence is followed before the voltage is too low.

For the internal voltage supervisor to function, the system microcontroller should operate down to 2.35 V to ensure a proper deactivation sequence. If this is not possible, external resistor values can be chosen to overcome the problem.

#### 8.2.3.1 Microcontroller requiring a 3.3 V $\pm 20\%$ supply

For a microcontroller supplied by 3.3 V with a  $\pm 5\%$  regulator and with resistors R1, R2 having a  $\pm 1\%$  tolerance, the minimum supply voltage is 3.135 V.

$V_{PORADJ} = k \times V_{DD}$ , where  $k = \frac{S1}{S1 + S2}$  with S1 and S2

the actual values of nominal resistors R1 and R2.

This can be shown as

$$0.99 \times R1 < S1 < 1.01 \times R1 \text{ and}$$

$$0.99 \times R2 < S2 < 1.01 \times R2$$

Transposed, this becomes

$$1 + \left(\frac{0.98 \times R1}{R2}\right) = 1 + \left(\frac{0.99}{1.01}\right) \times \frac{R1}{R2} < \frac{1}{k}$$

$$1 < 1 + \left(\frac{1.01}{0.99}\right) \times \frac{R1}{R2} = 1 + \left(1.02 \times \frac{R1}{R2}\right)$$

If  $V1 = V_{th(ext)(rise)(max)}$  and  $V2 = V_{th(ext)(fall)(min)}$

activation will always be possible if  $V_{PORADJ} > V1$  and deactivation will always be done for  $V_{PORADJ} < V2$ .

Activation is always possible for  $V_{DD} > \frac{V1}{k}$

and deactivation is always possible for  $V_{DD} < \frac{V2}{k}$

That is  $V1 = 1.31 \text{ V}$  and  $V2 = 1.19 \text{ V}$

$$\text{and } \frac{R1}{R2} < \left(\frac{3.135 - 1}{1.31}\right) \times 0.98 = 1.365$$

Suppose  $R1 + R2 = 100 \text{ k}\Omega$ , then

$$R2 = \frac{100 \text{ k}\Omega}{2.365} = 42.3 \text{ k}\Omega \text{ and } R1 = 57.7 \text{ k}\Omega.$$

Deactivation will be effective at

$$V2 \times (1 + 1.02 \times 1.365) = 2.847 \text{ V in any case.}$$

If the microcontroller continues to function down to 2.80 V, the slew rate on  $V_{DD}$  should be less than 2 V/ms to ensure that clock CLK is correctly delivered to the card until time  $t_{12}$  (see Fig.9).

#### 8.2.3.2 Microcontroller requiring a 3.3 V $\pm 10\%$ supply

For a microcontroller supplied by a 3.3 V with a  $\pm 1\%$  regulator and with resistors R1, R2 having a  $\pm 0.1\%$  tolerance, the minimum supply voltage is 3.267 V.

The same calculations as in Section 8.2.3.1 conclude:

$$\frac{R1}{R2} < \left(\frac{3.267 - 1}{1.310}\right) \times 0.998 = 1.491$$

$$\text{Therefore } R2 = \frac{100 \text{ k}\Omega}{2.49} = 40.14 \text{ k}\Omega \text{ and } R1 = 59.86 \text{ k}\Omega.$$

Deactivation will be effective at

$$V2 \times (1 + 1.002 \times 1.491) = 2.967 \text{ V in any case.}$$

If the microcontroller continues to function down to 2.97 V, the slew rate on  $V_{DD}$  should be less than 0.20 V/ms to ensure that clock CLK is correctly delivered to the card until time  $t_{12}$  (see Fig.9).

### 8.3 Clock circuitry

The card clock signal (CLK) is derived from a clock signal input to pin XTAL1 or from a crystal operating at up to 26 MHz connected between pins XTAL1 and XTAL2.

The clock frequency can be  $f_{XTAL}$ ,  $\frac{1}{2} \times f_{XTAL}$ ,  $\frac{1}{4} \times f_{XTAL}$  or  $\frac{1}{8} \times f_{XTAL}$ . Frequency selection is made via inputs CLKDIV1 and CLKDIV2 (see Table 1).

**Table 1** Clock frequency selection; note 1

CLKDIV1	CLKDIV2	$f_{CLK}$
0	0	$\frac{f_{XTAL}}{8}$
0	1	$\frac{f_{XTAL}}{4}$
1	1	$\frac{f_{XTAL}}{2}$
1	0	$f_{XTAL}$

#### Note

1. The status of pins CLKDIV1 and CLKDIV2 must not be changed simultaneously; a delay of 10 ns minimum between changes is needed; the minimum duration of any state of CLK is eight periods of XTAL1.

The frequency change is synchronous, which means that during transition no pulse is shorter than 45% of the smallest period, and that the first and last clock pulses about the instant of change have the correct width.

When changing the frequency dynamically, the change is effective for only eight periods of XTAL1 after the command.

The duty factor of  $f_{XTAL}$  depends on the signal present at pin XTAL1.

In order to reach a 45 to 55% duty factor on pin CLK, the input signal on pin XTAL1 should have a duty factor of 48 to 52% and transition times of less than 5% of the input signal period.

If a crystal is used, the duty factor on pin CLK may be 45 to 55% depending on the circuit layout and on the crystal characteristics and frequency.

In other cases, the duty factor on pin CLK is guaranteed between 45 and 55% of the clock period.

The crystal oscillator runs as soon as the IC is powered up. If the crystal oscillator is used, or if the clock pulse on pin XTAL1 is permanent, the clock pulse is applied to the card as shown in the activation sequences shown in Figs 7 and 8.

If the signal applied to XTAL1 is controlled by the system microcontroller, the clock pulse will be applied to the card when it is sent by the system microcontroller (after completion of the activation sequence).

### 8.4 I/O transceivers

The three data lines I/O, AUX1 and AUX2 are identical.

The idle state is realized by both I/O and I/OUC lines being pulled HIGH via a 11 k $\Omega$  resistor (I/O to  $V_{CC}$  and I/OUC to  $V_{DD}$ ).

Pin I/O is referenced to  $V_{CC}$ , and pin I/OUC to  $V_{DD}$ , thus allowing operation when  $V_{CC}$  is not equal to  $V_{DD}$ .

The first side of the transceiver to receive a falling edge becomes the master. An anti-latch circuit disables the detection of falling edges on the line of the other side, which then becomes a slave.

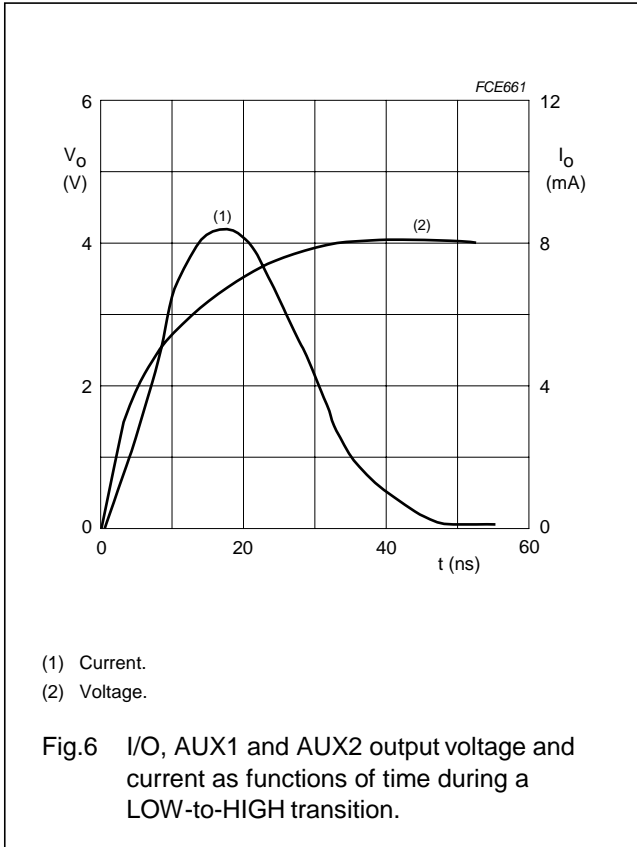
After a time delay  $t_{d(edge)}$ , an N transistor on the slave side is turned on, thus transmitting the logic 0 present on the master side.

When the master side returns to logic 1, a P transistor on the slave side is turned on during the time delay  $t_{pu}$  and then both sides return to their idle states.

This active pull-up feature ensures fast LOW-to-HIGH transitions; as shown in Fig.6, it is able to deliver more than 1 mA at an output voltage of up to  $0.9V_{CC}$  into an 80 pF load. At the end of the active pull-up pulse, the output voltage depends only on the internal pull-up resistor and the load current.

The current to and from the card I/O lines is limited internally to 15 mA and the maximum frequency on these lines is 1 MHz.





### 8.5 Inactive mode

After a Power-on reset, the circuit enters the inactive mode. A minimum number of circuits are active while waiting for the microcontroller to start a session:

- All card contacts are inactive (approximately 200  $\Omega$  to GND)
- Pins I/OUC, AUX1UC and AUX2UC are in the high-impedance state (11 k $\Omega$  pull-up resistor to  $V_{DD}$ )
- Voltage generators are stopped
- XTAL oscillator is running
- Voltage supervisor is active
- The internal oscillator is running at its low frequency.

### 8.6 Activation sequence

After power-on and after the internal pulse width delay, the system microcontroller can check the presence of a card using the signals  $\overline{\text{OFF}}$  and  $\overline{\text{CMDVCC}}$  as shown in Table 2.

**Table 2** Card presence indication

$\overline{\text{OFF}}$	$\overline{\text{CMDVCC}}$	INDICATION
HIGH	HIGH	card present
LOW	HIGH	card not present

If the card is in the reader (this is the case if  $\overline{\text{PRES}}$  or  $\overline{\text{PRES}}$  is active), the system microcontroller can start a card session by pulling  $\overline{\text{CMDVCC}}$  LOW. The following sequence then occurs (see Fig.6):

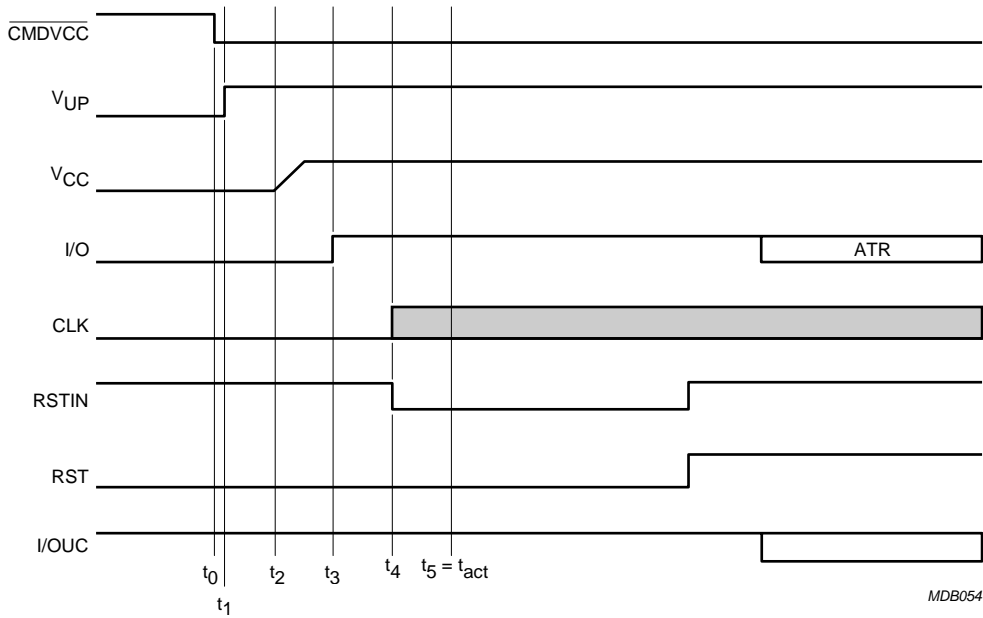
1.  $\overline{\text{CMDVCC}}$  is pulled LOW and the internal oscillator changes to its high frequency ( $t_0$ ).
2. The voltage doubler is started (between  $t_0$  and  $t_1$ ).
3.  $V_{CC}$  rises from 0 to 5 V (or 3 V) with a controlled slope ( $t_2 = t_1 + 1.5 \times T$ ) where T is 64 times the period of the internal oscillator (approximately 25  $\mu\text{s}$ ).
4. I/O, AUX1 and AUX2 are enabled ( $t_3 = t_1 + 4T$ ) (these were pulled LOW until this moment).
5. CLK is applied to the C3 contact of the card reader ( $t_4$ ).
6. RST is enabled ( $t_5 = t_1 + 7T$ ).

The clock may be applied to the card using the following sequence:

1. Set  $\overline{\text{RSTIN}}$  HIGH.
2. Set  $\overline{\text{CMDVCC}}$  LOW.
3. Reset  $\overline{\text{RSTIN}}$  LOW between  $t_3$  and  $t_5$ ; CLK will start at this moment.
4. RST remains LOW until  $t_5$ , when RST is enabled to be the copy of  $\overline{\text{RSTIN}}$ .
5. After  $t_5$ ,  $\overline{\text{RSTIN}}$  has no further affect on CLK; this allows a precise count of CLK pulses before toggling RST.

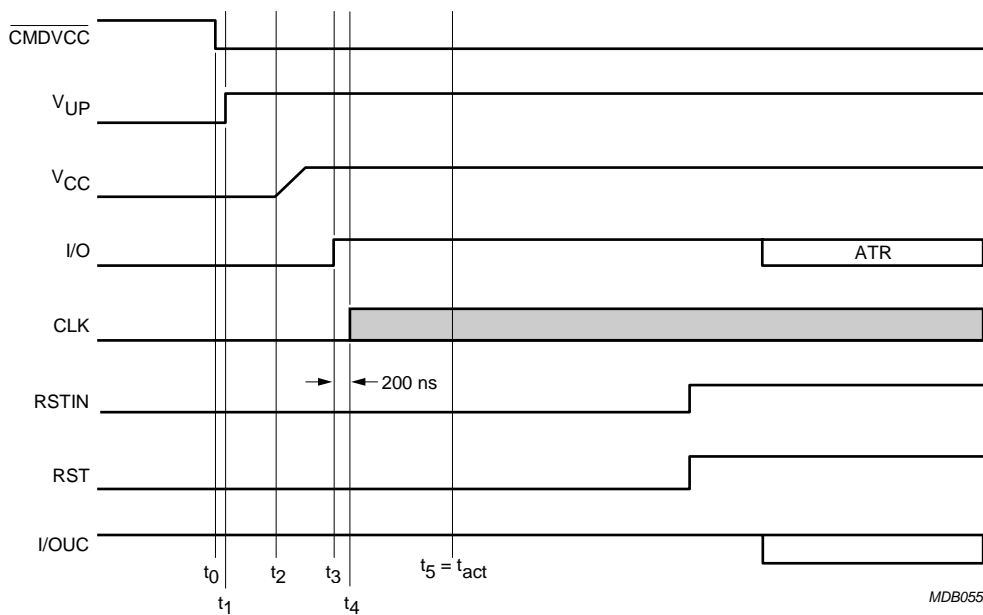
If the applied clock is not needed, then  $\overline{\text{CMDVCC}}$  may be set LOW with  $\overline{\text{RSTIN}}$  LOW. In this case, CLK will start at  $t_3$  (minimum 200 ns after the transition on I/O), and after  $t_5$ ,  $\overline{\text{RSTIN}}$  may be set HIGH in order to obtain an Answer To Request (ATR) from the card.

Activation should not be performed with  $\overline{\text{RSTIN}}$  held permanently HIGH.



MDB054

Fig.7 Activation sequence using RSTIN and  $\overline{\text{CMDVCC}}$ .



MDB055

Fig.8 Activation sequence at  $t_3$ .

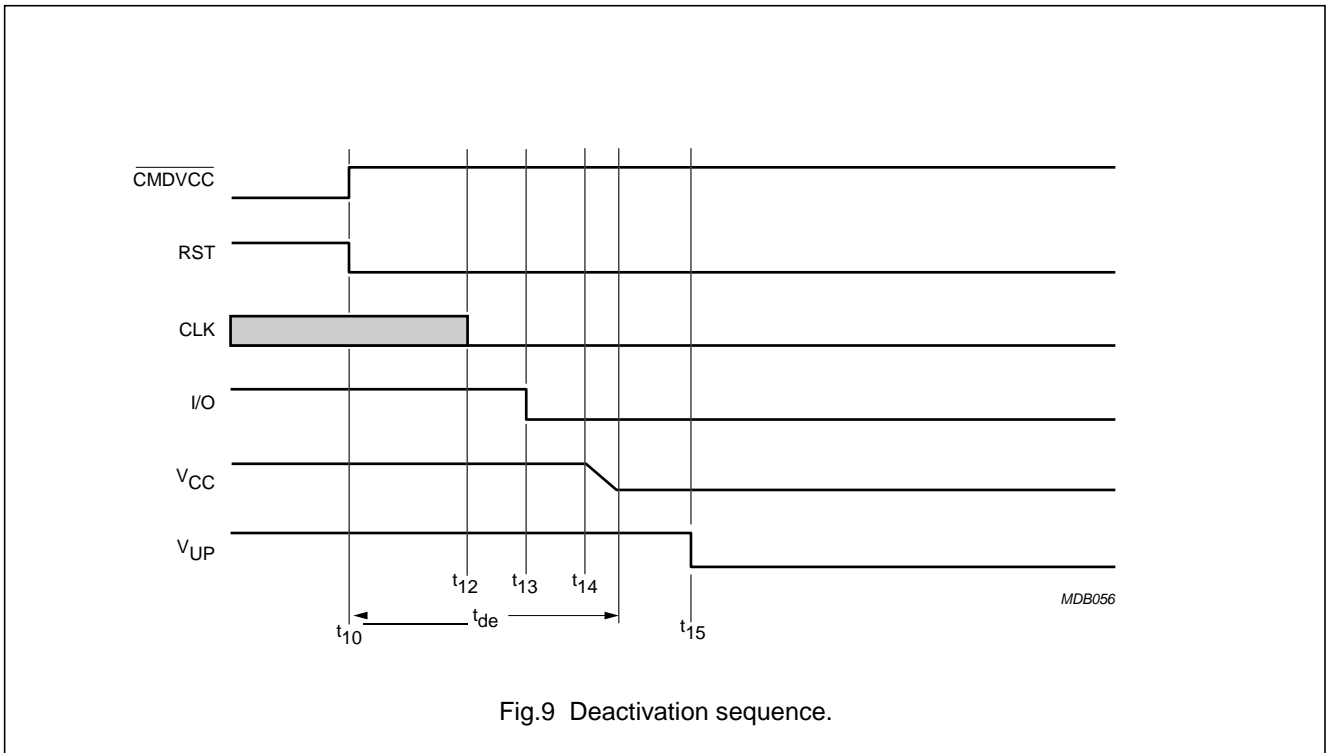
### 8.7 Active mode

When the activation sequence is completed, the HT8024A will be in its active mode. Data is exchanged between the card and the microcontroller via the I/O lines. The HT8024A is designed for cards without  $V_{PP}$  (the voltage required to program or erase the internal non-volatile memory).

### 8.8 Deactivation sequence

When a session is completed, the microcontroller sets the  $\overline{\text{CMDVCC}}$  line HIGH. The circuit then executes an automatic deactivation sequence by counting the sequencer back and finishing in the inactive mode (see Fig.9):

1. RST goes LOW ( $t_{10}$ ).
2. CLK is held LOW ( $t_{12} = t_{10} + 0.5 \times T$ ) where T is 64 times the period of the internal oscillator (approximately 25  $\mu\text{s}$ ).
3. I/O, AUX1 and AUX2 are pulled LOW ( $t_{13} = t_{10} + T$ ).
4.  $V_{CC}$  starts to fall towards zero ( $t_{14} = t_{10} + 1.5 \times T$ ).
5. The deactivation sequence is complete at  $t_{de}$ , when  $V_{CC}$  reaches its inactive state.
6.  $V_{UP}$  falls to zero ( $t_{15} = t_{10} + 5T$ ) and all card contacts become low-impedance to GND; I/OUC, AUX1UC and AUX2UC remain at  $V_{DD}$  (pulled-up via a 11  $k\Omega$  resistor).
7. The internal oscillator returns to its lower frequency.



### 8.9 V<sub>CC</sub> generator

The V<sub>CC</sub> generator has a capacity to supply up to 80 mA continuously at 5 V and 65 mA at 3 V.

An internal overload detector operates at approximately 120 mA. Current samples to the detector are internally filtered, allowing spurious current pulses up to 200 mA with a duration in the order of μs to be drawn by the card without causing deactivation. The average current must stay below the specified maximum current value.

For reasons of V<sub>CC</sub> voltage accuracy, a 100 nF capacitor with an ESR < 100 mΩ should be tied to CGND near to pin V<sub>CC</sub>, and a 100 or 220 nF capacitor (220 nF is the best choice) with the same ESR should be tied to CGND near card reader contact C1.

### 8.10 Fault detection

The following fault conditions are monitored:

- Short-circuit or high current on V<sub>CC</sub>
- Removal of a card during a transaction
- V<sub>DD</sub> drooping
- DC/DC converter operating out of the specified values (V<sub>DDP</sub> too low or current from V<sub>UP</sub> too high)
- Overheating.

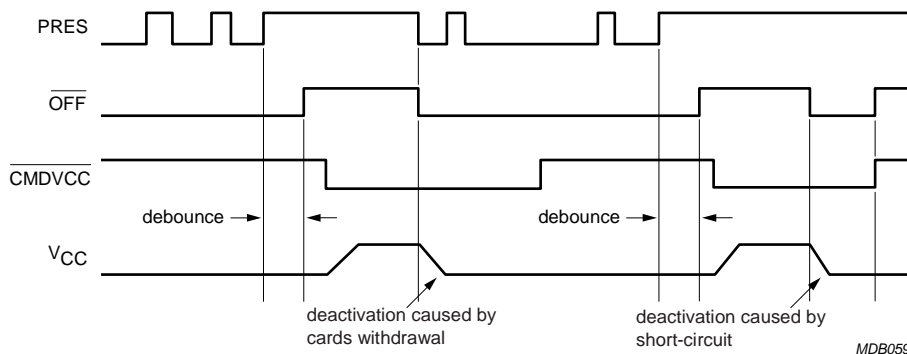
There are two different cases (see Fig.10):

- **CMDVCC HIGH outside a card session.** Output  $\overline{\text{OFF}}$  is LOW if a card is not in the card reader, and HIGH if a card is in the reader. A voltage drop on the V<sub>DD</sub> supply is detected by the supply supervisor, this generates an internal Power-on reset pulse but does not act upon  $\overline{\text{OFF}}$ . No short-circuit or overheating is detected because the card is not powered-up.
- **CMDVCC LOW within a card session.** Output  $\overline{\text{OFF}}$  goes LOW when a fault condition is detected. As soon as this occurs, an emergency deactivation is performed automatically (see Fig.11). When the system controller resets  $\overline{\text{CMDVCC}}$  to HIGH it may sense the  $\overline{\text{OFF}}$  level again after completing the deactivation sequence. This distinguishes between a hardware problem or a card extraction ( $\overline{\text{OFF}}$  goes HIGH again if a card is present).

Depending on the type of card-present switch within the connector (normally-closed or normally-open) and on the mechanical characteristics of the switch, bouncing may occur on the PRES signals at card insertion or withdrawal.

There is a debounce feature in the device with an 8 ms typical duration (see Fig.10). When a card is inserted, output  $\overline{\text{OFF}}$  goes HIGH only at the end of the debounce time.

When the card is extracted, an automatic deactivation sequence of the card is performed on the first true/false transition on PRES or  $\overline{\text{PRES}}$  and output  $\overline{\text{OFF}}$  goes LOW.



See "Application note AN10141" for software decision algorithm on  $\overline{\text{OFF}}$  signal.

Fig.10 Behaviour of  $\overline{\text{OFF}}$ ,  $\overline{\text{CMDVCC}}$ , PRES and V<sub>CC</sub>.

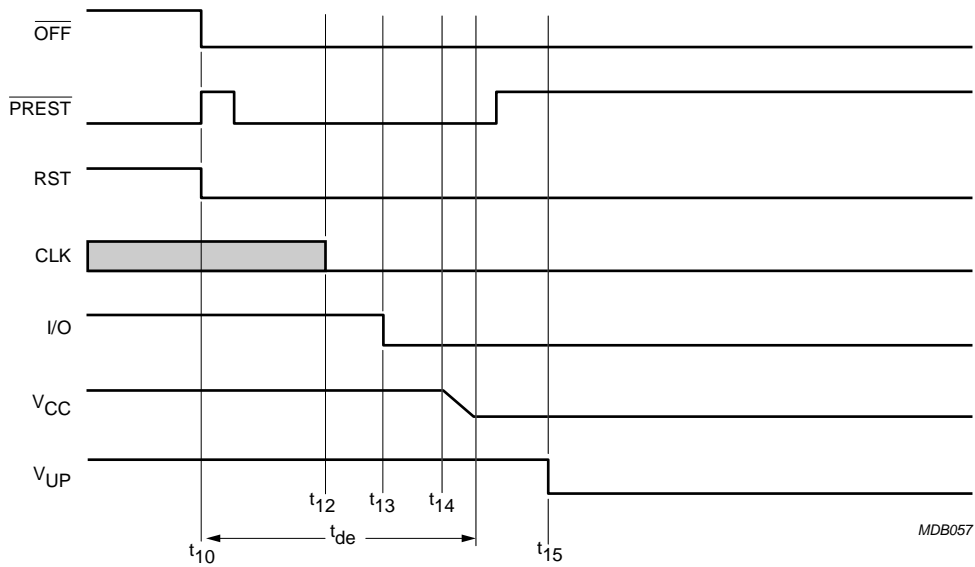


Fig.11 Emergency deactivation sequence (card extraction).

**9 LIMITING VALUES**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DD</sub>	supply voltage		-0.3	+6.5	V
V <sub>DDP</sub>	DC/DC converter supply voltage		-0.3	+6.5	V
V <sub>i</sub> , V <sub>O</sub>	voltage on input and output pins	pins XTAL1, XTAL2, 5V/3V, RSTIN, AUX1UC, AUX2UC, I/OUC, CLKDIV1, CLKDIV2, CMDVCC, OFF and PORADJ	-0.3	+6.5	V
V <sub>card</sub>	voltage on card pins	pins PRES, PRES, I/O, RST, AUX1, AUX2 and CLK	-0.3	+6.5	V
V <sub>n</sub>	voltage on other pins	pins V <sub>UP</sub> , S1 and S2	-0.3	+6.5	V
T <sub>j(max)</sub>	maximum junction temperature		-	150	°C
T <sub>stg</sub>	storage temperature		-55	+150	°C
V <sub>esd</sub>	electrostatic discharge voltage	card contacts in typical application; notes 1 and 2 pins I/O, RST, V <sub>CC</sub> , AUX1, AUX2, CLK, PRES and PRES	-6	+6	kV
		all pins; note 1 human body model; notes 2 and 3 machine model; note 4	-2 -200	+2 +200	kV V

**Notes**

- All card contacts are protected against any short-circuit with any other card contact.
- Every pin withstands the ESD test according to MIL-STD-883C class 3 for card contacts, class 2 for the remaining. Method 3015 (HBM; 1500 Ω and 100 pF) 3 pulses positive and 3 pulses negative on each pin referenced to ground.
- In accordance with EIA/JESD22-A114-B, June 2000.
- In accordance with EIA/JESD22-A115-A, October 1997.

**10 HANDLING**

Inputs and outputs are protected against electrostatic discharge in normal handling. However it is good practice to take normal precautions appropriate to handling MOS devices (see "Handling MOS devices").

**11 THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient HT8024A	in free air	70	K/W

**12 CHARACTERISTICS**

$V_{DD} = 3.3\text{ V}$ ;  $V_{DDP} = 5\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $f_{XTAL} = 10\text{ MHz}$ ; all currents flowing into the IC are positive; see note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP	MAX.	UNIT
<b>Temperature</b>						
$T_{amb}$	ambient temperature		-25	-	+85	°C
<b>Supplies</b>						
$V_{DD}$	supply voltage		2.7	-	6.5	V
$V_{DDP}$	DC/DC converter supply voltage	$V_{CC} = 5\text{ V}$ ; $ I_{CC}  < 80\text{ mA}$	4.0	5.0	6.5	V
		$V_{CC} = 5\text{ V}$ ; $ I_{CC}  < 20\text{ mA}$	3.0	-	6.5	V
$I_{DD}$	supply current	card inactive	-	-	1.2	mA
		card active; $f_{CLK} = f_{XTAL}$ ; $C_L = 30\text{ pF}$	-	-	1.5	mA
$I_{DDP}$	DC/DC converter supply current	inactive mode	-	-	0.1	mA
		active mode; $f_{CLK} = f_{XTAL}$ ; $C_L = 30\text{ pF}$ ; $ I_{CC}  = 0$	-	-	10	mA
		$V_{CC} = 5\text{ V}$ ; $ I_{CC}  = 80\text{ mA}$	-	-	200	mA
		$V_{CC} = 3\text{ V}$ ; $ I_{CC}  = 65\text{ mA}$	-	-	100	mA
$V_{th2}$	falling threshold voltage on $V_{DD}$	no external resistors at pin PORADJ; $V_{DD}$ level falling	2.35	2.45	2.55	V
$V_{hys2}$	hysteresis of threshold voltage $V_{th2}$	no external resistors at pin PORADJ	50	100	150	mV
<b>Pin PORADJ; note 2</b>						
$V_{th(ext)(rise)}$	external rising threshold voltage on $V_{DD}$	external resistor bridge at pin PORADJ; $V_{DD}$ level rising	1.240	1.28	1.310	V
$V_{th(ext)(fall)}$	external falling threshold voltage on $V_{DD}$	external resistor bridge at pin PORADJ; $V_{DD}$ level falling	1.190	1.22	1.26	V
$V_{hys(ext)}$	hysteresis of threshold voltage $V_{th(ext)}$	external resistor bridge at pin PORADJ	30	60	90	mV
$\Delta V_{hys(ext)}$	hysteresis of threshold voltage $V_{th(ext)}$ variation with temperature	external resistor bridge at pin PORADJ	-	-	0.25	mV/K
$t_w$	width of internal Power-on reset pulse	no external resistors at pin PORADJ	4	8	12	ms
		external resistor bridge at pin PORADJ	8	16	24	ms
$I_L(PORADJ)$	leakage current on pin PORADJ	$V_{PORADJ} < 0.5\text{ V}$	-0.1	4	10	μA
		$V_{PORADJ} > 1\text{ V}$	-1	-	+1	μA
$P_{tot}$	total power dissipation	continuous operation; $T_{amb} = -25\text{ to }+85\text{ °C}$	-	-	0.56	W

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP	MAX.	UNIT
<b>DC/DC converter</b>						
$f_{CLK}$	clock frequency	card active	2.2	–	3.2	MHz
$V_{th(vd-vf)}$	threshold voltage for voltage doubler to change to voltage follower	5 V card	5.2	5.8	6.2	V
		3 V card	3.8	4.1	4.4	V
$V_{UP(av)}$	output voltage on pin $V_{UP}$ (average value)	$V_{CC} = 5\text{ V}$	5.2	5.7	6.2	V
		$V_{CC} = 3\text{ V}; V_{DDP} = 3.3\text{ V}$	3.5	3.9	4.3	V
<b>Card supply voltage (pin <math>V_{CC}</math>); note 3</b>						
$C_{VCC}$	external capacitance on pin $V_{CC}$	note 4	80	–	400	nF
$V_{CC}$	card supply voltage (including ripple voltage)	5 V card				
		card inactive; $ I_{CC}  = 0\text{ mA}$	–0.1	0	+0.1	V
		card inactive; $ I_{CC}  = 1\text{ mA}$	–0.1	0	+0.3	V
		card active; $ I_{CC}  < 80\text{ mA}$	4.75	5.0	5.25	V
		card active; single current pulse, $I_p = -100\text{ mA}$ , $t_p = 2\text{ ms}$	4.65	5.0	5.25	V
		card active; current pulses, $I_p = 40\text{ nAs}$	4.65	5.0	5.25	V
		card active; current pulses, $I_p = 40\text{ nAs}$ with $ I_{CC}  < 200\text{ mA}$ , $t_p < 400\text{ ns}$	4.65	5.0	5.25	V
		3 V card				
		card inactive; $ I_{CC}  = 0\text{ mA}$	–0.1	0	+0.1	V
		card inactive; $ I_{CC}  = 1\text{ mA}$	–0.1	0	+0.3	V
		card active; $ I_{CC}  < 65\text{ mA}$	2.85	3.0	3.15	V
		card active; single current pulse $I_p = -100\text{ mA}$ ; $t_p = 2\text{ ms}$	2.76	3.0	3.20	V
		card active; current pulses, $I_p = 40\text{ nAs}$	2.76	3.0	3.20	V
		card active; current pulses, $I_p = 40\text{ nAs}$ with $ I_{CC}  < 200\text{ mA}$ , $t_p < 400\text{ ns}$	2.76	3.0	3.20	V
$V_{CC(ripple)(p-p)}$	ripple voltage on $V_{CC}$ (peak to peak value)	$f_{ripple} = 20\text{ kHz to } 200\text{ MHz}$	–	–	350	mV
$ I_{CC} $	card supply current	$V_{CC} = 0\text{ to } 5\text{ V}$	–	–	80	mA
		$V_{CC} = 0\text{ to } 3\text{ V}$	–	–	65	mA
		$V_{CC}$ short-circuit to GND	100	120	150	mA
SR	slew rate	slew up or down	0.08	0.15	0.22	V/ $\mu$ s



SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP	MAX.	UNIT
<b>Crystal oscillator (pins XTAL1 and XTAL2)</b>						
C <sub>XTAL1</sub> , C <sub>XTAL2</sub>	external capacitance on pins XTAL1 and XTAL2	depends on type of crystal or resonator used	–	–	15	pF
f <sub>XTAL</sub>	crystal frequency		2	–	26	MHz
f <sub>XTAL1</sub>	frequency applied on pin XTAL1		0	–	26	MHz
V <sub>IL</sub>	LOW-level input voltage on pin XTAL1		–0.3	–	+0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage on pin XTAL1		0.7V <sub>DD</sub>	–	V <sub>DD</sub> + 0.3	V
<b>Data lines (pins I/O, I/OUC, AUX1, AUX2, AUX1UC and AUX2UC)</b>						
t <sub>d(I/O-I/OUC)</sub> , t <sub>d(I/OUC-I/O)</sub>	I/O to I/OUC, I/OUC to I/O falling edge delay		–	–	200	ns
t <sub>pu</sub>	active pull-up pulse width		–	–	100	ns
f <sub>I/O(max)</sub>	maximum frequency on data lines		–	–	1	MHz
C <sub>i</sub>	input capacitance on data lines		–	–	10	pF
<b>Data lines to card reader (pins I/O, AUX1 and AUX2; with integrated 11 kΩ pull-up resistors to V<sub>CC</sub>)</b>						
V <sub>o(inactive)</sub>	output voltage	inactive mode no load I <sub>o(inactive)</sub> = 1 mA	0 –	– –	0.1 0.3	V V
I <sub>o(inactive)</sub>	output current	inactive mode; pin grounded	–	–	–1	mA
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 1 mA I <sub>OL</sub> ≥ 15 mA	0 V <sub>CC</sub> – 0.4	– –	0.3 V <sub>CC</sub>	V V
V <sub>OH</sub>	HIGH-level output voltage	no DC load 5 and 3 V cards; I <sub>OH</sub> < –40 μA  I <sub>OH</sub>   ≥ 10 mA	0.9V <sub>CC</sub> 0.75V <sub>CC</sub> 0	– – –	V <sub>CC</sub> + 0.1 V <sub>CC</sub> + 0.1 0.4	V V V
V <sub>IL</sub>	LOW-level input voltage		0.3	–	0.8	V
V <sub>IH</sub>	HIGH-level input voltage		1.5	–	V <sub>CC</sub> + 0.3	V
I <sub>IL</sub>	LOW-level input current	V <sub>IL</sub> = 0V	–	–	600	μA
I <sub>LIH</sub>	HIGH-level input leakage current	V <sub>IH</sub> = V <sub>CC</sub>	–	–	10	μA
t <sub>t(DI)</sub>	data input transition time	V <sub>IL(max)</sub> to V <sub>IH(min)</sub>	–	–	1.2	μs
t <sub>t(DO)</sub>	data output transition time	V <sub>o</sub> = 0 to V <sub>CC</sub> ; C <sub>L</sub> ≤ 80 pF; 10% to 90%	–	–	0.1	μs
R <sub>pu</sub>	integrated pull-up resistor	pull-up resistor to V <sub>CC</sub>	9	11	13	kΩ
I <sub>pu</sub>	current when pull-up active	V <sub>OH</sub> = 0.9V <sub>CC</sub> ; C = 80 pF	–1	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP	MAX.	UNIT
<b>Data lines to microcontroller (pins I/OU, AUX1UC and AUX2UC; with integrated 11 kΩ pull-up resistors to V<sub>DD</sub>)</b>						
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 1 mA	0	–	0.3	V
V <sub>OH</sub>	HIGH-level output voltage	no DC load	0.9V <sub>DD</sub>	–	V <sub>DD</sub> + 0.1	V
		5 and 3 V cards; I <sub>OH</sub> < –40 μA	0.75V <sub>DD</sub>	–	V <sub>DD</sub> + 0.1	V
V <sub>IL</sub>	LOW-level input voltage		–0.3	–	+0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	–	V <sub>DD</sub> + 0.3	V
I <sub>LIH</sub>	HIGH-level input leakage current	V <sub>IH</sub> = V <sub>DD</sub>	–	–	10	μA
I <sub>L</sub>	LOW-level input current	V <sub>IL</sub> = 0V	–	–	600	μA
R <sub>pu</sub>	integrated pull-up resistor	pull-up resistor to V <sub>CC</sub>	9	11	13	kΩ
t <sub>t(DI)</sub>	data input transition time	V <sub>IL(max)</sub> to V <sub>IH(min)</sub>	–	–	1.2	μs
t <sub>t(DO)</sub>	data output transition time	V <sub>o</sub> = 0 to V <sub>DD</sub> ; C <sub>L</sub> < 30 pF; 10% to 90%	–	–	0.1	μs
I <sub>pu</sub>	current when pull-up active	V <sub>OH</sub> = 0.9V <sub>DD</sub> ; C = 30 pF	–1	–	–	mA
<b>Internal oscillator</b>						
f <sub>OSC(int)</sub>	frequency of internal oscillator	inactive mode	55	140	200	kHz
		active mode	2.2	2.7	3.2	MHz
<b>Reset output to card reader (pin RST)</b>						
V <sub>o(inactive)</sub>	output voltage	inactive mode				
		no load	0	–	0.1	V
		I <sub>o(inactive)</sub> = 1 mA	0	–	0.3	V
I <sub>o(inactive)</sub>	output current	inactive mode; pin grounded	0	–	–1	mA
t <sub>d(RSTIN-RST)</sub>	RSTIN to RST delay	RST enabled	–	–	2	μs
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 200 μA	0	–	0.2	V
		I <sub>OL</sub> = 20 mA (current limit)	V <sub>CC</sub> – 0.4	–	V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = –200 μA	0.9V <sub>CC</sub>	–	V <sub>CC</sub>	V
		I <sub>OH</sub> = –20 mA (current limit)	0	–	0.4	V
t <sub>r</sub>	rise time	C <sub>L</sub> = 100 pF; V <sub>CC</sub> = 5 or 3V	–	–	0.1	μs
t <sub>f</sub>	fall time	C <sub>L</sub> = 100 pF; V <sub>CC</sub> = 5 or 3V	–	–	0.1	μs
<b>Clock output to card reader (pin CLK)</b>						
V <sub>o(inactive)</sub>	output voltage	inactive mode				
		no load	0	–	0.1	V
		I <sub>o(inactive)</sub> = 1 mA	0	–	0.3	V
I <sub>o(inactive)</sub>	output current	CLK inactive; pin grounded	0	–	–1	mA
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 200 μA	0	–	0.3	V
		I <sub>OL</sub> = 70 mA (current limit)	V <sub>CC</sub> – 0.4	–	V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = –200 μA	0.9V <sub>CC</sub>	–	V <sub>CC</sub>	V
		I <sub>OH</sub> = –70 mA (current limit)	0	–	0.4	V
t <sub>r</sub>	rise time	C <sub>L</sub> = 30 pF; note 5	–	–	16	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP	MAX.	UNIT
$t_f$	fall time	$C_L = 30 \text{ pF}$ ; note 5	–	–	16	ns
$\delta$	duty factor (except for $f_{XTAL}$ )	$C_L = 30 \text{ pF}$ ; note 5	45	–	55	%
SR	slew rate	slew up or down; $C_L = 30 \text{ pF}$	0.2	–	–	V/ns
<b>Control inputs (pins CLKDIV1, CLKDIV2, CMDVCC, RSTIN and 5V/3V); note 6</b>						
$V_{IL}$	LOW-level input voltage		–0.3	–	+0.3 $V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		0.7 $V_{DD}$	–	$V_{DD} + 0.3$	V
$ I_{LIL} $	LOW-level input leakage current	$0 < V_{IL} < V_{DD}$	–	–	1	$\mu\text{A}$
$ I_{LIH} $	HIGH-level input leakage current	$0 < V_{IH} < V_{DD}$	–	–	1	$\mu\text{A}$
<b>Card presence inputs (pins PRES and PRES); note 7</b>						
$V_{IL}$	LOW-level input voltage		–0.3	–	+0.3 $V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		0.7 $V_{DD}$	–	$V_{DD} + 0.3$	V
$ I_{LIL} $	LOW-level input leakage current	$0 < V_{IL} < V_{DD}$	–	–	5	$\mu\text{A}$
$ I_{LIH} $	HIGH-level input leakage current	$0 < V_{IH} < V_{DD}$	–	–	5	$\mu\text{A}$
<b>Interrupt output (pin OFF; NMOS drain with integrated 20 k<math>\Omega</math> pull-up resistor to <math>V_{DD}</math>)</b>						
$V_{OL}$	LOW-level output voltage	$I_{OL} = 2 \text{ mA}$	0	–	0.3	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -15 \mu\text{A}$	0.75 $V_{DD}$	–	–	V
$R_{pu}$	integrated pull-up resistor	20 k $\Omega$ pull-up resistor to $V_{DD}$	16	20	24	k $\Omega$
<b>Protection and limitation</b>						
$ I_{CC(sd)} $	shutdown and limitation current pin $V_{CC}$		–	130	150	mA
$I_{I/O(lim)}$	limitation current pins I/O, AUX1 and AUX2		–15	–	+15	mA
$I_{CLK(lim)}$	limitation current pin CLK		–70	–	+70	mA
$I_{RST(lim)}$	limitation current pin RST		–20	–	+20	mA
$T_{sd}$	shut-down temperature		–	150	–	$^{\circ}\text{C}$
<b>Timing</b>						
$t_{act}$	activation time	see Fig.7	50	–	220	$\mu\text{s}$
$t_{de}$	deactivation time	see Fig.8	50	80	100	$\mu\text{s}$
$t_3$	start of the window for sending CLK to the card	see Fig.7	50	–	130	$\mu\text{s}$
$t_5$	end of the window for sending CLK to the card	see Fig.7	140	–	220	$\mu\text{s}$
$t_{debounce}$	debounce time pins PRES and PRES	see Fig.10	5	8	11	ms

**Notes**

- All parameters remain within limits but are tested only statistically for the temperature range. When a parameter is specified as a function of  $V_{DD}$  or  $V_{CC}$  it means their actual value at the moment of measurement.
- If no external bridge is used then, to avoid any disturbance, it is recommended to connect pin 18 to ground. Pin 18 is not connected in the HT8024A
- To meet these specifications, pin  $V_{CC}$  should be decoupled to CGND using two ceramic multilayer capacitors of low ESR both with values of 100 nF, or one 100 nF and one 220 nF (see Fig.13).
- Permitted capacitor values are 100, or 100 + 100, or 220, or 220 + 100, or 330 nF.
- Transition time and duty factor definitions are shown in Fig.12;  $\delta = \frac{t_1}{t_1 + t_2}$
- Pin  $\overline{CMDVCC}$  is active LOW; pin RSTIN is active HIGH; for CLKDIV1 and CLKDIV2 functions see Table 1.
- Pin  $\overline{PRES}$  is active LOW; pin PRES is active HIGH; PRES has an integrated 1.25  $\mu A$  current source to GND (PRES to  $V_{DD}$ ); the card is considered present if at least one of the inputs  $\overline{PRES}$  or PRES is active.

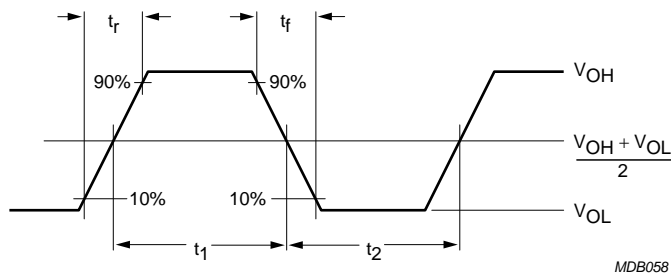


Fig.12 Definition of output and input transition times.

**13 APPLICATION INFORMATION**

Performance can be affected by the layout of the application. For example, an additional cross-capacitance of 1 pF between card reader contacts C2 and C3 or C2 and C7 can cause contact C2 to be polluted with high frequency noise from C3 (or C7). In this case, include a 100 pF capacitor between contacts C2 and CGND.

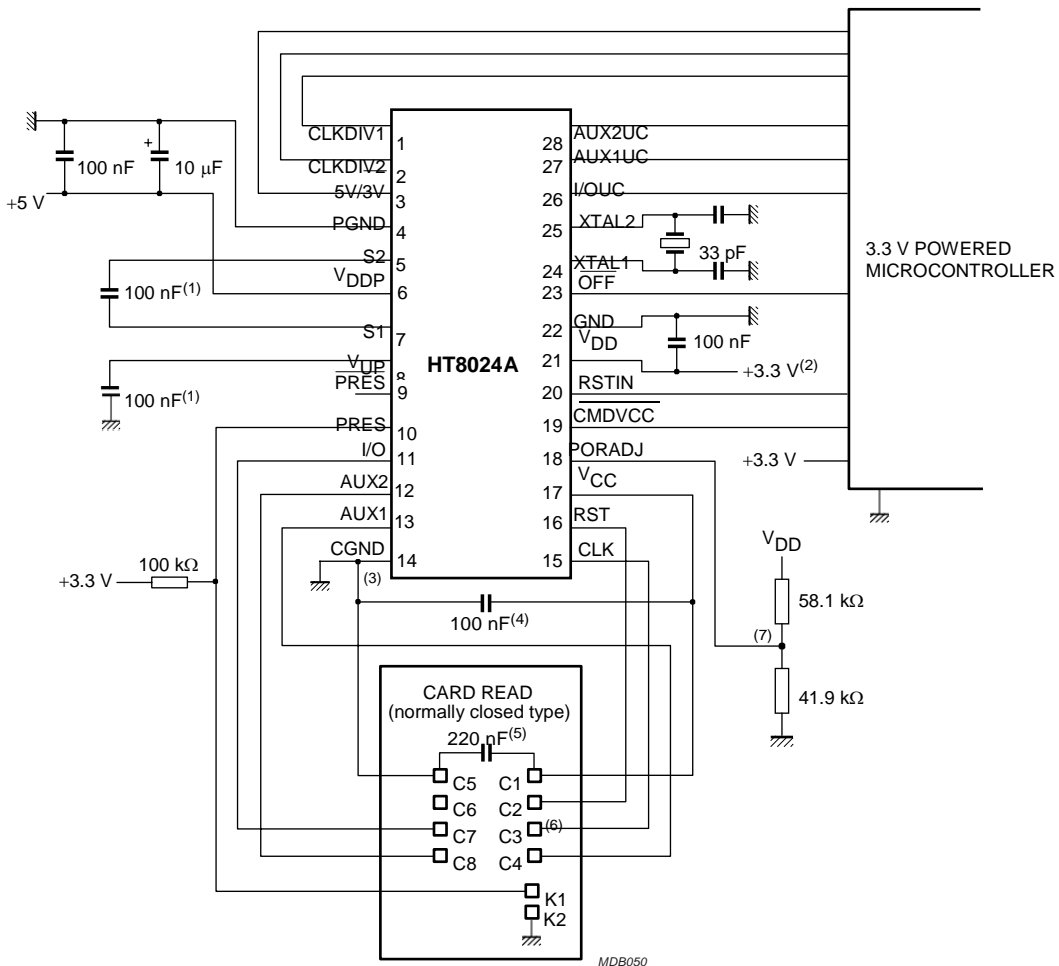
Application recommendations:

- Ensure there is ample ground area around the HT8024A and the connector; place the HT8024A very near to the connector; decouple the  $V_{DD}$  and  $V_{DDP}$  lines (these lines are best positioned under the connector)
- The HT8024A and the microcontroller must use the same  $V_{DD}$  supply. Pins CLKDIV1, CLKDIV2, RSTIN, PRES,  $\overline{PRES}$ , AUX1UC, I/OUC, AUX2UC, 5V/3V,  $\overline{CMDVCC}$ , and OFF are referred to  $V_{DD}$ ; if pin XTAL1 is to be driven by an external clock, also refer this pin to  $V_{DD}$

- Track C3 should be placed as far as possible from the other tracks
- The track connecting CGND to C5 should be straight (the two capacitors on C1 should be connected to this ground track)
- Avoid ground loops between CGND, PGND and GND
- Decouple  $V_{DDP}$  and  $V_{DD}$  separately; if the two supplies are the same in the application, then they should be connected in star on the main track.

With all these layout precautions, noise should be kept to an acceptable level and jitter on C3 should be less than 100 ps.

Reference layouts are provided in "Application note 10141", available on request.

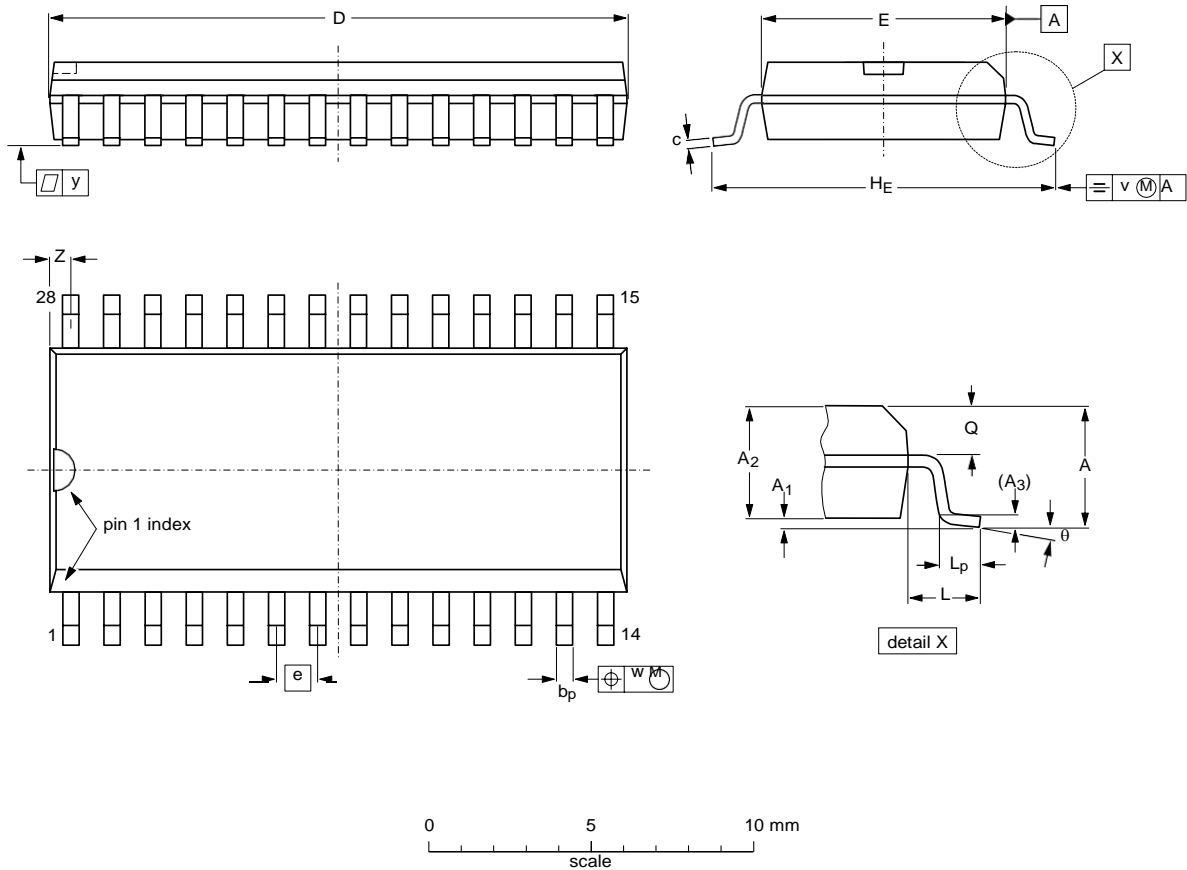


- (1) These capacitors must be of the low ESR-type and be placed near the IC (within 100 mm).
- (2) HT8024A and the microcontroller must use the same  $V_{DD}$  supply.
- (3) Make short, straight connections between CGND, C5 and the ground connection to the capacitor.
- (4) Mount one low ESR-type 100 nF capacitor close to pin  $V_{CC}$ .
- (5) Mount one low ESR-type 100 or 220 nF capacitor close to C1 contact (less than 100 mm from it).
- (6) The connection to C3 should be routed as far from C2, C7, C4 and C8 and, if possible, surrounded by grounded tracks.
- (7) Optional resistor bridge for changing the threshold of  $V_{DD}$ . If this bridge is not required pin 18 should be connected to ground; see Section 8.2.2. Pin 18 is not connected in the HT8024A.

Fig.13 Application diagram.

14 PACKAGE OUTLINES

SO28: plastic small outline package; 28 leads; body width 7.5 mm

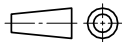


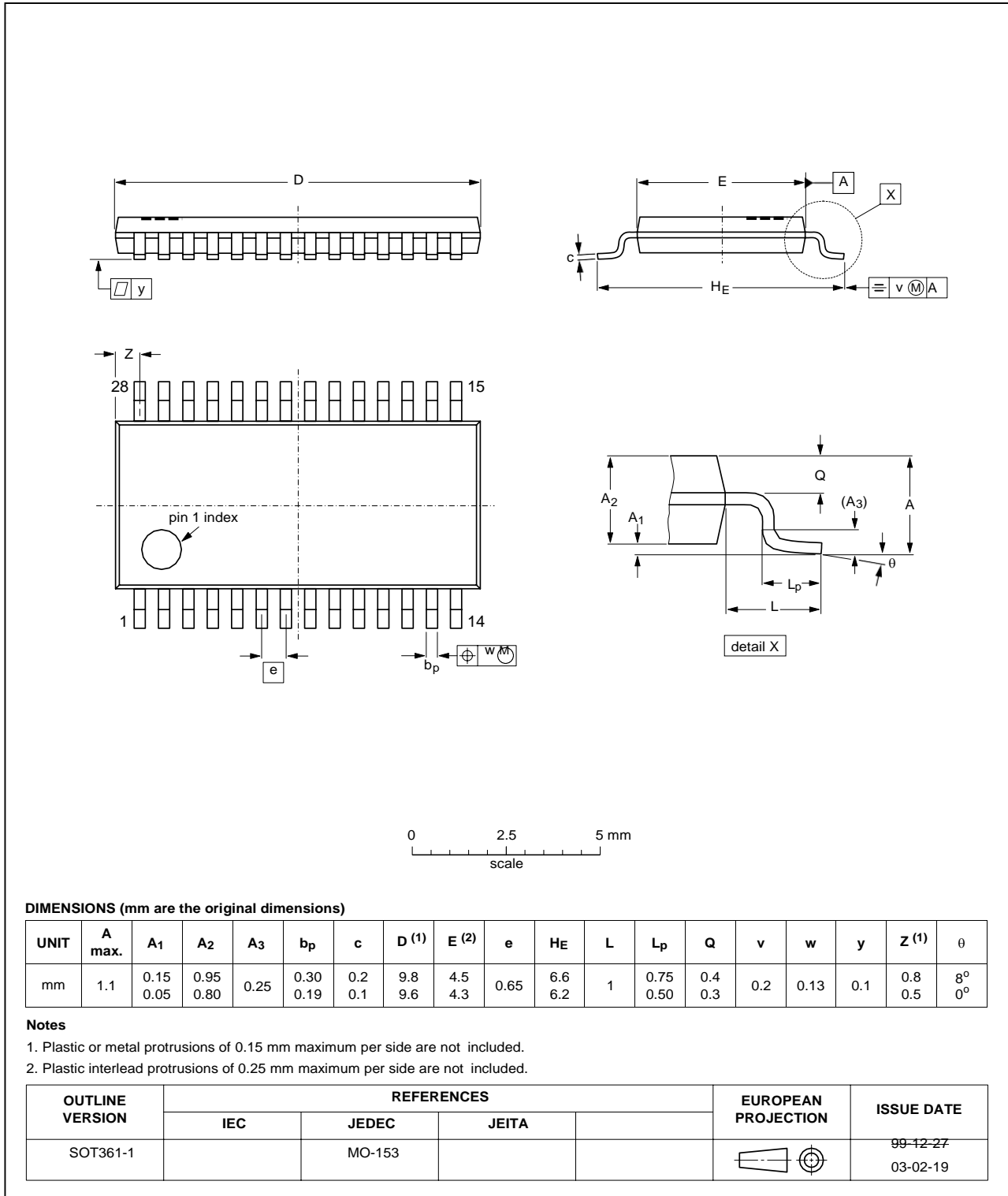
DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT136-1	075E06	MS-013			99-12-27 03-02-19

**TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm**


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