HT893x Single, Dual, Quad 1.8 V, RRIO Operational Amplifiers

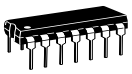
The HT893x family (HT8931 single, HT8932 dual and HT8934 quad) are low-voltage, low- power operational amplifiers. The HT893x family operates from 1.8-V to 5.5-V supply voltages and have rail-to-rail input and output. The input common- mode voltage extends 200 mV beyond the supplies which enables user enhanced functionality beyond the supply voltage range. The output can swing rail- to-rail unloaded and within 105 mV from the rail with 600-Ω load at 1.8-V supply. The HT893x devices are optimized to work at 1.8 V, which make them ideal for portable two-cell, battery-powered systems and single-cell Li-Ion systems.

1 Features

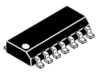
- Typical 1.8-V Supply Values; Unless Otherwise Noted
- Specified at 1.8 V, 2.7 V and 5 V
- Output Swing
  - With 600-Ω Load 80 mV from Rail
  - With 2-kΩ Load 30 mV from Rail
- V_{CM} 200 mV Beyond Rails
- Supply Current (per Channel) 100 μA
- Gain Bandwidth Product 1.4 MHz
- Maximum V_{OS} 3 mV
- Ultra Tiny Packages
- Temperature Range −40°C to +125°C

2 Applications

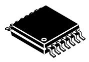
- Phones
- Tablets
- Wearables
- Health Monitoring
- Portable and Battery-Powered Electronic Equipment
- Battery Monitoring



DIP−14 N SUFFIX
HT8934ANZ



SOP−14 R SUFFIX
HT8934ARZ

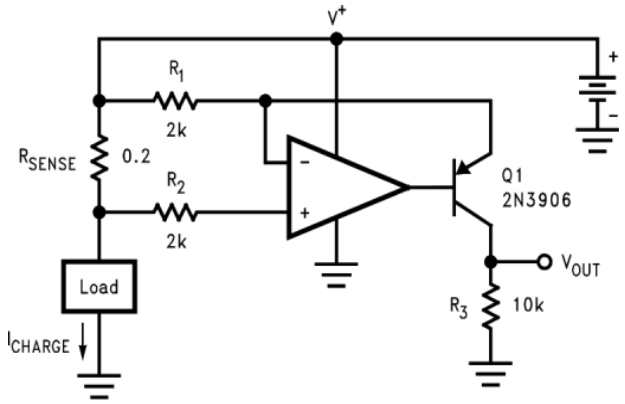


TSSOP−14 T SUFFIX
HT8934ARTZ

T_A = -40° to 125°C for all packages.

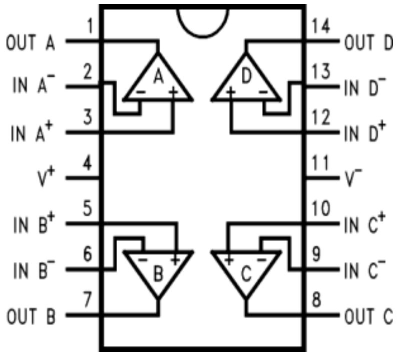
NOTE: suffix B is version, suffix R is roll tape, suffix Z environmental protection.

High-Side Current Sense Amplifier



$$V_{OUT} = \frac{R_{SENSE} \bullet R_3}{R_1} \bullet I_{Charge} = 1\Omega \bullet I_{Charge}$$

14-Pin TSSOP and SOIC
HT8934 Top View



PIN			I/O	DESCRIPTION
NAME	HT8932	HT8934		
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	—	10	I	Noninverting input, channel C
+IN D	—	12	I	Noninverting input, channel D
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	—	9	I	Inverting input, channel C
–IN D	—	13	I	Inverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	—	8	O	Output, channel C
OUT D	—	14	O	Output, channel D
V+	8	4	P	Positive (highest) power supply
V–	4	11	P	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

See (1) (2).

	MIN	MAX	UNIT
Supply voltage ($V^+ – V^-$)	–0.3	6	V
Differential input voltage	V^-	V^+	V
Voltage at input/output pins	(V^-) - 0.3	(V^+) + 0.3	V
Junction temperature (3)	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not specified. For specifications and the test conditions, see the *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(max)}$, $R_{θJA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}–T_A)/R_{θJA}$. All numbers apply for packages soldered directly into a PC board.

6.2 ESD Ratings (Commercial)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	
		Machine model (MM)(3)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Machine model, 200 Ω in series with 100 pF.

6.3 Recommended Operating Ratings

See(1).

	MIN	MAX	UNIT
Supply voltage range ($V^+ – V^-$)	1.8	5.5	V
Ambient temperature	−40	125	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not specified. For specifications and the test conditions, see the *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC(1)		HT8931		HT8932		HT8934		UNIT
		DBV (SOT-23)	DCK (SC70)	D (SOIC)	DGK (VSSOP)	D (SOIC)	PW (TSSOP)	
		5 PINS	5 PINS	8 PINS	8 PINS	14 PINS	14 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	197.2	285.9	125.9	184.5	94.4	124.8	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	156.7	115.9	70.2	74.3	52.5	51.4	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	55.6	63.7	66.5	105.1	48.9	67.2	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	41.4	4.5	19.8	13.1	14.3	6.6	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	55	62.9	65.9	103.6	48.6	66.6	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 DC Electrical Characteristics 1.8 V

Unless otherwise specified, all limits specified for $T_J = 25°C$. $V^+ = 1.8$ V, $V^- = 0$ V, $V_{CM} = V^+/2$, $V_O = V^+/2$ and $R_L > 1$ MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP [1]	MAX	UNIT
V_{OS}	Input Offset Voltage	HT8931 (Single)	25°C		1	3	mV
			Full Range			3	
		HT8932 (Dual), HT8934 (Quad)	25°C		1	3	mV
			Full Range			3.5	
TCV_{OS}	Input Offset Voltage Average Drift		Full Range		5.5		µV/°C
I_B	Input Bias Current		25°C		15	35	nA
			Full Range			50	
I_{OS}	Input Offset Current		25°C		13	25	nA
			Full Range			40	
I_S	Supply Current (per channel)		25°C		103	185	µA
			Full Range			205	
CMRR	Common-Mode Rejection Ratio	HT8931, $0 \le V_{CM} \le 0.6$ V $1.4\ V \le V_{CM} \le 1.8\ V^{(2)}$	25°C	60	78		dB
			Full Range	55			
		HT8932 and HT8934 $0 \le V_{CM} \le 0.6$ V $1.4\ V \le V_{CM} \le 1.8\ V^{(2)}$	25°C	55	76		dB
			Full Range	50			
		$-0.2\ V \le V_{CM} \le 0$ V $1.8\ V \le V_{CM} \le 2.0$ V	25°C	50	72		dB
PSRR	Power Supply Rejection Ratio	$1.8\ V \le V^+ \le 5$ V	25°C	75	100		dB
			Full Range	70			
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50dB	25°C	$V^- - 0.2$	−0.2 to 2.1	$V^+ + 0.2$	V
			−40°C to 85°C	V^-		V^+	
			125°C	$V^- + 0.2$		$V^+ - 0.2$	
A_V	Large Signal Voltage Gain HT8931 (Single)	$R_L = 600\ \Omega$ to 0.9 V, $V_O = 0.2$ V to 1.6 V, $V_{CM} = 0.5$ V	25°C	77	101		dB
			Full Range	73			
		$R_L = 2\ k\Omega$ to 0.9 V, $V_O = 0.2$ V to 1.6 V, $V_{CM} = 0.5$ V	25°C	80	105		dB
			Full Range	75			
	Large Signal Voltage Gain HT8932 (Dual) HT8934 (Quad)	$R_L = 600\ \Omega$ to 0.9 V, $V_O = 0.2$ V to 1.6 V, $V_{CM} = 0.5$ V	25°C	75	90		dB
			Full Range	72			
		$R_L = 2\ k\Omega$ to 0.9 V, $V_O = 0.2$ V to 1.6 V, $V_{CM} = 0.5$ V	25°C	78	100		dB
			Full Range	75			
V_O	Output Swing	$R_L = 600\ \Omega$ to 0.9 V $V_{IN} = \pm 100$ mV	25°C	1.65	1.72		V
					0.077	0.105	
			Full Range	1.63		0.120	
		$R_L = 2\ k\Omega$ to 0.9 V $V_{IN} = \pm 100$ mV	25°C	1.75	1.77		V
					0.024	0.035	
			Full Range	1.74		0.04	

DC Electrical Characteristics 1.8 V (continued)

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 1.8 V, V^- = 0 V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP [(1)]	MAX	UNIT
I_O	Output Short Circuit Current[(3)]	Sourcing, V_O = 0 V V_{IN} = 100 mV	25°C	4	8		mA
			Full Range	3.3			
		Sinking, V_O = 1.8 V V_{IN} = −100 mV	25°C	7	9		mA
			Full Range	5			

(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

6.6 AC Electrical Characteristics 1.8 V

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 1.8 V, V^- = 0 V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP [(1)]	MAX	UNIT
SR	Slew Rate	See [(2)].		0.35		V/µs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			67		deg
G_m	Gain Margin			7		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 0.5 V		60		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz
THD	Total Harmonic Distortion	f = 1 kHz, A_V = +1 R_L = 600 Ω, V_{IN} = 1 V_{PP}		0.023%		
	Amplifier-to-Amplifier Isolation	See[(3)]		123		dB

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(2) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.

(3) Input referred, R_L = 100 kΩ connected to $V^+/2$. Each amplifier excited in turn with 1 kHz to produce V_O = 3 V_{PP} (For supply voltages < 3 V, V_O = V^+).

6.7 DC Electrical Characteristics 2.7 V

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 2.7 V, V^- = 0 V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP [(1)]	MAX	UNIT
V_{OS}	Input Offset Voltage	HT8931 (Single)	25°C		1	4	mV
			Full Range			6	
		HT8932 (Dual) HT8934 (Quad)	25°C		1	5.5	mV
			Full Range			7.5	
TCV_{OS}	Input Offset Voltage Average Drift		Full Range		5.5		µV/°C
I_B	Input Bias Current		25°C		15	35	nA
			Full Range			50	
I_{OS}	Input Offset Current		25°C		8	25	nA
			Full Range			40	
I_S	Supply Current (per channel)		25°C		105	190	µA
			Full Range			210	

DC Electrical Characteristics 2.7 V (continued)

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 2.7 V, V^- = 0 V, $V_{CM} = V^+/2$, $V_O = V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP [1]	MAX	UNIT
CMRR	Common-Mode Rejection Ratio	HT8931, $0 \le V_{CM} \le 1.5$ V $2.3\text{ V} \le V_{CM} \le 2.7\text{ V}^{(2)}$	25°C	60	81		dB
			Full Range	55			
		LHT8932 and HT8934 $0 \le V_{CM} \le 1.5$ V $2.3\text{ V} \le V_{CM} \le 2.7\text{ V}^{(2)}$	25°C	55	80		dB
			Full Range	50			
		$-0.2\text{ V} \le V_{CM} \le 0$ V $2.7\text{ V} \le V_{CM} \le 2.9$ V	25°C	50	74		dB
PSRR	Power Supply Rejection Ratio	$1.8\text{ V} \le V^+ \le 5$ V V_{CM} = 0.5 V	25°C	75	100		dB
			Full Range	70			
V_{CM}	Input Common-Mode Voltage Range	For CMRR Range ≥ 50 dB	25°C	$V^- - 0.2$	−0.2 to 3.0	$V^+ + 0.2$	V
			−40°C to 85°C	V^-		V^+	
			125°C	$V^- + 0.2$		$V^+ - 0.2$	
A_V	Large Signal Voltage Gain HT8931 (Single)	R_L = 600 Ω to 1.35 V, V_O = 0.2 V to 2.5 V	25°C	87	104		dB
			Full Range	86			
		R_L = 2 kΩ to 1.35 V, V_O = 0.2 V to 2.5 V	25°C	92	110		dB
			Full Range	91			
	Large Signal Voltage Gain HT8932 (Dual) HT8934 (Quad)	R_L = 600 Ω to 1.35 V, V_O = 0.2 V to 2.5 V	25°C	78	90		dB
			Full Range	75			
		R_L = 2 kΩ to 1.35 V, V_O = 0.2 V to 2.5 V	25°C	81	100		dB
			Full Range	78			
V_O	Output Swing	R_L = 600 Ω to 1.35 V V_{IN} = ±100 mV	25°C	2.55	2.62		V
					0.083	0.110	
			Full Range	2.53		0.130	
		R_L = 2 kΩ to 1.35 V V_{IN} = ±100 mV	25°C	2.65	2.675		V
					0.025	0.04	
			Full Range	2.64		0.045	
I_O	Output Short Circuit Current[3]	Sourcing, V_O = 0 V V_{IN} = +100 mV	25°C	20	30		mA
			Full Range	15			
		Sinking, V_O = 2.7 V V_{IN} = −100 mV	25°C	18	25		mA
			Full Range	12			

(2) For specified temperature ranges, see the CMVR parameter in *DC Electrical Characteristics 1.8 V* for the input common-mode voltage specifications.

(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

6.8 AC Electrical Characteristics 2.7 V

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.0 V, V_O = 1.35 V and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
SR	Slew Rate	See[2]		0.4		V/µs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			70		deg
G_m	Gain Margin			7.5		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 0.5 V		57		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(2) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.

AC Electrical Characteristics 2.7 V (continued)

Unless otherwise specified, all limits specified for $T_J = 25°C$. $V^+ = 2.7$ V, $V^- = 0$ V, $V_{CM} = 1.0$ V, $V_O = 1.35$ V and $R_L >$ 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
THD	Total Harmonic Distortion	f = 1 kHz, $A_V = +1$ $R_L = 600$ Ω, $V_{IN} = 1$ V_{PP}		0.022%		
	Amp-to-Amp Isolation	See(3)		123		dB

(3) Input referred, $R_L = 100$ kΩ connected to $V^+/2$. Each amplifier excited in turn with 1 kHz to produce $V_O = 3$ V_{PP} (For supply voltages < 3 V, $V_O = V^+$).

6.9 Electrical Characteristics 5 V DC

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 5 V, V^- = 0 V, $V_{CM} = V^+/2$, $V_O = V^+/2$ and $R_L > 1$ MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
V_{OS}	Input Offset Voltage	HT8931 (Single)	25°C		1	4	mV
			Full Range			6	
		HT8932 (Dual) HT8934 (Quad)	25°C		1	5.5	mV
			Full Range			7.5	
TCV_{OS}	Input Offset Voltage Average Drift				5.5		µV/°C
I_B	Input Bias Current		25°C		14	35	nA
			Full Range			50	
I_{OS}	Input Offset Current		25°C		9	25	nA
			Full Range			40	
I_S	Supply Current (per channel)		25°C		116	210	µA
			Full Range			230	
CMRR	Common-Mode Rejection Ratio	$0 \le V_{CM} \le 3.8$ V $4.6\ V \le V_{CM} \le 5\ V$(2)	25°C	60	86		dB
			Full Range	55			
		$-0.2\ V \le V_{CM} \le 0$ V $5\ V \le V_{CM} \le 5.2$ V	25°C	50	78		dB
PSRR	Power Supply Rejection Ratio	$1.8\ V \le V^+ \le 5$ V V_{CM} = 0.5 V	25°C	75	100		dB
			Full Range	70			
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50 dB	25°C	$V^- - 0.2$	−0.2 to 5.3	$V^+ + 0.2$	V
			−40°C to 85°C	V^-		V^+	
			125°C	$V^- + 0.3$		$V^+ - 0.3$	
A_V	Large Signal Voltage Gain HT8931 (Single)	R_L = 600 Ω to 2.5 V, V_O = 0.2 V to 4.8 V	25°C	88	102		dB
			Full Range	87			
		R_L = 2 kΩ to 2.5 V, V_O = 0.2 V to 4.8 V	25°C	94	113		dB
			Full Range	93			
	Large Signal Voltage Gain HT8932 (Dual) HT8934 (Quad)	R_L = 600 Ω to 2.5 V, V_O = 0.2 V to 4.8 V	25°C	81	90		dB
			Full Range	78			
		R_L = 2 kΩ to 2.5 V, V_O = 0.2 V to 4.8 V	25°C	85	100		dB
			Full Range	82			
V_O	Output Swing	R_L = 600 Ω to 2.5 V V_{IN} = ±100 mV	25°C	4.855	4.890		V
					0.120	0.160	
			Full Range	4.835		0.180	
		R_L = 2 kΩ to 2.5 V V_{IN} = ±100 mV	25°C	4.945	4.967		V
					0.037	0.065	
			Full Range	4.935		0.075	
I_O	Output Short Circuit Current(3)	HT8931, Sourcing, V_O = 0 V V_{IN} = +100 mV	25°C	80	100		mA
			Full Range	68			
		Sinking, V_O = 5 V V_{IN} = −100 mV	25°C	58	65		mA
			Full Range	45			

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(2) For specified temperature ranges, see the CMVR parameter in *DC Electrical Characteristics 1.8 V* for the input common-mode voltage specifications.

(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

6.10 AC Electrical Characteristics 5 V

Unless otherwise specified, all limits specified for $T_J = 25°C$. $V^+ = 5$ V, $V^- = 0$ V, $V_{CM} = V^+/2$, $V_O = 2.5$ V and $R_L >$ 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
SR	Slew Rate	See .[2]		0.42		V/µs
GBW	Gain-Bandwidth Product			1.5		MHz
Φ_m	Phase Margin			71		deg
G_m	Gain Margin			8		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, $V_{CM} = 1$ V		50		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz
THD	Total Harmonic Distortion	f = 1 kHz, $A_V = 1$ $R_L = 600$ Ω, $V_O = 1$ V_{PP}		0.022%		
	Amplifier-to-Amplifier Isolation	See[3]		123		dB

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(2) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.

(3) Input referred, $R_L = 100$ kΩ connected to $V^+/2$. Each amplifier excited in turn with 1 kHz to produce $V_O = 3$ V_{PP} (For supply voltages < 3 V, $V_O = V^+$).

6.11 Typical Characteristics

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

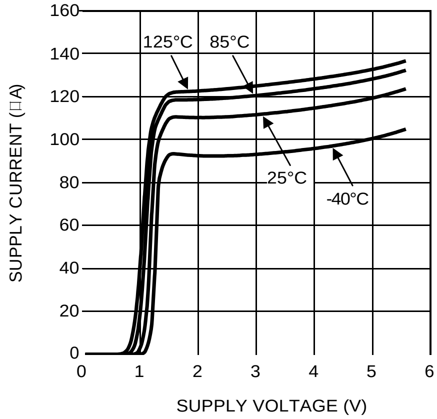


Figure 1. Supply Current vs Supply Voltage (HT8931)

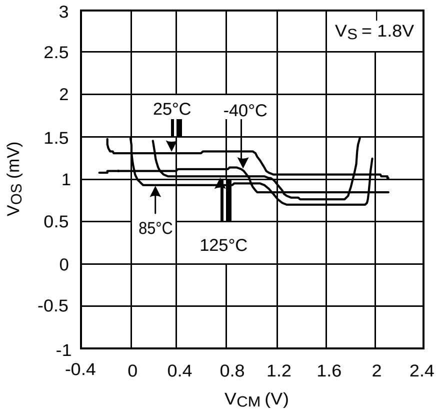


Figure 2. Offset Voltage vs Common-Mode Range

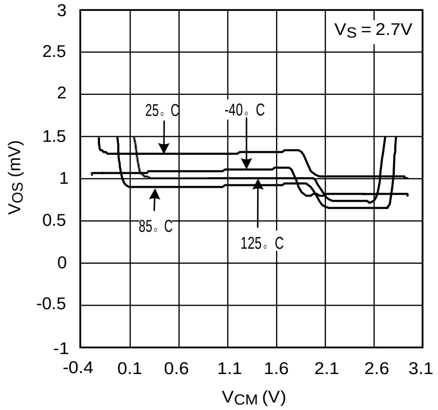


Figure 3. Offset Voltage vs Common-Mode Range

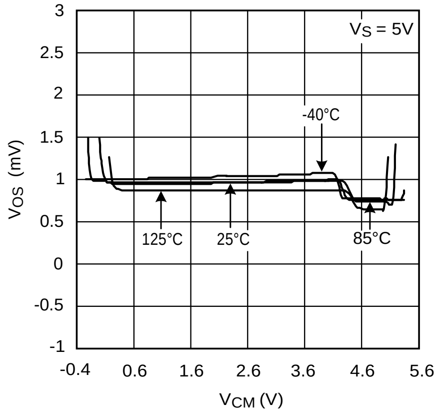


Figure 4. Offset Voltage vs Common-Mode Range

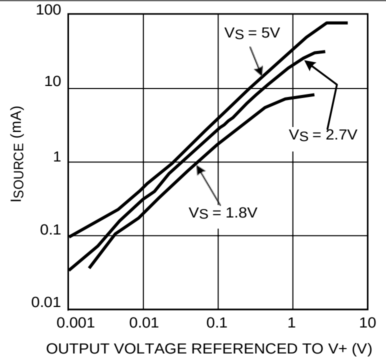


Figure 5. Sourcing Current vs Output Voltage

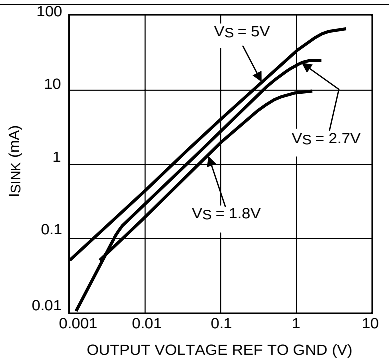
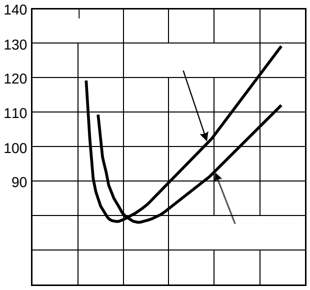
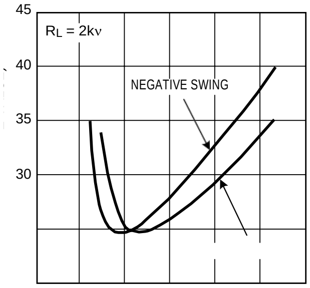


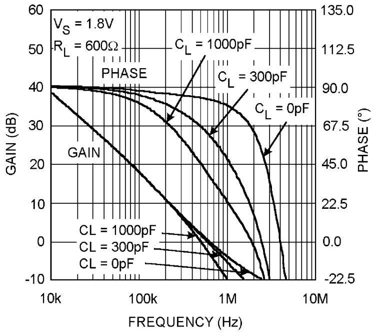
Figure 6. Sinking Current vs Output Voltage

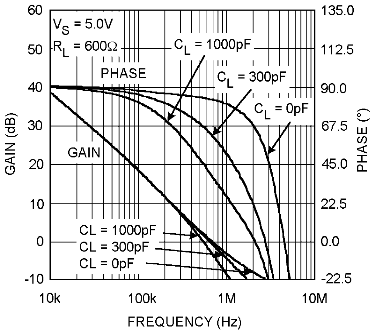
Typical Characteristics (continued)

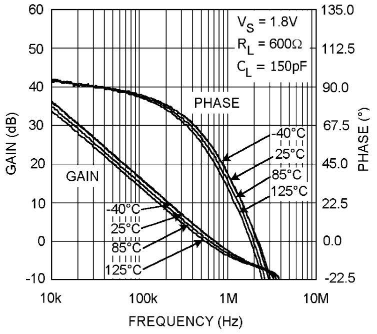
Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

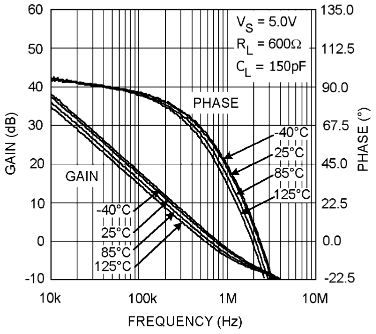












Typical Characteristics (continued)

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

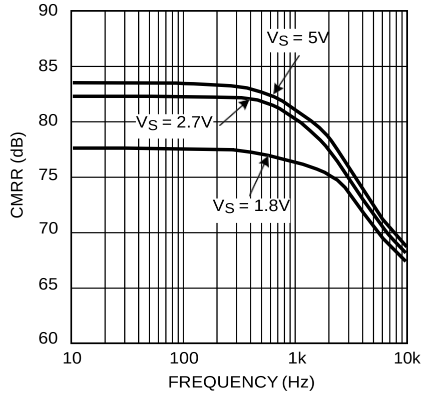


Figure 13. CMRR vs Frequency

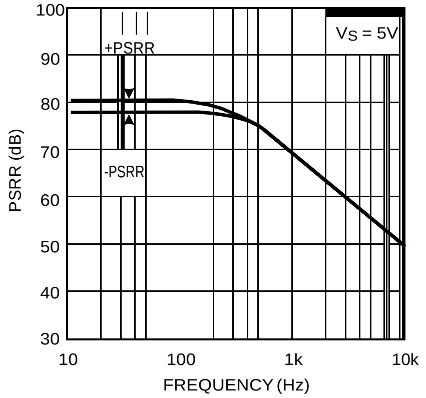


Figure 14. PSRR vs Frequency

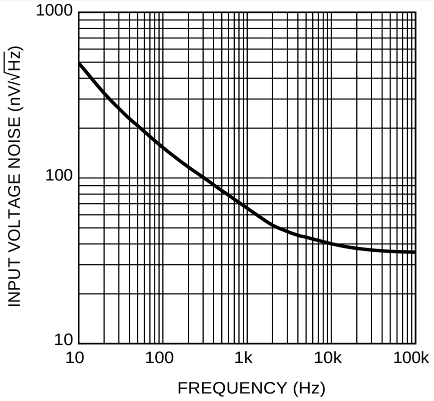


Figure 15. Input Voltage Noise vs Frequency

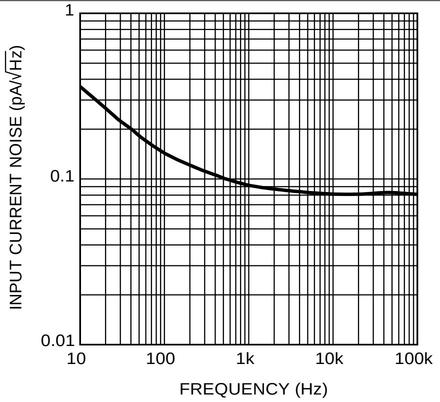


Figure 16. Input Current Noise vs Frequency

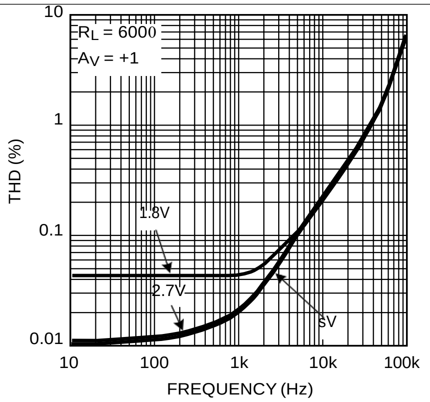


Figure 17. THD vs Frequency

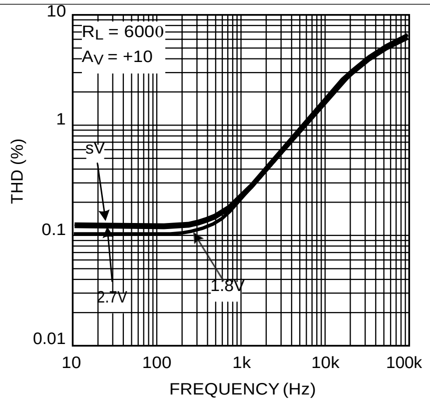


Figure 18. THD vs Frequency

Typical Characteristics (continued)

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

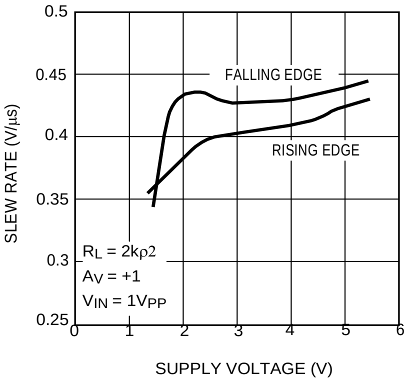


Figure 19. Slew Rate vs Supply Voltage

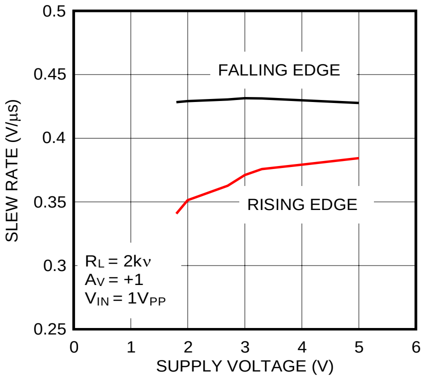


Figure 20. Slew Rate vs Supply Voltage

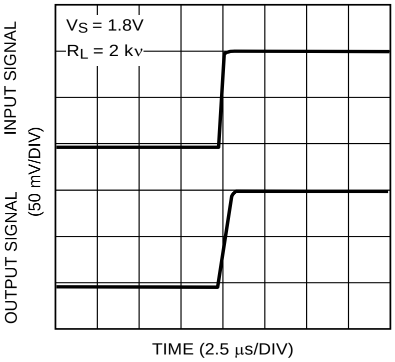


Figure 21. Small Signal Noninverting Response

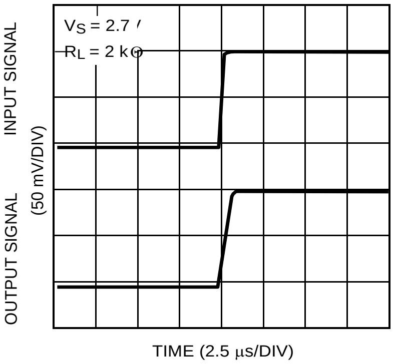


Figure 22. Small Signal Noninverting Response

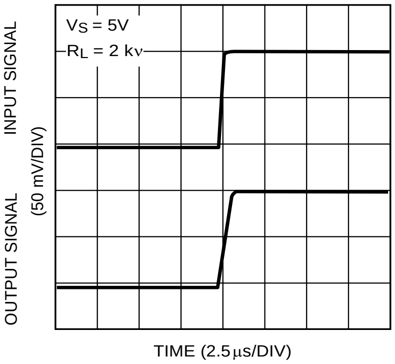


Figure 23. Small Signal Noninverting Response

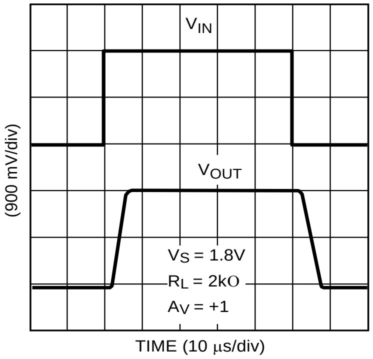
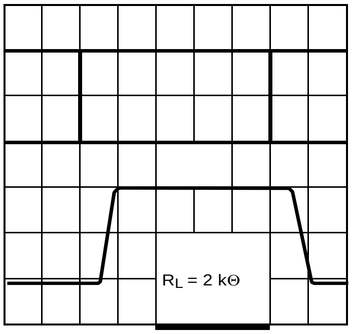
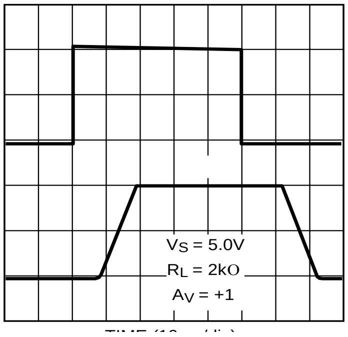


Figure 24. Large Signal Noninverting Response

Typical Characteristics (continued)

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.





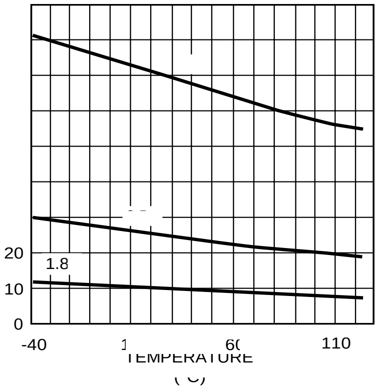
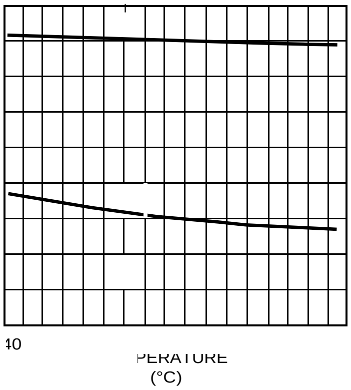


Figure 27. Short Circuit Current vs Temperature (Sinking)



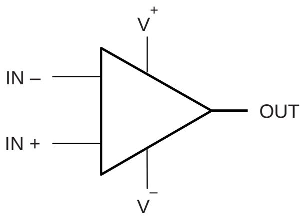
gure 28. Short Circuit Current vs Temperature (Sourcing)

7 Detailed Description

7.1 Overview

The HT893x are low-voltage, low-power operational amplifiers (op-amp) operating from 1.8-V to 5.5-V supply voltages and have rail-to-rail input and output. HT893x input common-mode voltage extends 200 mV beyond the supplies which enables user enhanced functionality beyond the supply voltage range.

7.2 Functional Block Diagram



(Each Amplifier)

7.3 Feature Description

The differential inputs of the amplifier consist of a noninverting input (+IN) and an inverting input (–IN). The amplifer amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by Equation 1:

$$V_{OUT} = A_{OL} (IN^{+} - IN^{-}) \quad (1)$$

where

- A_{OL} is the open-loop gain of the amplifier, typically around 100 dB (100,000x, or 10 µV per volt).

7.4 Device Functional Modes

7.4.1 Input and Output Stage

The rail-to-rail input stage of this family provides more flexibility for the designer. The HT893x use a complimentary PNP and NPN input stage in which the PNP stage senses common-mode voltage near V^{-} and the NPN stage senses common-mode voltage near V^{+}. The transition from the PNP stage to NPN stage occurs 1 V below V^{+}. Because both input stages have their own offset voltage, the offset of the amplifier becomes a function of the input common-mode voltage and has a crossover point at 1 V below V^{+}.

Device Functional Modes (continued)

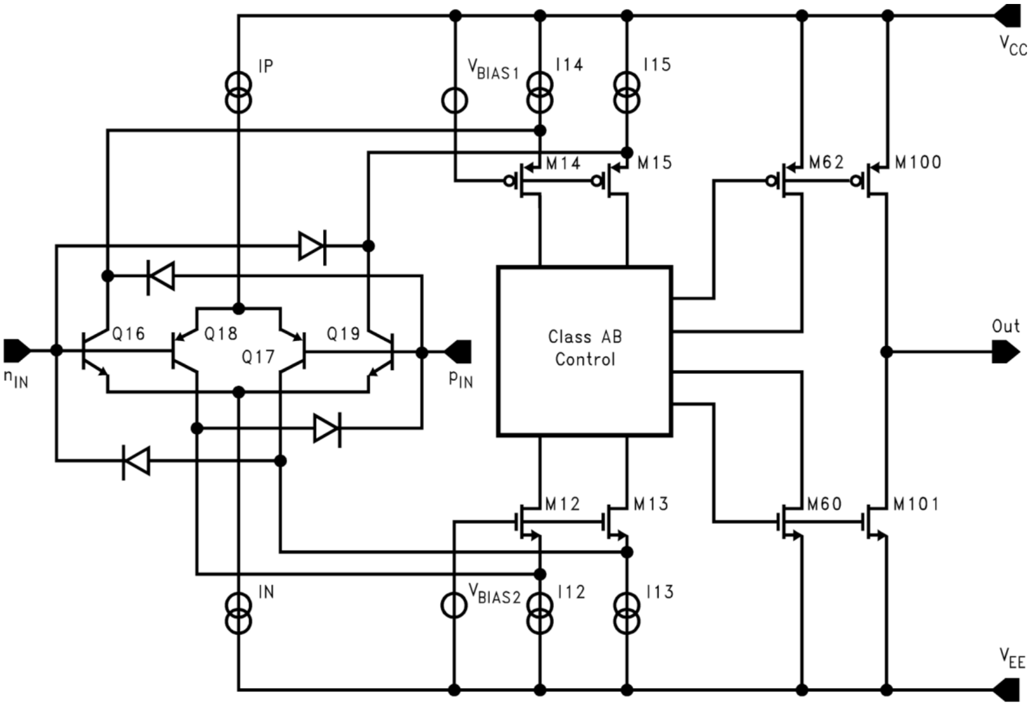


Figure 29. Simplified Schematic Diagram

This V_{OS} crossover point can create problems for both DC− and AC-coupled signals if proper care is not taken. Large input signals that include the V_{OS} crossover point will cause distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover. For example, in a unity gain buffer configuration with $V_S = 5$ V, a 5-V peak-to-peak signal will contain input-crossover distortion while a 3-V peak-to-peak signal centered at 1.5 V will not contain input-crossover distortion as it avoids the crossover point. Another way to avoid large signal distortion is to use a gain of −1 circuit which avoids any voltage excursions at the input terminals of the amplifier. In that circuit, the common-mode DC voltage can be set at a level away from the V_{OS} cross-over point. For small signals, this transition in V_{OS} shows up as a V_{CM} dependent spurious signal in series with the input signal and can effectively degrade small signal parameters such as gain and common-mode rejection ratio. To resolve this problem, the small signal should be placed such that it avoids the V_{OS} crossover point. In addition to the rail-to-rail performance, the output stage can provide enough output current to drive 600-Ω loads. Because of the high-current capability, take care not to exceed the 150°C maximum junction temperature specification.

7.4.2 Input Bias Current Consideration

The HT893x family has a complementary bipolar input stage. The typical input bias current (I_B) is 15 nA. The input bias current can develop a significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F. For example, if I_B is 50 nA and R_F is 100 kΩ, then an offset voltage of 5 mV will develop ($V_{OS} = I_B \times R_F$). Using a compensation resistor (R_C), as shown in Figure 30, cancels this effect. But the input offset current (I_{OS}) will still contribute to an offset voltage in the same manner.

Device Functional Modes (continued)

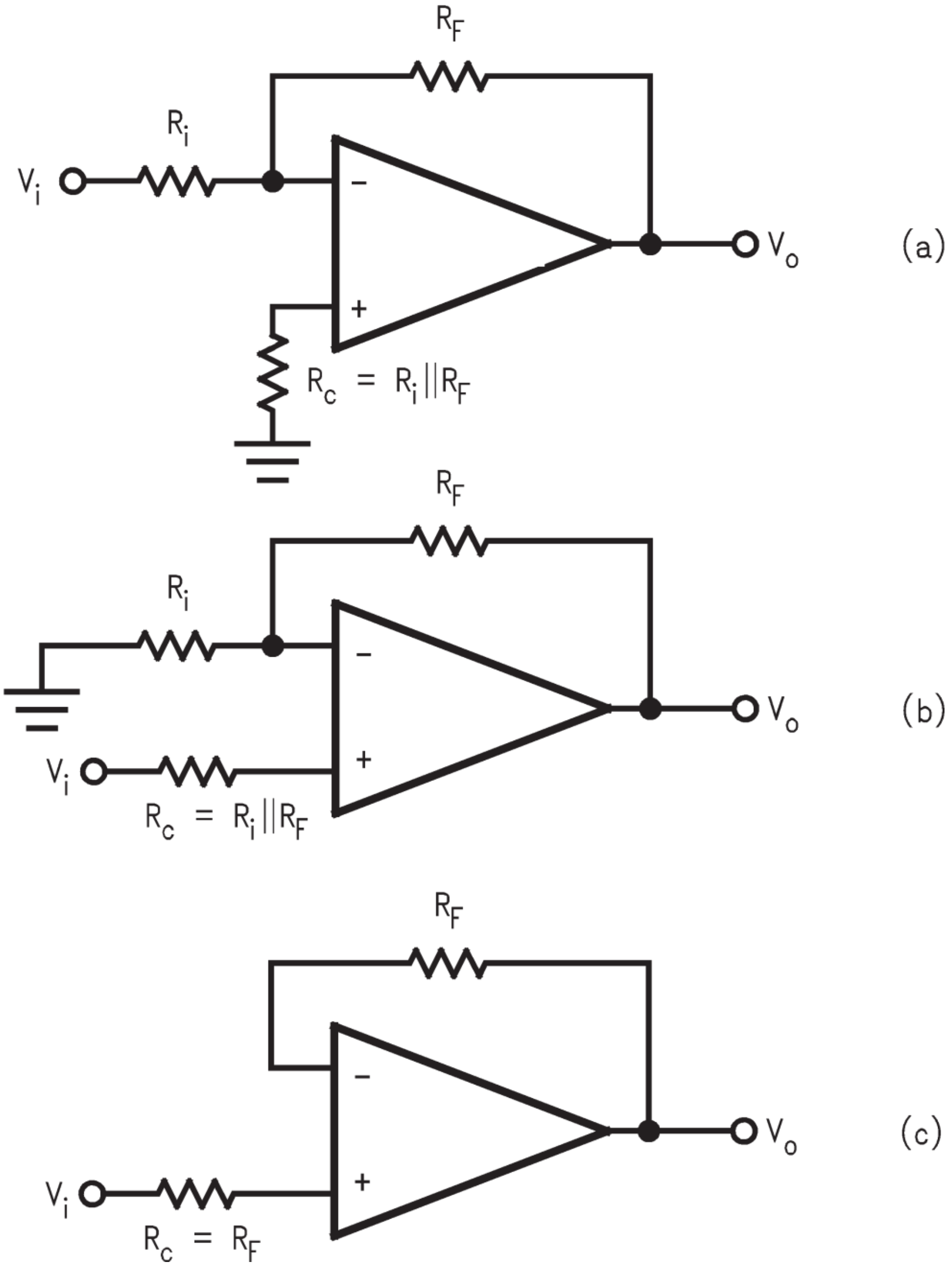


Figure 30. Canceling the Offset Voltage due to Input Bias Current

8 Application and Implementation

NOTE

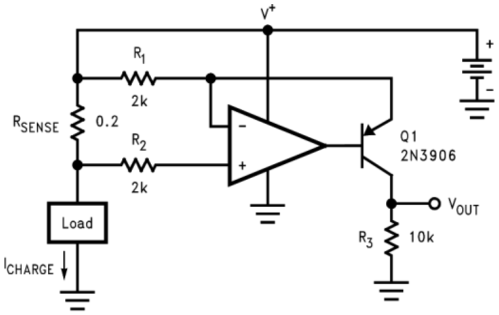
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The HT893x devices bring performance, economy and ease-of-use to low-voltage, low-power systems. They provide rail-to-rail input and rail-to-rail output swings into heavy loads.

8.2 Typical Applications

8.2.1 High-Side Current-Sensing Application



$$V_{OUT} = \frac{R_{SENSE} \bullet R_3}{R_1} \bullet I_{Charge} = 1\Omega \bullet I_{Charge}$$

Figure 31. High-Side Current Sensing

8.2.1.1 Design Requirements

The high-side current-sensing circuit (Figure 31) is commonly used in a battery charger to monitor charging current to prevent overcharging. A sense resistor R_{SENSE} is connected to the battery directly. This system requires an op amp with rail-to-rail input. The HT893x are ideal for this application because its common-mode input range extends up to the positive supply.

8.2.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the HT893x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

As seen in Figure 31, the I_{CHARGE} current flowing through sense resistor R_{SENSE} develops a voltage drop equal to V_{SENSE}. The voltage at the negative sense point will now be less than the positive sense point by an amount proportional to the V_{SENSE} voltage.

The low-bias currents of the HT893x cause little voltage drop through R_2, so the negative input of the HT893x amplifier is at essentially the same potential as the negative sense input.

The HT893x will detect this voltage error between its inputs and servo the transistor base to conduct more current through Q1, increasing the voltage drop across R_1 until the HT893x inverting input matches the noninverting input. At this point, the voltage drop across R_1 now matches V_{SENSE}.

I_G, a current proportional to I_{CHARGE}, will flow according to the following relation:

$$I_G = V_{RSENSE} / R_1 = (R_{SENSE} * I_{CHARGE}) / R_1 \quad (2)$$

I_G also flows through the gain resistor R_3 developing a voltage drop equal to:

$$V_3 = I_G * R_3 = (V_{RSENSE} / R_1) * R_3 = ((R_{SENSE} * I_{CHARGE}) / R_2) * R_3 \quad (3)$$

Typical Applications (continued)

$V_{OUT} = (R_{SENSE} * I_{CHARGE}) * G$

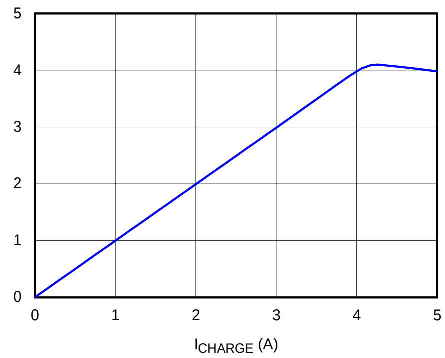
where

- $G = R_3 / R_1$ (4)

The other channel of the HT893x may be used to buffer the voltage across R3 to drive the following stages.

8.2.1.3 Application Curve

Figure 32 shows the results of the example current sense circuit.



NOTE: the error after 4 V where transistor Q1 runs out of headroom and saturates, limiting the upper output swing.

Figure 32. Current Sense Amplifier Results

8.2.2 Half-Wave Rectifier Applications

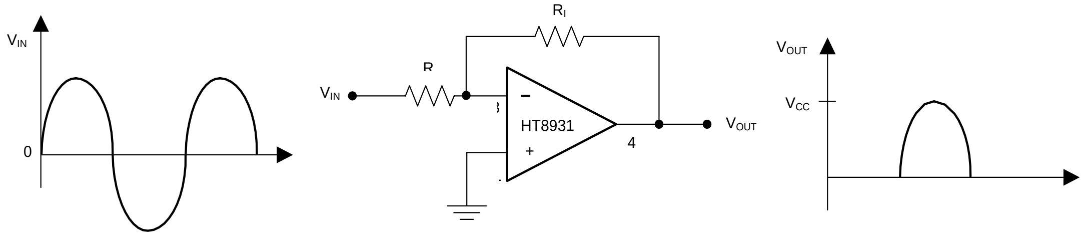


Figure 33. Half-Wave Rectifier With Rail-To-Ground Output Swing Referenced to Ground

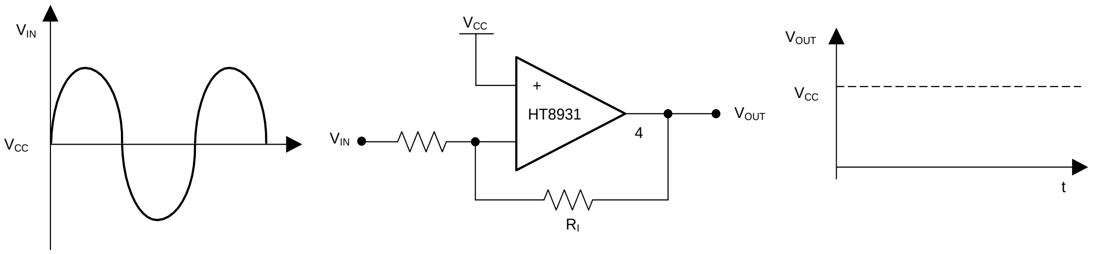


Figure 34. Half-Wave Rectifier With Negative-Going Output Referenced to V_{CC}

Typical Applications (continued)

8.2.2.1 Design Requirements

Because the HT8931, HT8932, HT8934 input common-mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction is an easy task. All that is needed are two external resistors; there is no need for diodes or matched resistors. The half-wave rectifier can have either positive or negative going outputs, depending on the way the circuit is arranged.

8.2.2.2 Detailed Design Procedure

In Figure 33 the circuit is referenced to ground, while in Figure 34 the circuit is biased to the positive supply. These configurations implement the half-wave rectifier because the HT893x can not respond to one-half of the incoming waveform. It can not respond to one-half of the incoming because the amplifier cannot swing the output beyond either rail therefore the output disengages during this half cycle. During the other half cycle, however, the amplifier achieves a half wave that can have a peak equal to the total supply voltage. R_l should be large enough not to load the HT893x.

8.2.2.3 Application Curve

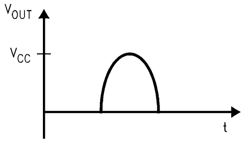


Figure 35. Output of Ground-to-Rail Circuit

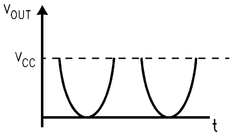


Figure 36. Output of Rail-to-Ground Circuit

8.2.3 Instrumentation Amplifier With Rail-to-Rail Input and Output Application

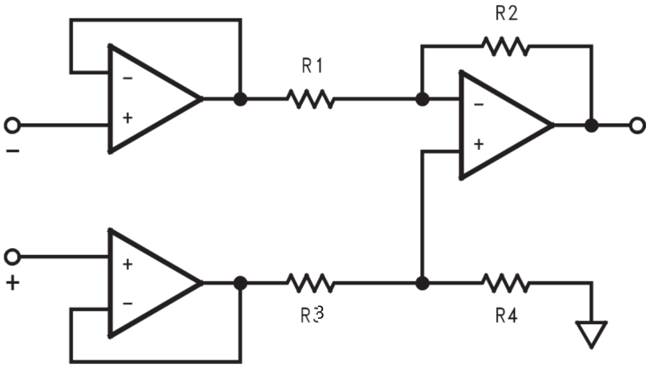


Figure 37. Rail-to-Rail Instrumentation Amplifier

8.2.3.1 Design Requirements

Using three of the HT893x amplifiers, an instrumentation amplifier with rail-to-rail inputs and outputs can be made as shown in Figure 37.

8.2.3.2 Detailed Design Procedure

In this example, amplifiers on the left side act as buffers to the differential stage. These buffers assure that the input impedance is very high. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMRR set by the matching R_1-R_2 with R_3-R_4. The gain is set by the ratio of R_2/R_1 and R_3 should equal R_1 and R_4 equal R_2. With both rail-to-rail input and output ranges, the input and output are only limited by the supply voltages. Remember that even with rail-to-rail outputs, the output can not swing past the supplies so the combined common-mode voltages plus the signal should not be greater that the supplies or limiting will occur.

Typical Applications (continued)

8.2.3.3 Application Curve

Figure 38 shows the results of the instrumentation amplifier with R_1 and R_3 = 1 K, and R_2 and R_4 = 100 kΩ, for a gain of 100, running on a single 5-V supply with a input of $V_{CM} = V_S/2$. The combined effects of the individual offset voltages can be seen as a shift in the offset of the curve.

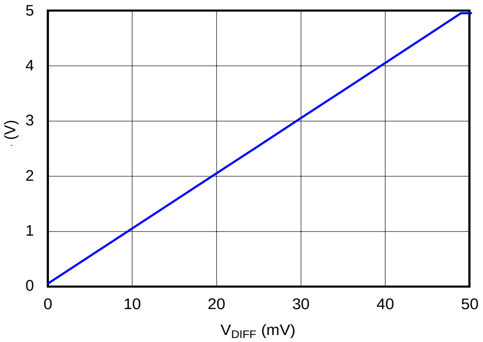


Figure 38. Instrumentation Amplifier Output Results

8.3 Dos and Don'ts

Do properly bypass the power supplies.

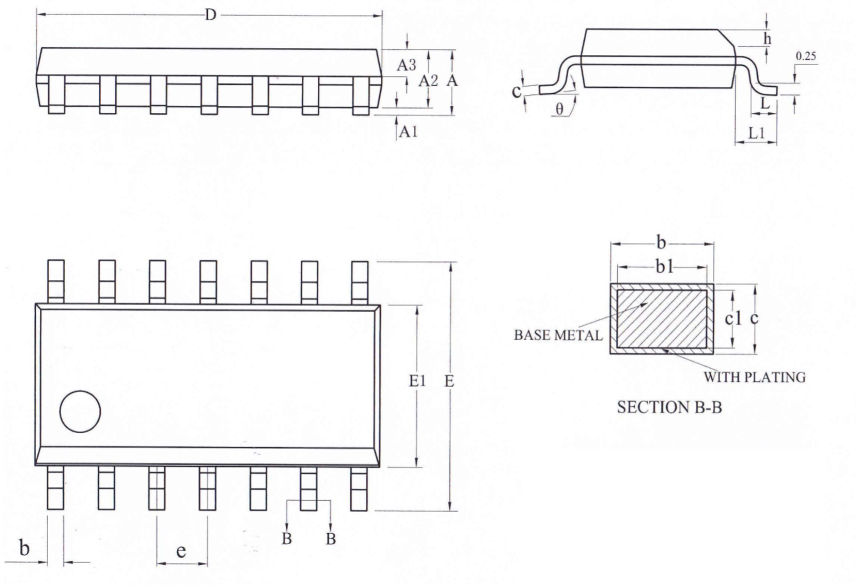
Do add series resistence to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1 kΩ per volt).

9 Power Supply Recommendations

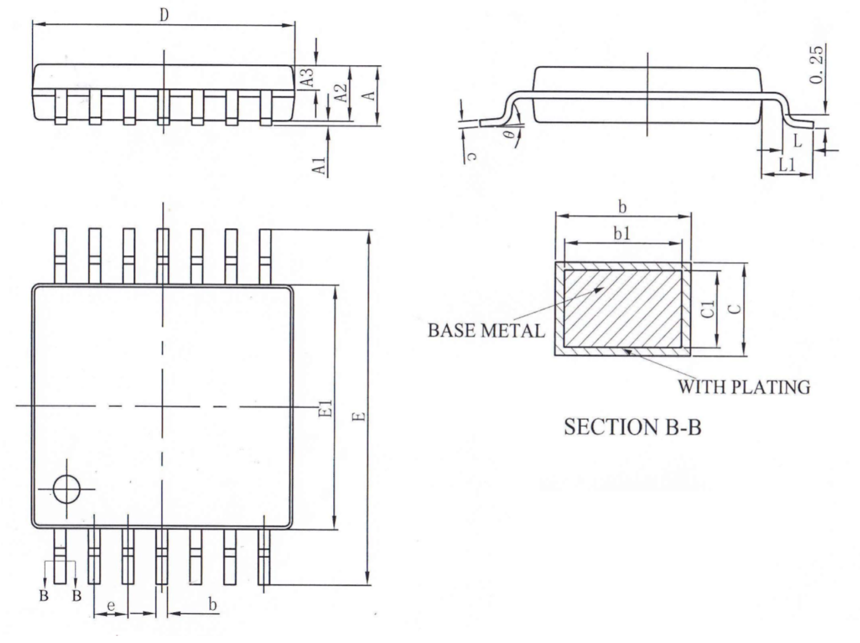
For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the op amp power supply pins. For single-supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

SOP14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
⚠ b	0.39	—	0.47
⚠ b1	0.38	0.41	0.44
⚠ c	0.20	—	0.24
c1	0.19	0.20	0.21
⚠ D	8.55	8.65	8.75
E	5.80	6.00	6.20
⚠ E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

TSSOP14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°