8-Bit 50MSPS 3.3V A/D CONVERTER

FEATURES

- CMOS 8-Bit 50 MSPS A/D CONVERTER
- EXCELLENT SPURIOUS-FREE DYNAMIC RANGE PERFORMANCE
- SINGLE 3.3V POWER SUPPLY
- LOW POWER CONSUMPTION
- 28-PIN SSOP PB-FREE PACKAGE

PRODUCT HIGHLIGHTS

- Maximum sampling clock frequency 50 MHz
- Resolution: 8 bit
- DNL ±0.2LSB
- SFDR 68 dB @ 1 MHz
- 2.7~3.6V analog power supply
- 2.7~3.6V digital power supply
- 2mW Power Consumption at Sleep Mode
- On-Chip Reference
- Out-of-range indicator
- Built-in clamp function

APPLICATIONS

- Video Applications
- Wide Band Data Communication
- Medical Imaging Equipment
- Digital TV
- Measurement Instrumentation

The HT9280A is an 8-bit, 50 MSPS, multistage, analog-to-digital converter with excellent dynamic performance. The HT9280A has an on-chip programmable reference. The HT9280A takes a differential, pipeline architecture. Also it has an on-chip sample-and-hold amplifier and voltage reference. The HT9280A features monolithic, single supply, single clock input and guarantees no missing codes over the full operating temperature range. Benefited from a built-in high performance sample-and-hold amplifier (SHA) and an on-chip

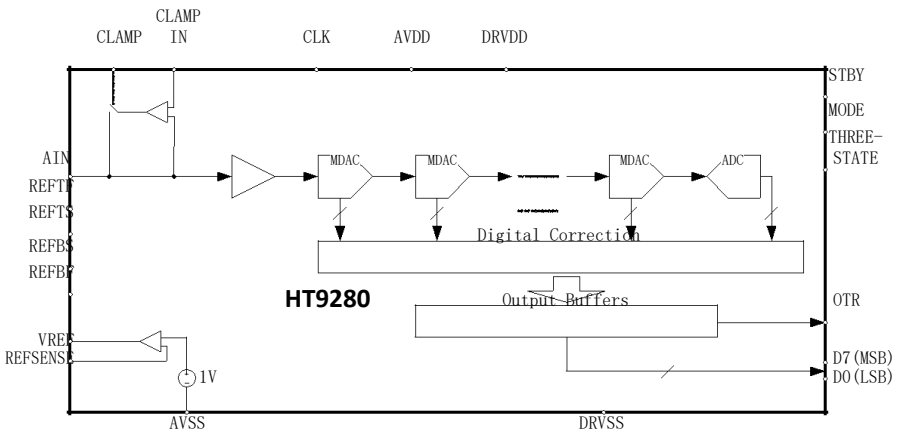
programmable reference, the HT9280A is flexible for various input ranges and offsets, and the input can be either single-ended or differential, which make the HT9280A well suited for imaging and communications systems. For the application that dc accuracy and temperature drift are required, an external reference can also be used.

The output data of the HT9280A is straight binary output

format. When the input overflows, an out-of-range signal (OTR) is set to high, which indicates the overflow condition.

The HT9280A is developed for low-power low-voltage applications. Its supply range is from +2.7 V to +3.6 V. The HT9280A is specified over the industrial (–40°C to +85°C) or commercial (0°C to +70°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

(AVDD = 3.3 V, DVDD = 3.3 V, F_S=50MHz (50% Duty Cycle), MODE=AVDD, 2V Input Span from 0.5V to 2.5V, External Reference, unless otherwise noted.)

PARAMETER	MIN	TYP	MAX	UNITS
RESOLUTION	8			Bits
CONVERSION RATE (F_S)			50	MHz
DC ACCURACY[1]				
Differential Nonlinearity* (DNL)	-0.5	±0.2	+0.5	LSB
Integral Nonlinearity (INL)	-0.5	±0.3	+0.5	LSB
Offset Error	–1.5	±0.2	+1.5	% of FSR
Gain Error (Without Internal Reference)	–4.0	±1.2	+4.0	% of FSR
Gain Error (With Internal Reference)	–5	±1.2	+5	% of FSR
REFERENCE OUTPUT				
Reference Voltage		2		V_{P-P}
Reference Input Resistance		15		kΩ
INTERNAL REFERENCE				
Output Voltage (1V Mode)		1		V
Output Voltage Tolerance (1V Mode)		±10	±40	mV
Output Voltage (2V Mode)		2		V
ANALOG INPUT				
Input Voltage Range**	REFBS		REFTS	V
Input Capacitance		1.5		pF
Aperture Delay		4		ns
Aperture Uncertainty (Jitter)		2		ps
Input Bandwidth (-3dB)		350		MHz
DC Leakage		45		uA
POWER SUPPLY				
Operating Voltage — AVDD	2.7	3.3	3.6	V
Operating Voltage — DRVDD	2.7	3.3	3.6	V
Analog Supply Current*** (I_{AVDD})		27.5	32	mA
Supply Current Sleep Mode (I_{AVDD})		0.6		mA
Power Consumption—P_D		82.7	96.5	mW
Power Supply Rejection Ratio—DVDD		1		% of FSR
OPERATING RANGE	–40		+85	℃

NOTES

* REFTS = 2.5V, REFBS = 0.5V

** REFBS Min = GND; REFTS Max = AVDD

*** AVDD = 3V, MODE = AVSS

DYNAMIC SPECIFICATIONS

(AVDD = 3.3 V, DRVDD = 3.3 V, AIN = 0.5 dBFS, unless otherwise noted.)

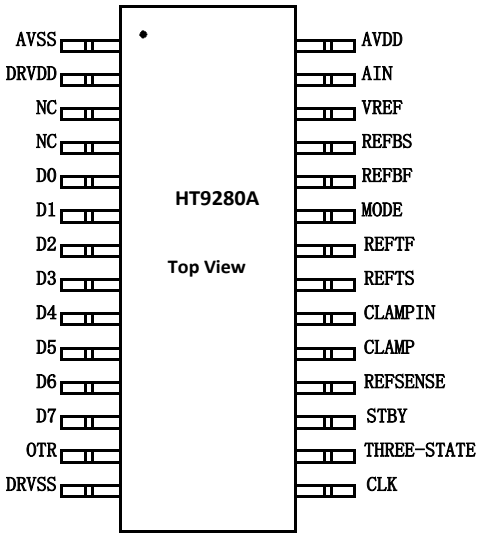
PARAMETER	MIN	TYP	MAX	UNITS
CLOCKING				
Maximum Output Update Rate (f_{CLOCK})		50		MSPS
Clock Pulse Width High		14.7		ns
Clock Pulse Width Low		14.7		ns
DIGITAL INPUT & OUTPUT				
High Input Voltage	2.4			V
Low Input Voltage			0.3	V
High-Z Leakage	-12		+12	uA
Data Valid Delay		15*		ns
Data Enable Delay		11*		ns
Data High-Z Delay		11*		ns
DIGITAL INPUT & OUTPUT				
Signal-to-Noise and Distortion Ratio (SINAD)				
f = 1.01MHz		48.5		dB
f = 3.58MHz		48.5		dB
f = 16MHz		47.4		dB
Effective Bits				
f = 1.01MHz		7.7		Bits
f = 3.58MHz		7.7		Bits
f = 16MHz		7.6		Bits
Signal-to-Noise Ratio (SNR)				
f = 1.01MHz		48.5		dB
f = 3.58MHz		48.5		dB
f = 16MHz		47.4		dB
Spurious Free Dynamic Range (SFDR)				
f = 1.01MHz		68		dB
f = 3.58MHz		67		dB
f = 16MHz		60		dB
Total Harmonic Distortion (THD)				
f = 1.01MHz		-64		dB
f = 3.58MHz		-62		dB
f = 16MHz		-59		dB
Differential Phase		0.2		Degree
Differential Gain		0.1		%

* C_L=15pF

ORDERING GUIDE

Model	Temperature Range	Package Descriptions
HT9280A	-40°C to +85°C	28-Lead SSOP

PIN CONFIGURATION (SSOP28)



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1	AVSS	Analog Ground
2	DRVDD	Digital Driver Supply
3,4	NC	No Connect
5	D0	Bit 0 (LSB)
6-11	D1-D6	B1 – B6
12	D7	Bit 7 (MSB)
13	OTR	Out-of-range Indicator
14	DRVSS	Digital Ground
15	CLK	Clock Input
16	THREE-STATE	HI: High Impedance State. LO: Normal Operation
17	STBY	HI: Power-Down Mode. LO: Normal Operation
18	REFSENSE	Reference Select
19	CLAMP	HI: Enable Clamp Mode. LO: No Clamp
20	CLAMPIN	Clamp Reference Input
21	REFTS	Top Reference
22	REFTF	Top Reference Decoupling
23	MODE	Mode Select
24	REFBF	Bottom Reference Decoupling
25	REFBS	Bottom Reference
26	VREF	Internal Reference Output
27	AIN	Analog Input
28	AVDD	Analog Supply

DEFINITIONS OF SPECIFICATIONS

Differential Nonlinearity (or DNL)

DNL refers to the deviation of each individual code in LSB from the ideal ADC..

Linearity Error (Integral Nonlinearity or INL)

INL is a measure about how DNL is accumulated. It measures the deviation of each individual code from a line drawn from zero scale through positive full scale (1/2 LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

Gain Error

Gain Error indicates the deviation of slope between the actual ADC and the ideal ADC. It measures the difference of the range (the level from the first transition to the last transition) between actual and ideal ADC.

Offset Error

Offset Error measures the deviation of the level of the actual first code transition from the ideal level of 1 LSB above “zero.”

Temperature Drift

Temperature drift indicates the influence of temperature. it measures the deviation of the value at either TMIN or TMAX with the reference value at 25℃. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per ℃. For reference drift, the drift is reported in ppm per ℃.

Power Supply Rejection

Power Supply Rejection indicates the influence of variation of Power supply to the output. It is the ratio of the output change in the full-scale to the Power Supply change.

Pipeline Delay (Latency)

The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every rising edge.

Spurious-Free Dynamic Range

SFDR is defined as the ratio in dB of the RMS value of the signal component to the RMS value of the next largest noise or harmonic distortion component.

Total Harmonic Distortion

THD is the ratio in dB of the RMS sum of the first six harmonic components to the RMS value of the measured input signal.

Typical DC Characterization Curves (AVDD = 3.3 V, DRVDD = 3.3 V, F_S=50MHz (50% Duty Cycle), MODE=AVDD, 2V Input Span from 0.5V to 2.5V, External Reference, unless otherwise noted)

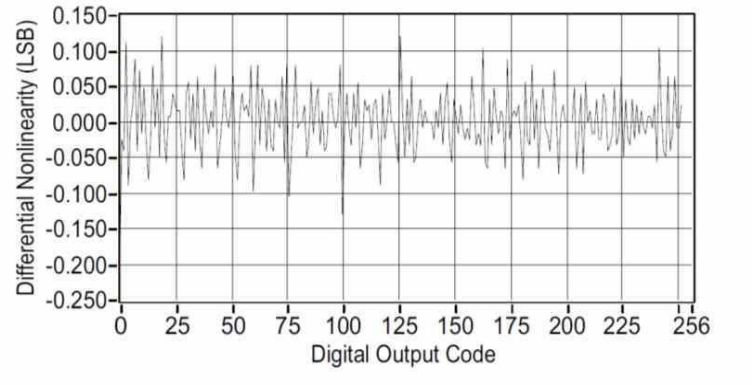


Figure 1. Typical DNL

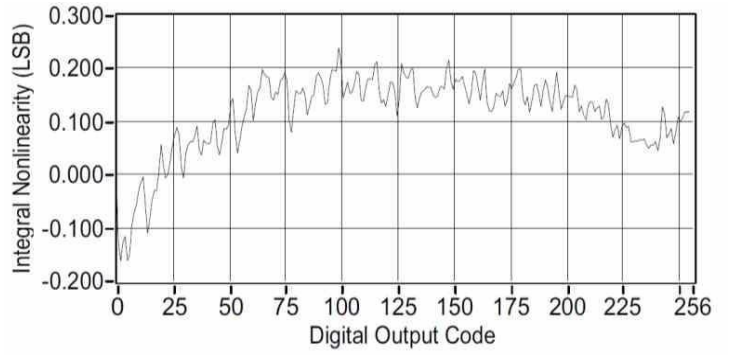


Figure 2. Typical INL

Typical AC Characterization Curves (AVDD = 3.3 V, DRVDD = 3.3 V, F_S=50MHz (50% Duty Cycle), MODE=AVDD, 2V Input Span from 0.5V to 2.5V, External Reference, unless otherwise noted)

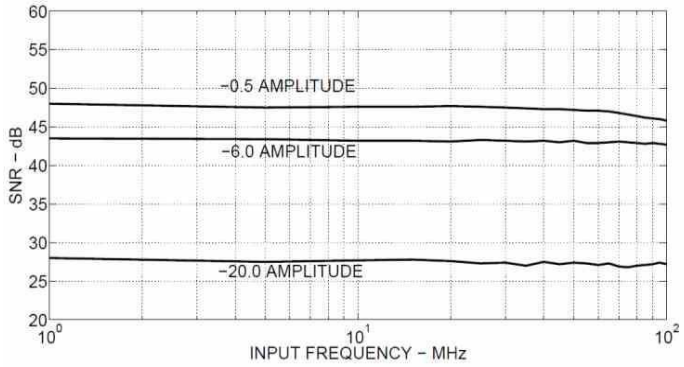


Figure 3. SNR vs. Input Frequency (AVDD and DRVDD=3.3V)

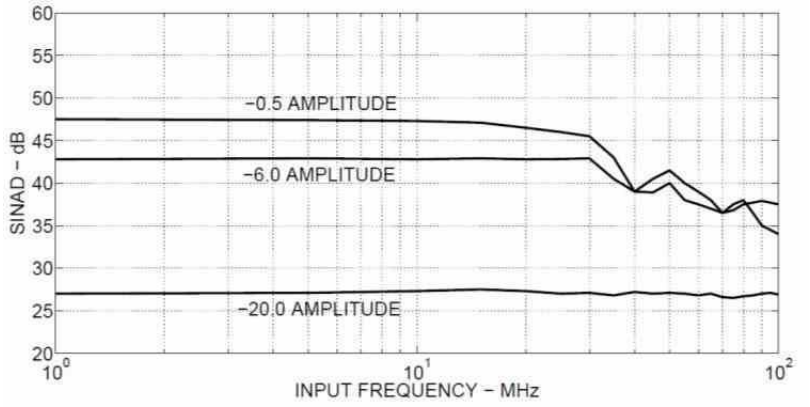


Figure 4. SINAD vs. Input Frequency (AVDD and DVDD=3.3V)

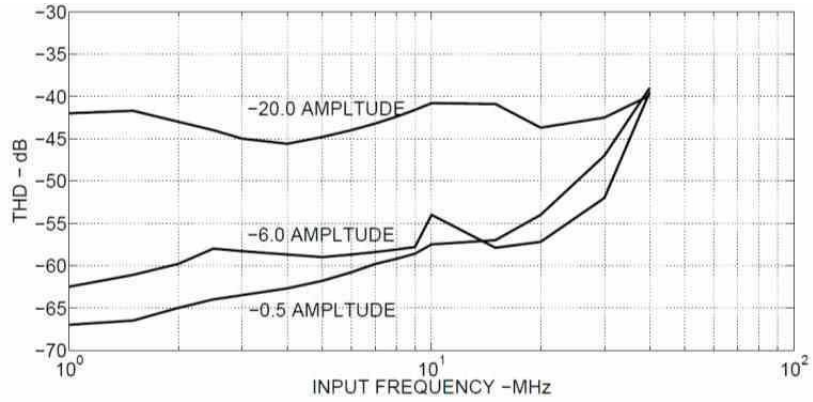


Figure 5. THD vs. Input Frequency (AVDD and DVDD=3.3V)

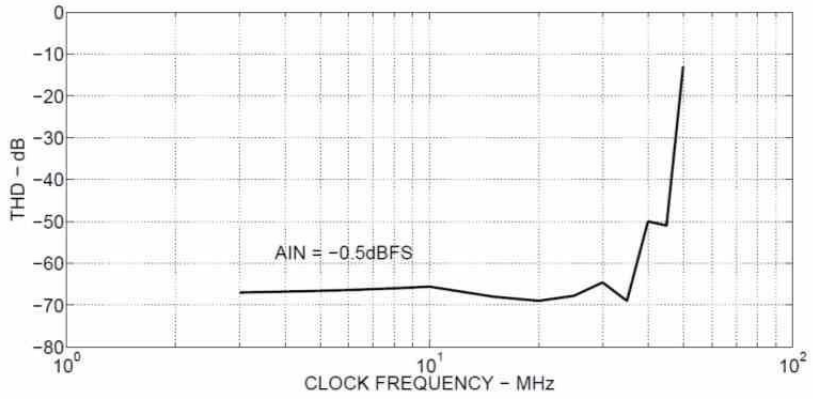


Figure 6. THD vs. Clock Frequency (AVDD and DVDD=3.3V)

FUNCTIONAL DESCRIPTION

The HT9280A implements a pipelined multistage architecture. Each stage has its own sample and hold function and each stage takes one clock period to process one sample. The first stage does the coarsest conversion, while the conversion processed by the second, the third and the fourth stage get finer and finer. It combines the merits of the successive approximation and flash ADCs. This architecture is fast, has a high resolution, and only requires a small die size.

OPERATIONAL MODES

The HT9280A is designed to adapt various applications. By appropriately strapping MODE, REFERENCE, VREF, REFTS, REFBS pins, the HT9280A can be reconfigured for different voltage reference, reference buffer, and analog input modes. The following part summarizes these modes, and Table I describes the various configurations in detail.

TABLE I. Mode Selection

Mode	Input Connect	Input Span	MODE Pin	REFSENSE Pin	VREF	REFTS	REFBS	Figure
TOP/BOTTOM	AIN	1V	AVDD	Short REFSENSE, REFTS and VREF Together			AGND	10
	AIN	2V	AVDD	AGND	Short REFTS and VREF Together		AGND	11
CENTER SPAN	AIN	1V	AVDD/2	Short VREF and REFSENSE Together		AVDD/2	AVDD/2	12
	AIN	2V	AVDD/2	AGND	No Connect	AVDD/2	AVDD/2	
Differential	AIN is Input 1 REFTS and REFBS are Shorted Together for Input 2	1V	AVDD/2	Short VREF and REFSENSE Together		Connect to Input 2		20
		2V	AVDD/2	AGND	No Connect			
External Ref	AIN	2V max	AVDD	AVDD	No Connect	Span = REFTS- REFBS (2V max)		13,14

SUMMARY OF MODES

VOLTAGE REFERENCE

1 V Mode, the internal reference is set to 1 V.
2 V Mode, the internal reference is set to 2 V. **External Divider Mode,** the internal reference is set by external resistors. Note that the voltage must in the range from 1V to 2 V.
External Reference Mode, external references are tied to REFTS, REFBS and VREF pins.

REFERENCE BUFFER

Center Span Mode, shorting REFTS and REFBS together and applying the midscale voltage to that point. The analog input will swing about that midscale point.
Top/Bottom Mode, the REFTS and REFBS pins are tied to the higher and the lower voltage point respectively. The input range is defined by these two points. Note that the two points must in the range from 1 V to 2 V.

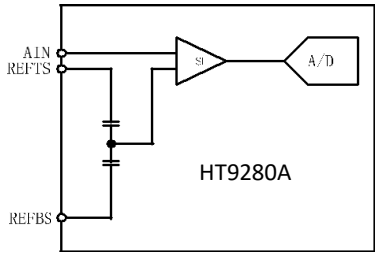


Figure 7. HT9280AEquivalent Functional Input Circuit **ANALOG INPUT**

Differential Mode, shorting REFTS and REFBS pins together and use it as one differential input pin, AIN pin is used as the other differential input pin. Note that this mode is preferred for optimal distortion performance.

Single-Ended, the AIN pin is used as the input pin while the REFTS and REFBS pins are held at a dc points.

Single-Ended/Clamped (AC Coupled), by tying the CLAMPIN to some dc point and applying a pulse to the CLAMP pin, the input may be clamped to some dc level by ac coupling the input.

INPUT AND REFERENCE OVERVIEW

Figure 8 demonstrates the various operating modes mentioned above.
In single-ended input application, the REFTS and REFBS define the maximum and minimum input voltages to the HT9280A,

$$REFBS \le AIN \le REFTS$$

Where, REFBS can be connected to GND and REFTS connected to VREF.
In differential operation, REFTS and REFBS are shorted together, and the input span is set by VREF,

$$(REFTS - VREF/2) \le AIN \le (REFTS + VREF/2)$$

Where, VREF is determined by the internal reference or brought in externally by the user.
When the HT9280Ais working in the 2V mode, the best noise performance may be achieved. While the best distortion performance is achieved when the HT9280A operates in 1 V mode

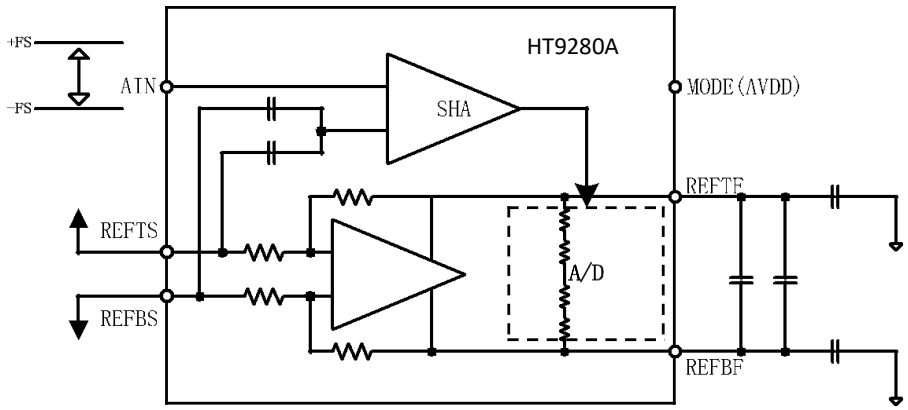
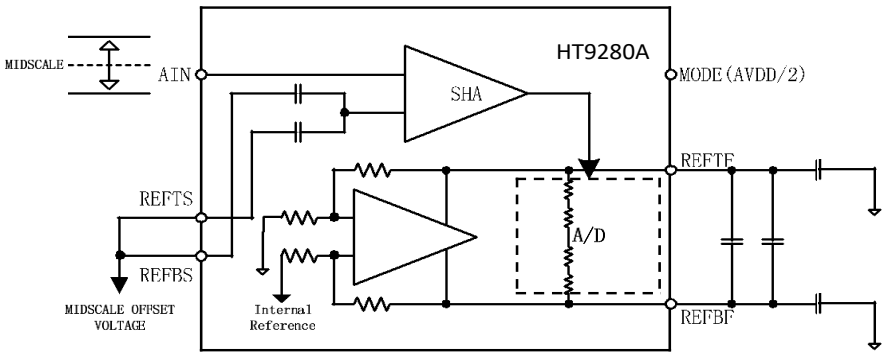


Figure 8a. Top/Bottom Mode



Figture 8b. Center Span Mode

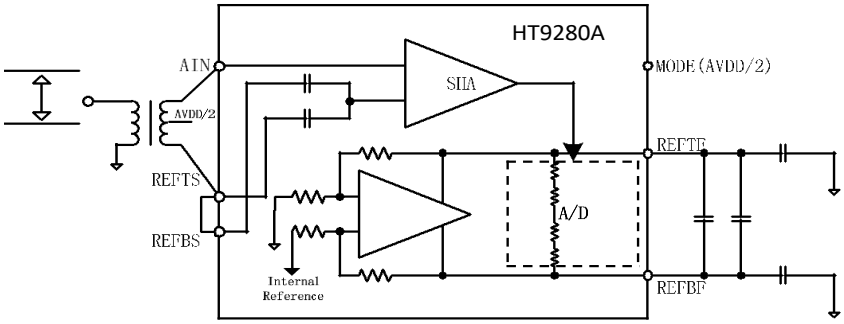
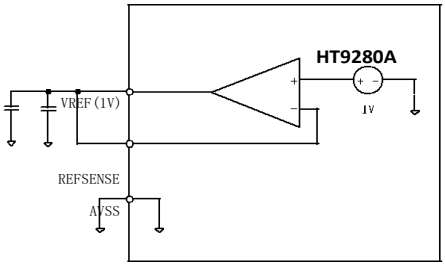
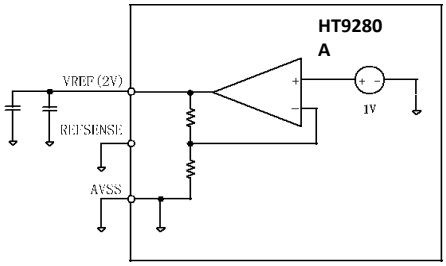


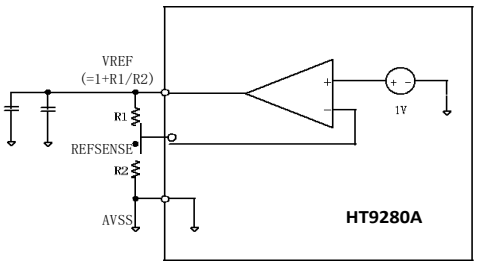
Figure 8c. Differential Mode



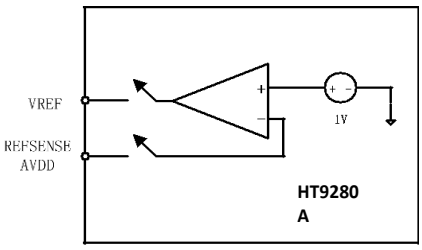
Figture 8d. 1V Reference



Figture 8e. 2V Reference



Figture 8f. Varible Reference



Figture 8g. Internal Reference Disable

REFERENCE OPERATION

The HT9280A has an on-chip bandgap reference. It provides 1 V or 2 V output by a pin-strappable option. Also, an external resistor divider can be connected between VREF, REFSENSE and analog ground to generate a desired reference anywhere between 1 V and 2 V. Furthermore, the user can use an external reference or even bring in top and bottom references, bypassing VREF altogether.

The reference architecture of the HT9280Ais illustrated in figures 8d, 8e and 8f. This shows that HT9280A has great flexibility to match the drive circuit.

In all configurations, the proper decoupling capacitor network (Figure. 9) to REFTF and REFBF is always required because the voltage appearing on REFTF and REFBF are used by the internal circuitry of the HT9280A.

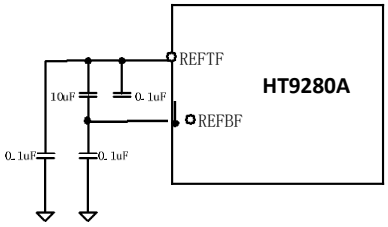


Figure 9. Reference Decoupling Network

INTERNAL REFERENCE OPERATION

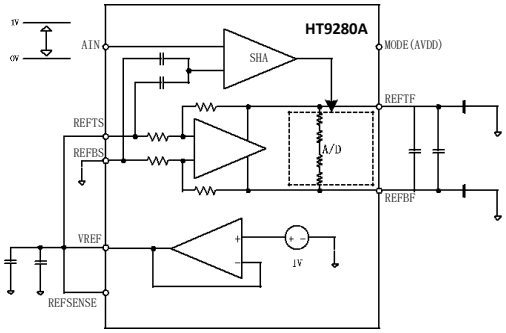


Figure 10. Internal Reference – 1V p-p Input Span (Top/Bottom Mode)

Figure 10 shows the single-ended, top-bottom configuration for 1V p-p operation. In this configuration, REFBS must be grounded. Also, a bypassing network constructed by a 1.0 uF tantalum capacitor in parallel with a low inductance, low ESR, 0.1 uF ceramic capacitor is recommended

Figure 11 shows the single-ended, top-bottom configuration for 2V p-p operation.

Figure 12 shows the single-ended, center-span configuration. To optimize dynamic performance, center the common-mode voltage of the analog input at approximately 1.5 V and connect the shorted REFTS and REFBS inputs to a low impedance 1.5 V source.

Note that the maximum reference drive current is about 0.5 mA and an external buffer may require for heavier loads.

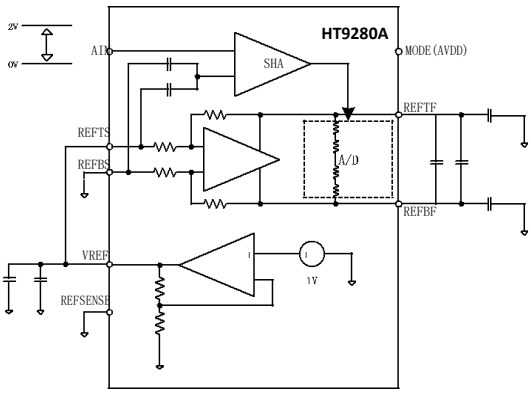


Figure 11. Internal Reference, 2Vp-p Input Span (Top/Bottom Mode)

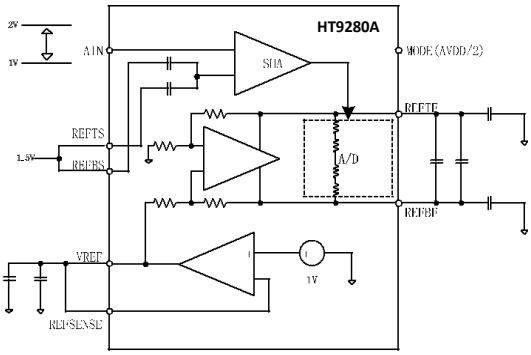


Figure 12. Internal Reference, 1Vp-p Input Span (Center Span Mode)

EXTERNAL REFERENCE OPERATION

The user can disable the internal reference by connecting the REFSENSE pin to VDD. This provides the user more flexibility to improve drift and accuracy by using an external reference.

Figure 13 shows the single-ended, external driving top-bottom configuration for 1 V p-p operation. The built-in reference buffer simplifies the drive requirements of an external reference.

Figure 14 shows the single-ended, external driving center span configuration for 1 V p-p operation.

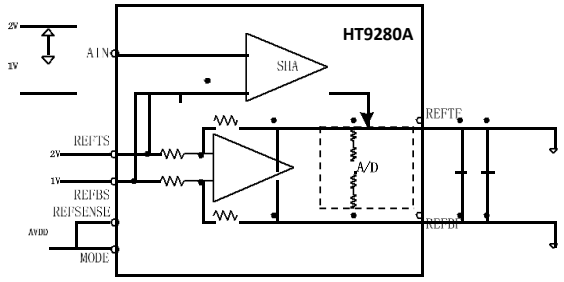


Figure 13. External Reference Mode – 1Vp-p Input Span

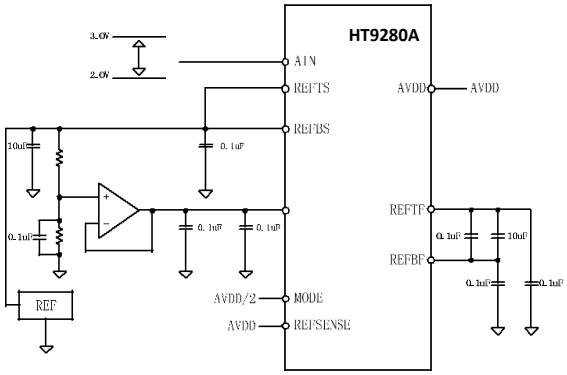


Figure 14. External Reference Mode – 1Vp-p Input Span 2.5VCM

STANDBY OPERATION

The ADC may be placed into a powered down mode by tying the STBY pin to AVDD and holding the clock at logic low. In this mode, the supply current is reduced to less than 0.6mA typically.

The HT9280Atakes approximately several microseconds to power back up

CLAMP OPERATION

Figure 16 shows the internal clamp circuitry and the external control signals needed for clamp operation. For applications in which dc restoration of video or ac coupled signals is required, the input of HT9280A may be clamped to some dc level by tying the CLAMPIN to some dc point and applying a pulse to the CLAMP pin. The allowable clamp voltage range of the HT9280A is between 0.5 volts and 2.0 volts.

To determine the value of the input capacitor, two factors should be taken into account: sufficient acquisition time of the clamp voltage at AIN within the clamping interval and the maximum tolerable deviation from V_C during clamping intervals.

The acquisition time equal:

during clamping intervals. V_C is the difference between the initial input dc level and the clamp voltage supplied attained at the input, only a very small voltage change will be required to correct for droop.

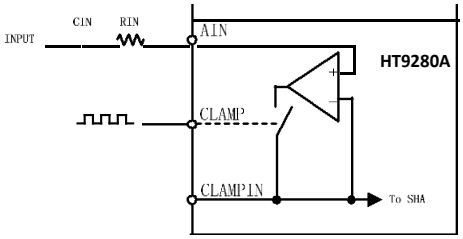


Figure 16a. Clamp Operation

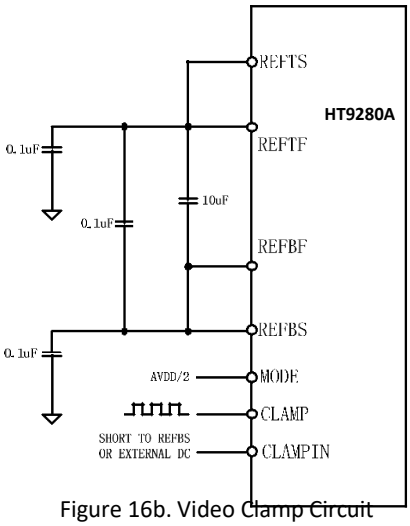


Figure 16b. Video Clamp Circuit

DRIVING THE ANALOG INPUT

Figure 17 shows the equivalent analog input of the HT9280A. In sample mode, Switches 1 and 2 are closed and Switch 3 is opened so that capacitor CH is charged. In hold mode, Switches 1 and 2 are opened and Switch 3 is closed, forcing the output of the op amp to equal the voltage stored on CH.

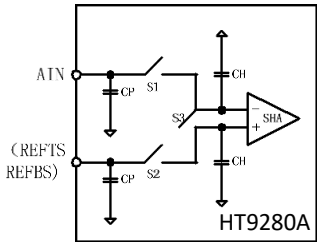


Figure 17. ADC9280 Equivalent Input Structure

The structure of the input SHA places certain speed requirements on the input drive source. Adding series resistance between the output of the source and the AIN pin may ease the drive requirements. The size of this resistor is dependent on the bandwidth of the particular application limits. To maintain the performance outlined in the data sheet specifications, the resistor should be limited to 20 Ω or less.

As mentioned in the Internal and External Reference sections of the data sheet, the input span of the HT9280A is determined by various reference configurations.

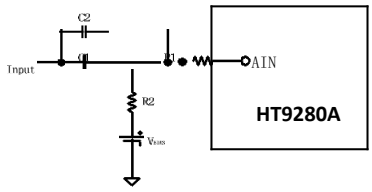


Figure 18. AC Coupled Input

Figure 18 shows a typical configuration for ac-coupling the analog input signal to the HT9280A. Optimal performance requires careful selection of the component values. The most important is the f_3dB

high-pass corner frequency. It is a function of R2 and the parallel combination of C1 and C2. For C1, large electrolytic or tantalum capacitor is recommended. And for C2, ceramic or polystyrene capacitor (on the order of 0.01 uF) is recommended.

For the application in which dc coupling is used, an op amp can be used to level shift a ground-referenced signal to comply with the input requirements of the HT9280A(Figure 19).

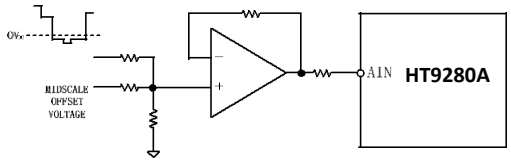


Figure 19. Bipolar Level Shift

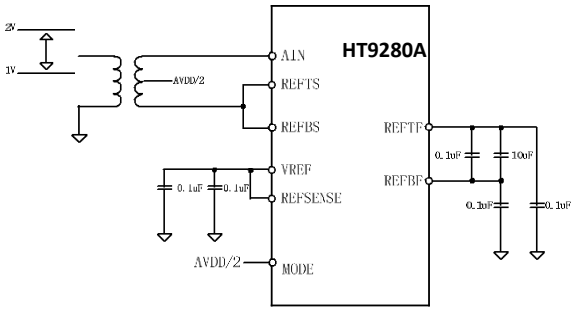


Figure 20. Differential Input

DIFFERENTIAL INPUT OPERATION

The HT9280A will accept differential input signals. This function may be used by shorting REFTS and REFBS and driving them as one leg of the differential signal (the top leg is driven into AIN). In the configuration of differential input, the HT9280A is accepting a 1 V p-p signal. See Figure 20.

DIGITAL INPUTS, OUTPUTS AND CLOCK INPUT

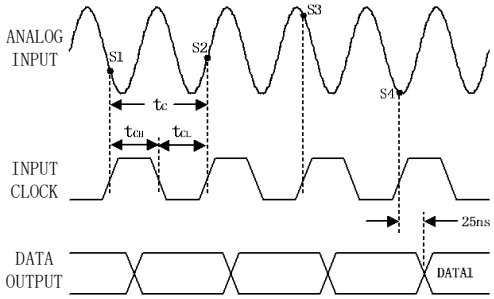


Figure 21. Timing Diagram

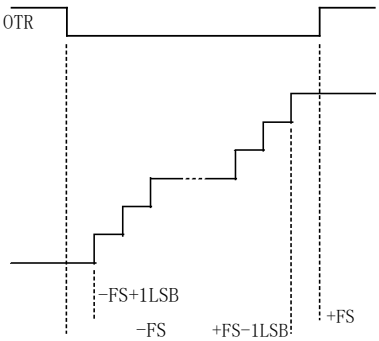


Figure 22. Output Data Format

The HT9280Asupports 3.3V CMOS logic family. All digital signals in the HT9280A are reference to analog ground. The format of the digital output is straight binary (see Figure 22). For the clock input, high speed or advanced CMOS (HC/HCT, AC/ACT) logic family is recommended. The HT9280A operates on both rising and falling edges of the input clock. Note that the HT9280A supports a conversion rate of up to 50 MSPS. And running the part at slightly faster clock rates may reduce the performance and increase the power consumption. Conversely, running the part at slower clock rates may slightly increase the performance and decrease the power consumption.

APPLICATION INFORMATION

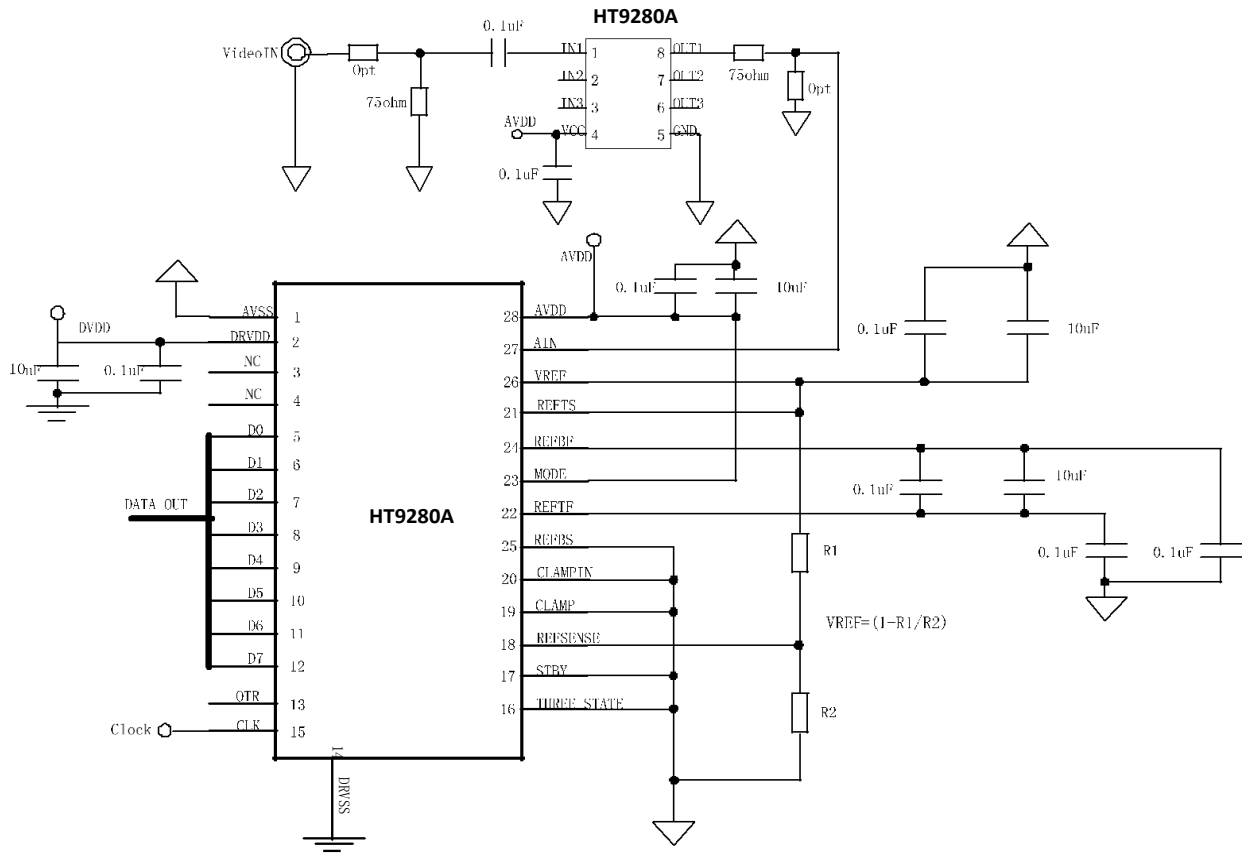


Figure 23. Variable Reference Application Schematic

MECHINAL DATA

28-LEAD SHRINK SMALL OUTLINE PACKAGE (SSOP28)

DIMENSIONS			
REF.	mm		
	MIN.	TYP.	MAX.
A	1.70	-	2.00
A1	0.05	-	0.15
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	9.90	10.20	10.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e	0.65BSC		
θ	0°	-	8°
L	0.55	-	0.95

SSOP28

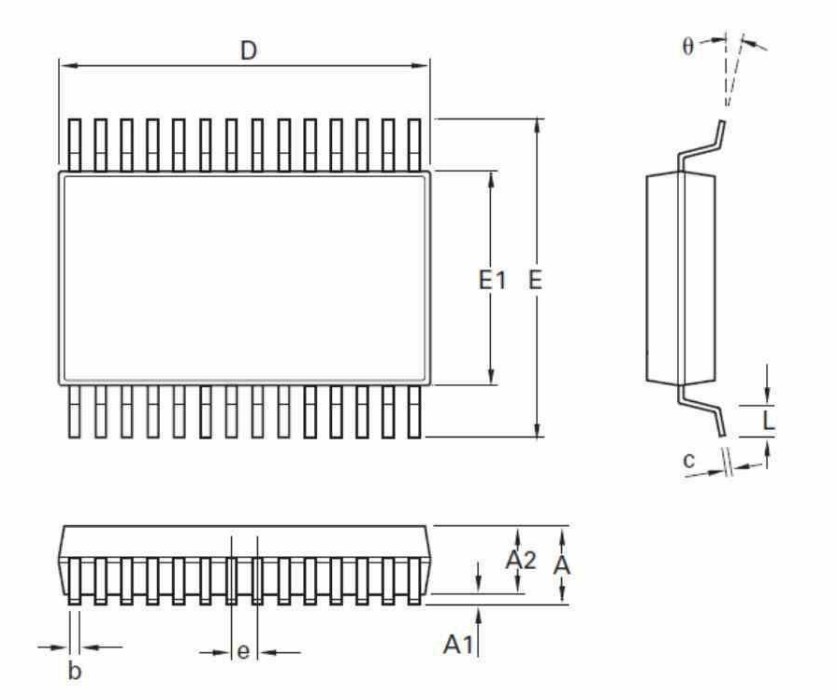


Figure 24. Package Outline

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