

### Description

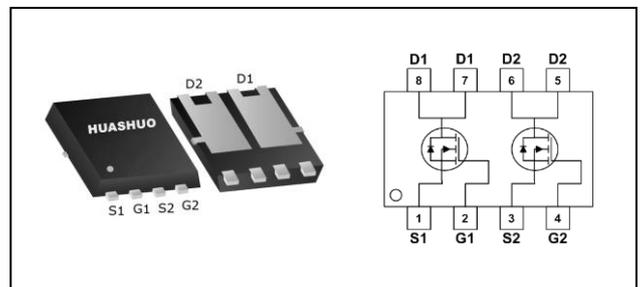
The HSBA0204 is the high cell density trench N-ch MOSFETs, which provides excellent RDS(ON) and efficiency for most of the small power switching and load switch applications. The HSBA0204 meets the RoHS and Green Product requirement with full function reliability approved.

- Portable Equipment
- Battery Powered Systems
- Hard Switching and High-Speed Circuit
- Advanced high cell density Trench technology

### Product Summary

V <sub>DS</sub>	100	V
R <sub>DS(ON),max</sub>	112	mΩ
I <sub>D</sub>	9.3	A

### PRPAK5\*6 Pin Configuration



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	100	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	9.3	A
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	5.9	A
I <sub>D</sub> @T <sub>A</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	2.9	A
I <sub>D</sub> @T <sub>A</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	1.8	A
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	36	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	6.1	mJ
I <sub>AS</sub>	Avalanche Current	11	A
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>3</sup>	21	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C

### Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R <sub>θJA</sub>	Thermal Resistance Junction-ambient <sup>1</sup>	---	63	°C/W
R <sub>θJC</sub>	Thermal Resistance Junction-Case <sup>1</sup>	---	6	°C/W

**Electrical Characteristics ( $T_J=25\text{ }^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=3A$	---	90	112	$m\Omega$
		$V_{GS}=4.5V, I_D=2A$	---	95	120	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.7	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.57	---	$mV/^\circ C$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V, T_J=25^\circ C$	---	---	1	$\mu A$
		$V_{DS}=80V, V_{GS}=0V, T_J=55^\circ C$	---	---	10	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V, I_D=2A$	---	12	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	2	---	$\Omega$
$Q_g$	Total Gate Charge (10V)	$V_{DS}=60V, V_{GS}=10V, I_D=2A$	---	19.5	---	nC
$Q_{gs}$	Gate-Source Charge		---	3.2	---	
$Q_{gd}$	Gate-Drain Charge		---	3.6	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=50V, V_{GS}=10V, R_G=3.3\Omega$ $I_D=1A$	---	16.2	---	ns
$T_r$	Rise Time		---	3	---	
$T_{d(off)}$	Turn-Off Delay Time		---	44	---	
$T_f$	Fall Time		---	2.6	---	
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	---	1535	---	pF
$C_{oss}$	Output Capacitance		---	60	---	
$C_{rss}$	Reverse Transfer Capacitance		---	37.4	---	

**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V, \text{ Force Current}$	---	---	9	A
$I_{SM}$	Pulsed Source Current <sup>2,5</sup>		---	---	18	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^\circ C$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=11A$
- 4.The power dissipation is limited by 175 $^\circ C$  junction temperature
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.



Typical Characteristics

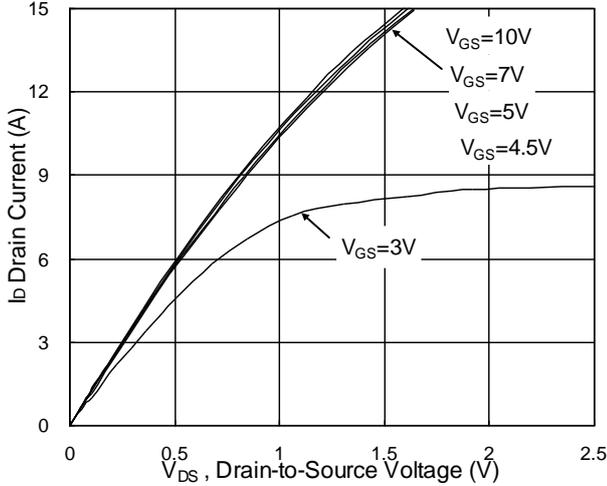


Fig.1 Typical Output Characteristics

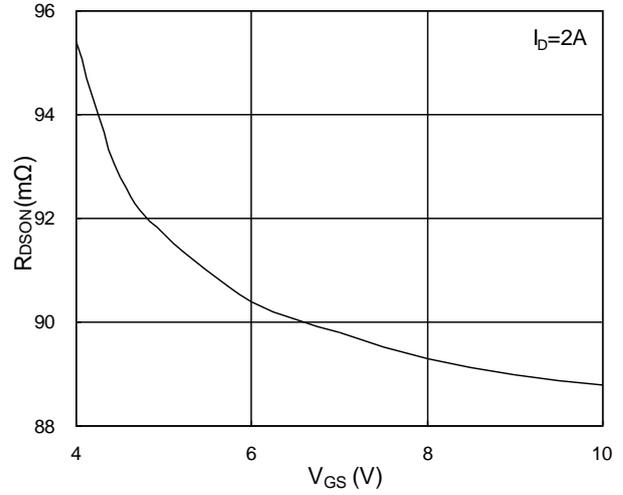


Fig.2 On-Resistance vs. Gate-Source

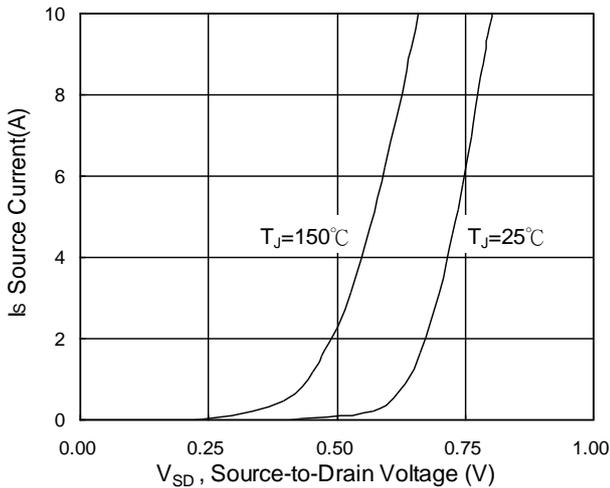


Fig.3 Forward Characteristics Of Reverse

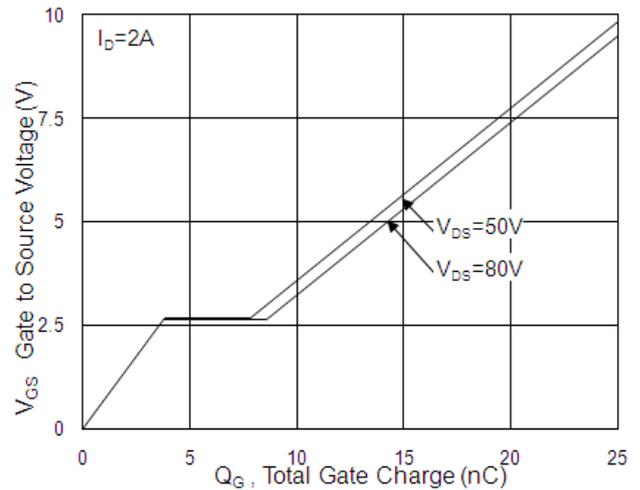


Fig.4 Gate-Charge Characteristics

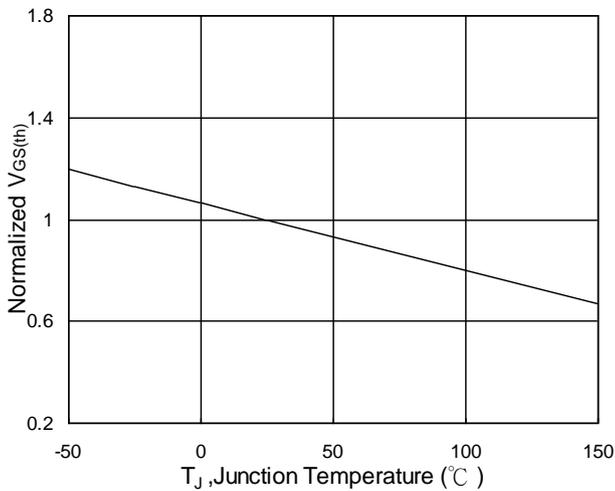


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

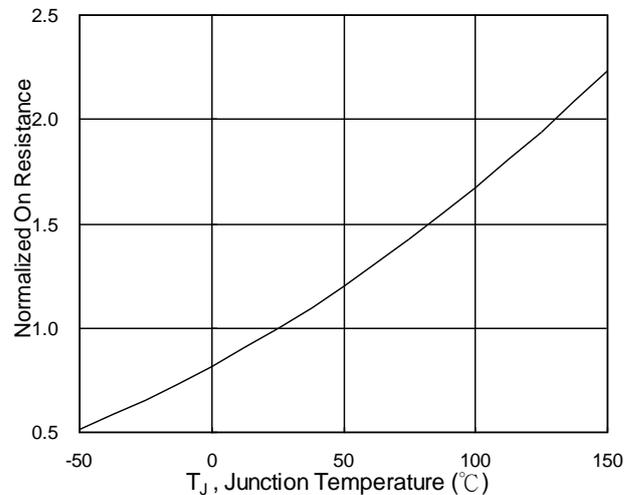
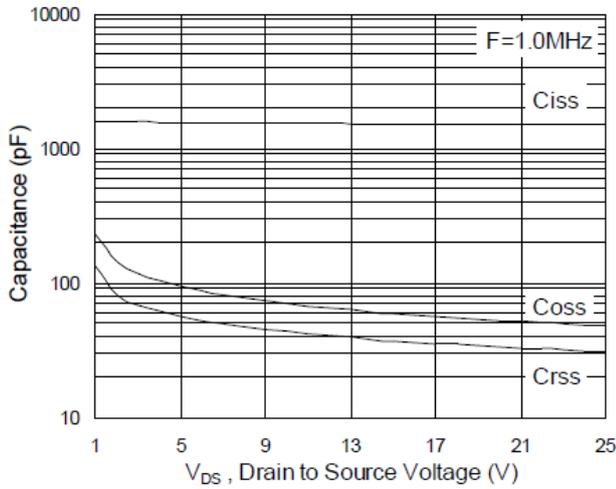


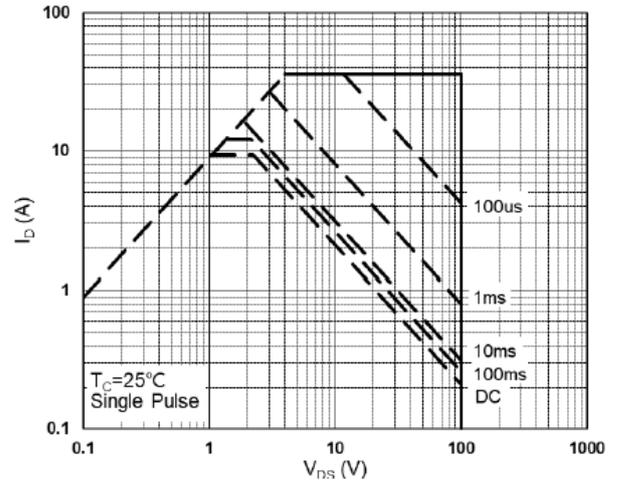
Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$



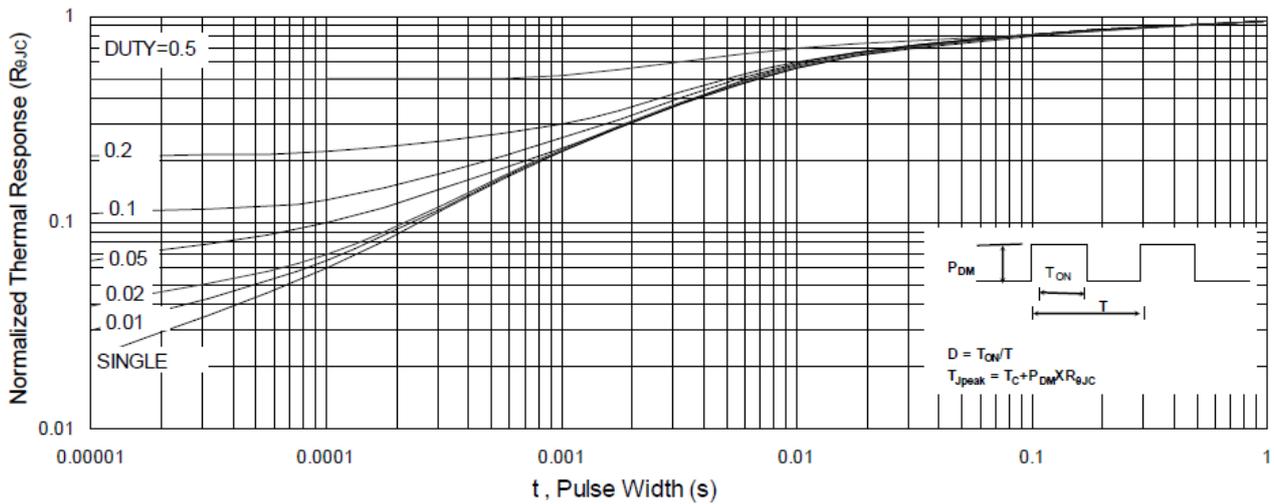
**Dual N-Ch 100V Fast Switching MOSFETs**



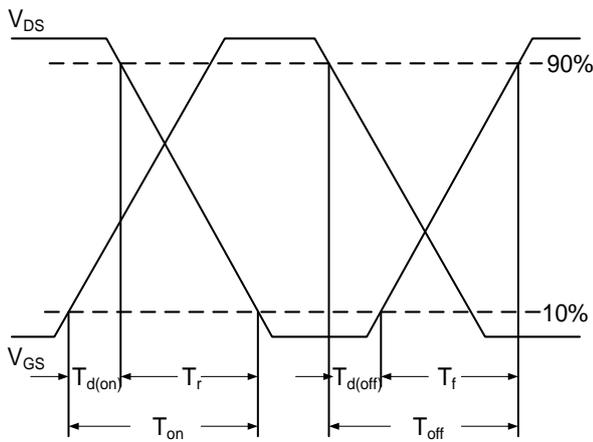
**Fig.7 Capacitance**



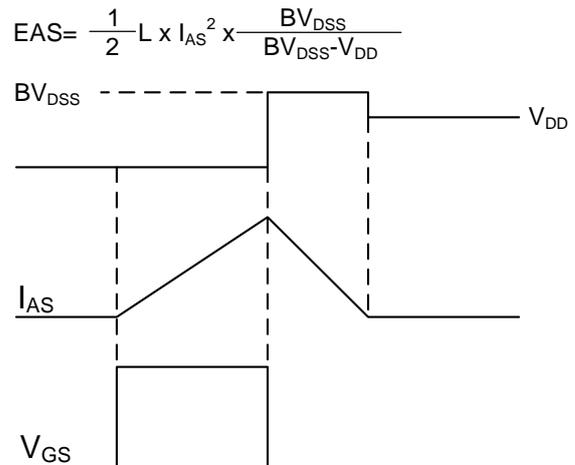
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**

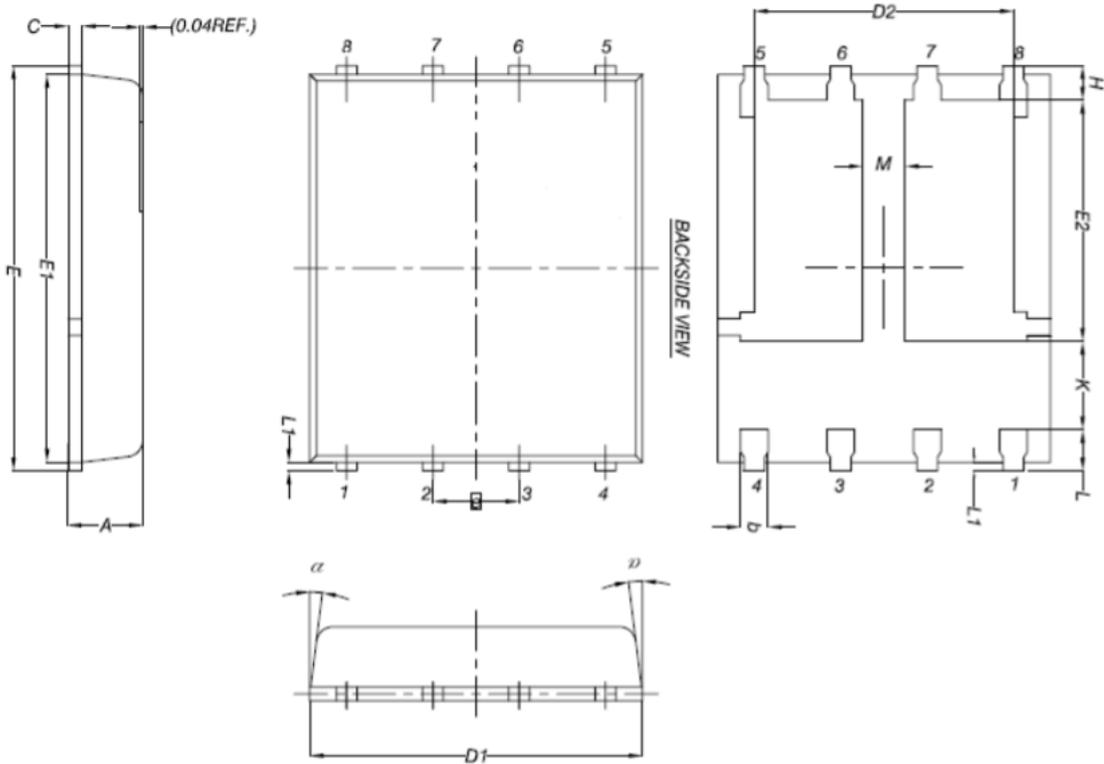


**Fig.11 Unclamped Inductive Switching**

$$EAS = \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



## PRPAK5x6-8L Dual EP2 Package Outline



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.17	0.035	0.046
b	0.33	0.51	0.013	0.020
C	0.20	0.30	0.008	0.012
D1	4.80	5.20	0.189	0.205
D2	3.61	3.96	0.142	0.156
E	5.90	6.15	0.232	0.242
E1	5.70	5.85	0.224	0.230
E2	3.30	3.78	0.130	0.149
e	1.27 BSC		0.05 BSC	
H	0.38	0.61	0.015	0.024
K	1.10	---	0.043	---
L	0.38	0.61	0.015	0.024
L1	0.05	0.25	0.002	0.010
M	0.50	---	0.020	---
$\alpha$	0°	12°	0°	12°

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