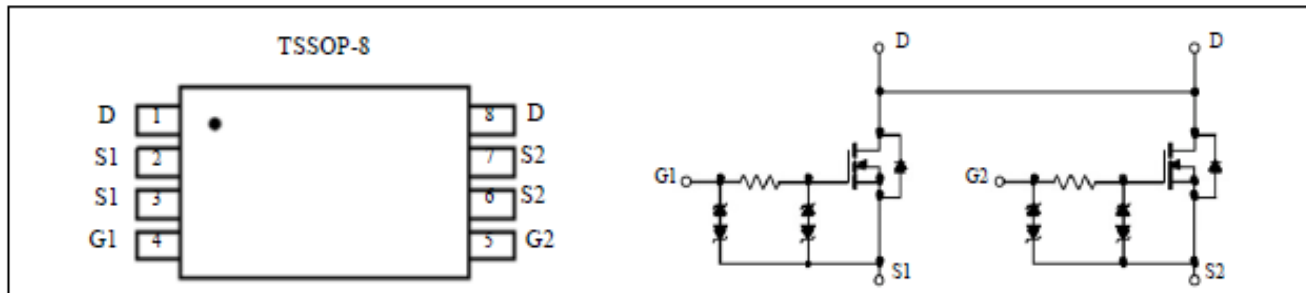


## Dual N-Channel High Density Trench MOSFET

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(on)</sub> (mΩ) Max
20V	6.5A	20 @ V <sub>GS</sub> = 4.5V
	5.5A	28 @ V <sub>GS</sub> = 2.5V

### FEATURES

- Super high dense cell trench design for low R<sub>DS(on)</sub>.
- Rugged and reliable.
- Battery Switch, ESD Protected 2KV.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	±12	V
Drain Current-Continuous <sup>a</sup> @ T <sub>A</sub> = 25 °C -Pulse <sup>b</sup>	I <sub>D</sub>	6.5	A
	I <sub>DM</sub>	30	A
Drain-Source Diode Forward Current <sup>a</sup>	I <sub>S</sub>	1.7	A
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> =25 °C	1.5
		T <sub>A</sub> =75 °C	0.96
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	- 55 to 150	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	83	°C/W
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Note :  
a. Surface Mounted on FR4 Board , t ≤ 10sec.  
b. Pulse width limited by maximum junction temperature.



**ELECTRICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20V, V_{GS} = 0V$			1	$\mu A$
Gate-Body Leakage	$I_{GSS}$	$V_{GS} = \pm 12V, V_{DS} = 0V$			$\pm 10$	$\mu A$
<b>ON CHARACTERISTICS</b> <sup>b</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.6	0.8	1.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 6.5A$		17	20	m $\Omega$
		$V_{GS} = 2.5V, I_D = 5.5A$		22	28	
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b> <sup>b</sup>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_S = 1.5A$			1.2	V
<b>DYNAMIC CHARACTERISTICS</b> <sup>c</sup>						
Input Capacitance	$C_{ISS}$	$V_{DS} = 10V, V_{GS} = 0V, f = 1.0MHz$		318		pF
Output Capacitance	$C_{OSS}$			103		pF
Reverse Transfer Capacitance	$C_{RSS}$			22		pF
<b>SWITCHING CHARACTERISTICS</b> <sup>c</sup>						
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = 10V, I_D = 2A$ $V_{GEN} = 4.5V$ $R_L = 5\Omega$ $R_{GEN} = 6\Omega$		304		ns
Rise Time	$t_r$			720		ns
Turn-Off Delay Time	$t_{D(OFF)}$			3480		ns
Fall Time	$t_f$			2140		ns
Total Gate Charge	$Q_g$	$V_{DS} = 12V, I_D = 6A$ $V_{GS} = 4.5V$		4.6		nC
Gate-Source Charge	$Q_{gs}$			2.7		nC
Gate-Drain Charge	$Q_{gd}$			1.6		nC

Note :  
b. Pulse Test : Pulse width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .  
c. Guaranteed by design, not subject to production testing.

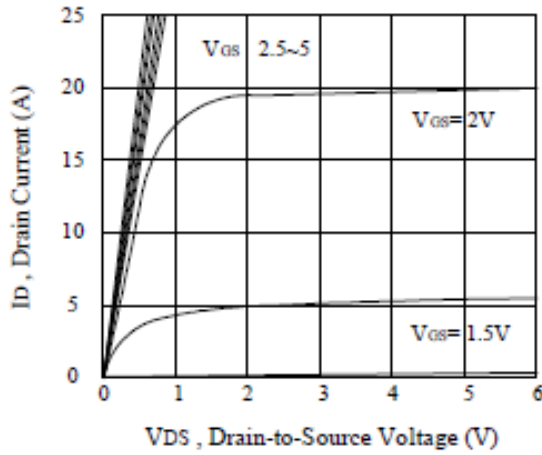


Figure 1. Output Characteristics

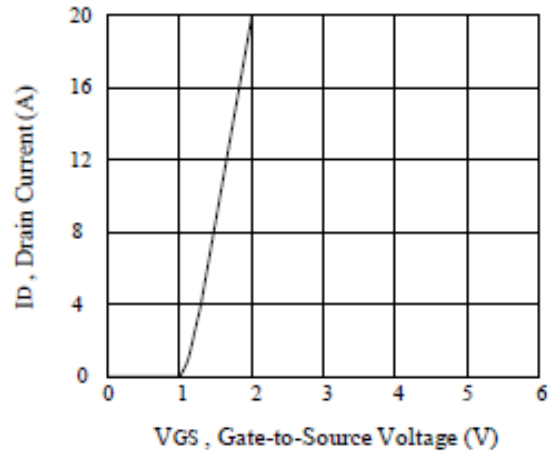


Figure 2. Transfer Characteristics

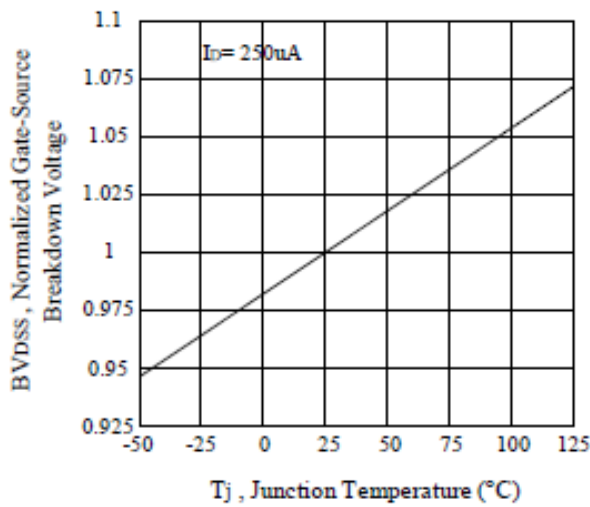


Figure 3. Breakdown Voltage Variation with

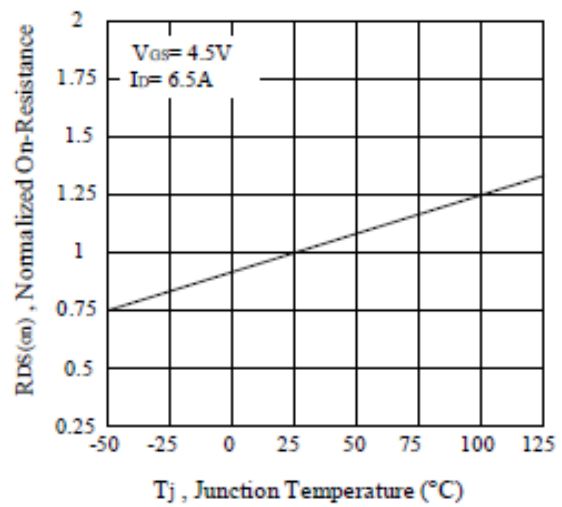


Figure 4. On-Resistance Variation with Temperature

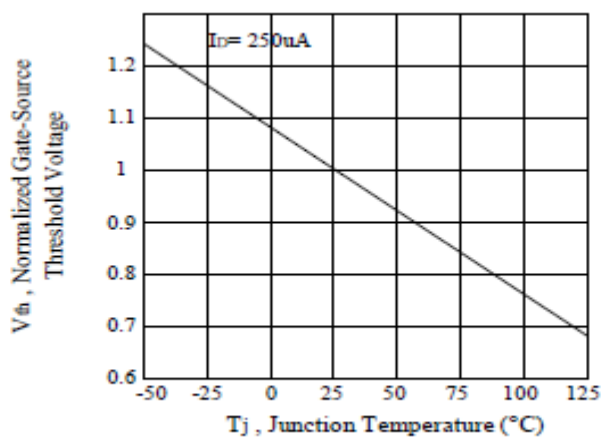


Figure 5. Gate Threshold Variation with Temperature

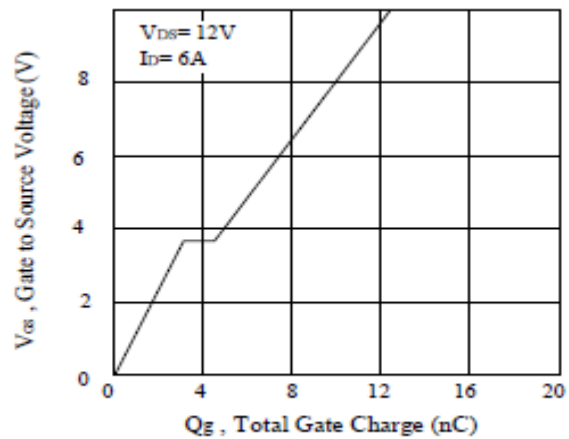
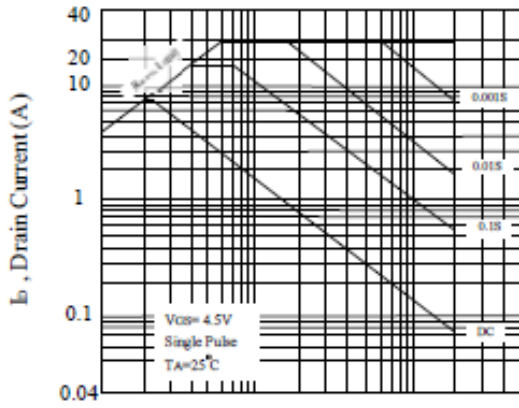
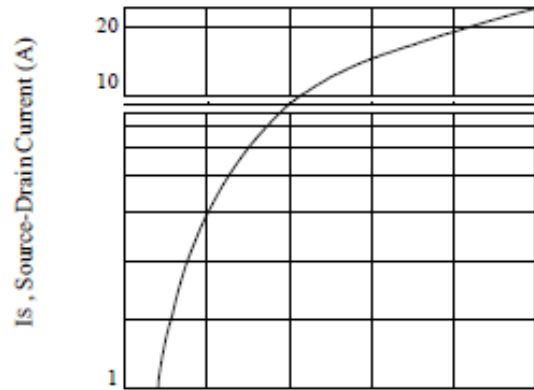


Figure 6. Gate Charge



VDS, Drain-Source Voltage (V)  
Figure 7. Maximum Safe Operating Area



VSD, Body Diode Forward Voltage (V)  
Figure 8. Body Diode Forward Voltage Variation with Source Current

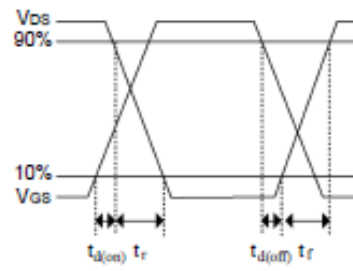
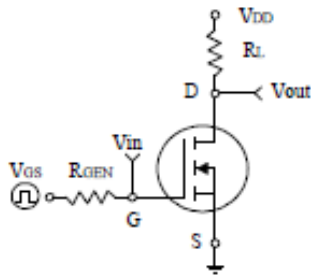


Figure 9. Switching Test Circuit and Switching Waveforms

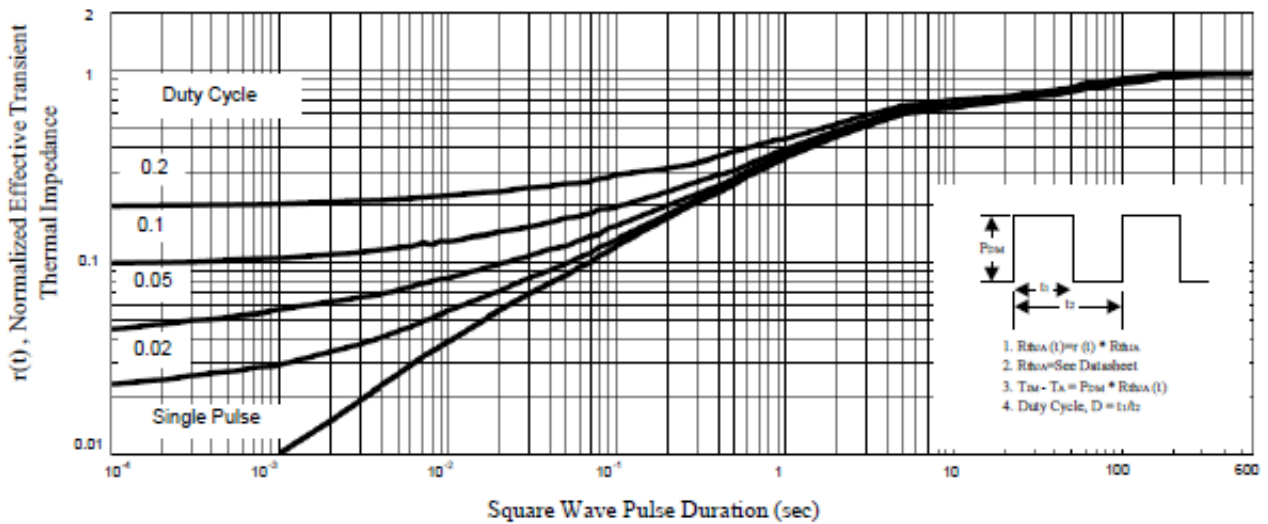


Figure 10. Normalized Thermal Transient Impedance Curve

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