

## Dual N-ch 20V Fast Switching MOSFETs

### Description

The HSO8810 is the low R<sub>DS(on)</sub> trenched N-CH MOSFETs with robust ESD protection. This product is suitable for Lithium-ion battery pack applications.

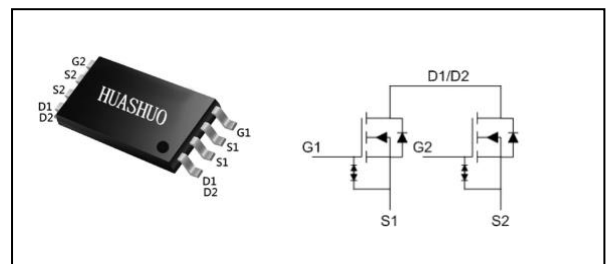
The HSO8810 meet the RoHS and Green Product requirement with full function reliability approved.

- Green Device Available
- Super Low Gate Charge
- Excellent C<sub>dv/dt</sub> effect decline
- Advanced high cell density Trench technology

### Product Summary

V <sub>DS</sub>	20	V
R <sub>DS(ON),typ</sub>	11.5	mΩ
I <sub>D</sub>	7.3	A

### TSSOP8 Pin Configuration



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	20	V
V <sub>GS</sub>	Gate-Source Voltage	± 12	V
I <sub>D</sub> @T <sub>A</sub> =25°C	Continuous Drain Current <sub>1</sub>	7.3	A
I <sub>D</sub> @T <sub>A</sub> =70°C	Continuous Drain Current <sub>1</sub>	5.8	A
I <sub>DM</sub>	Pulsed Drain Current <sub>2</sub>	30	A
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation <sub>3</sub>	2	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C

### Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R <sub>θJA</sub>	Thermal Resistance Junction-ambient <sub>1</sub>	---	62.5	°C/W



**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	20	---	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =3.5A	---	11.5	15	mΩ
		V <sub>GS</sub> =4.0V, I <sub>D</sub> =3.5A	---	12.5	16	
		V <sub>GS</sub> =3.7V, I <sub>D</sub> =3.5A	---	13.5	17	
		V <sub>GS</sub> =3.1V, I <sub>D</sub> =3.5A	---	14	17.5	
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =3.5A	---	14.5	18	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	0.5	---	1.0	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =16V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±8V, V <sub>DS</sub> =0V	---	---	±10	uA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =3.5A	---	21	---	S
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =15V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =7A	---	11.2	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	1.6	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	2.9	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =10V, V <sub>GS</sub> =4.5V, R <sub>G</sub> =3Ω I <sub>D</sub> =3.5A	---	30	---	ns
T <sub>r</sub>	Rise Time		---	250	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	450	---	
T <sub>f</sub>	Fall Time		---	700	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	850	---	pF
C <sub>oss</sub>	Output Capacitance		---	81	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	70	---	

**Diode Characteristics**

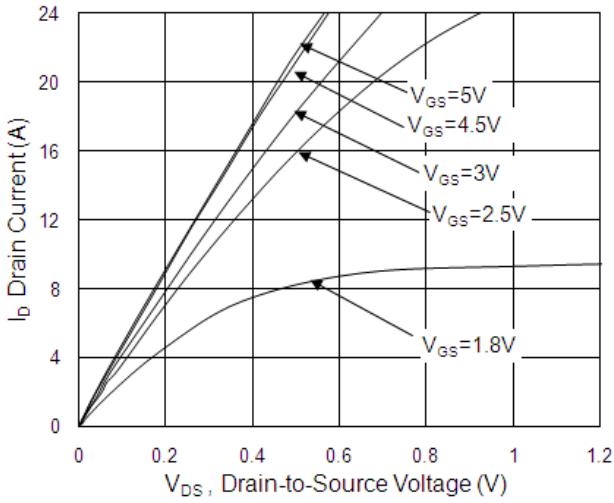
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Continuous Source Current <sup>1,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	7.3	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	---	---	1.2	V

Note :

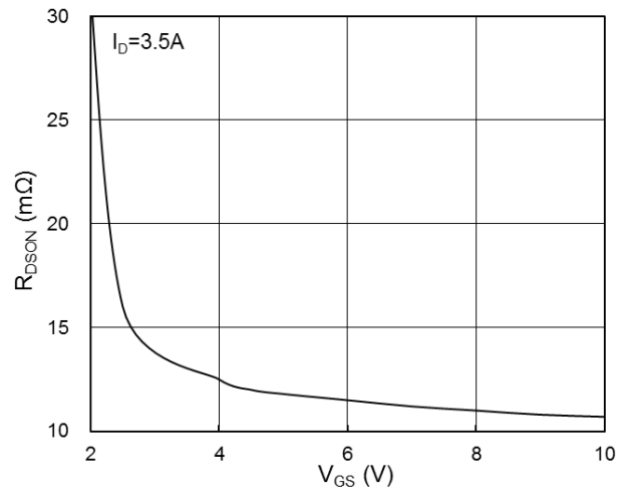
- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.



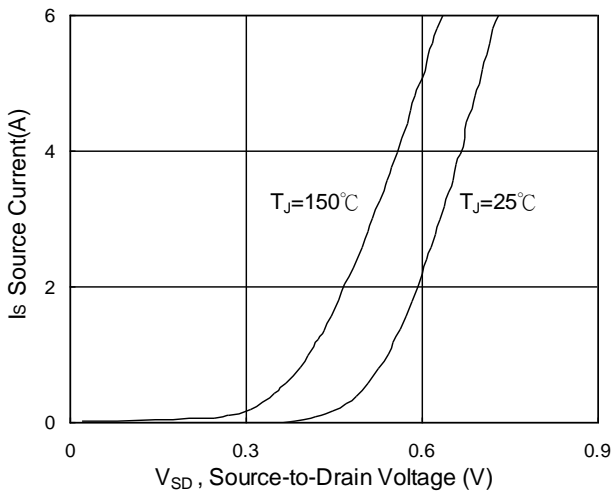
### Typical Characteristics



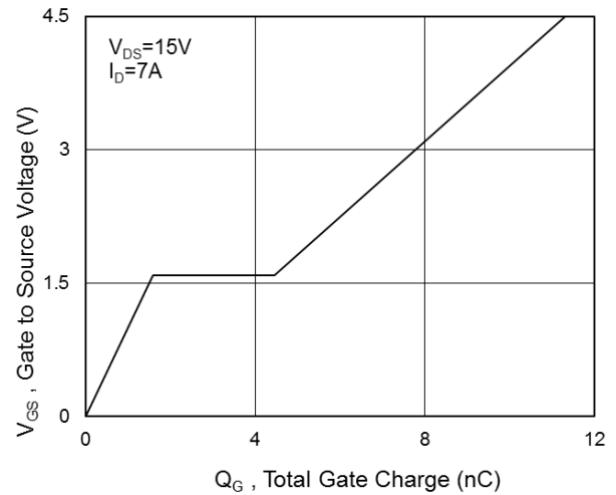
**Fig.1 Typical Output Characteristics**



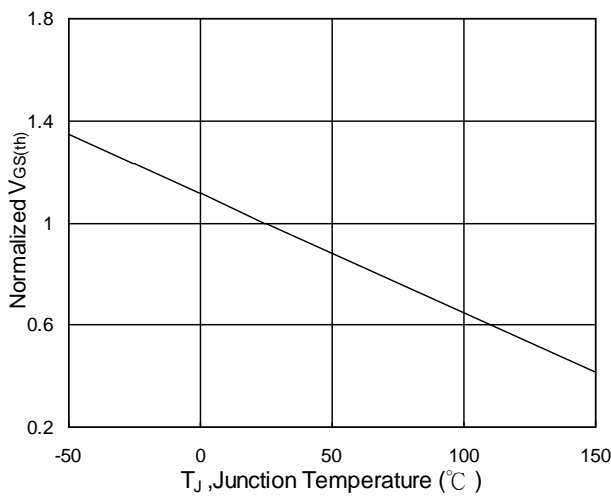
**Fig.2 On-Resistance vs. Gate-Source**



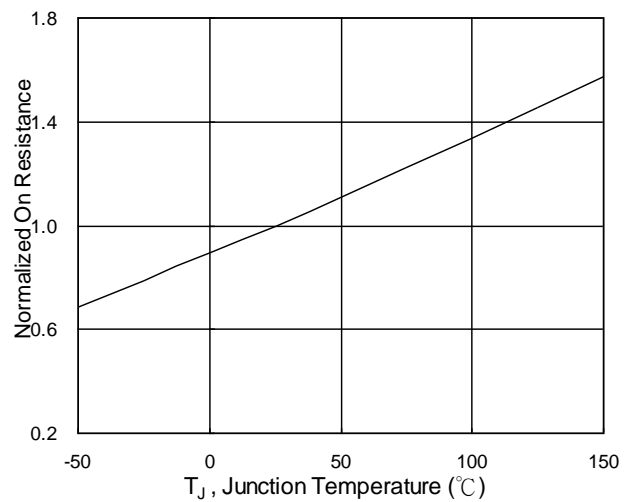
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**



**Fig.5 V<sub>GS(th)</sub> vs. T<sub>J</sub>**



**Fig.6 Normalized R<sub>DS(on)</sub> vs. T<sub>J</sub>**



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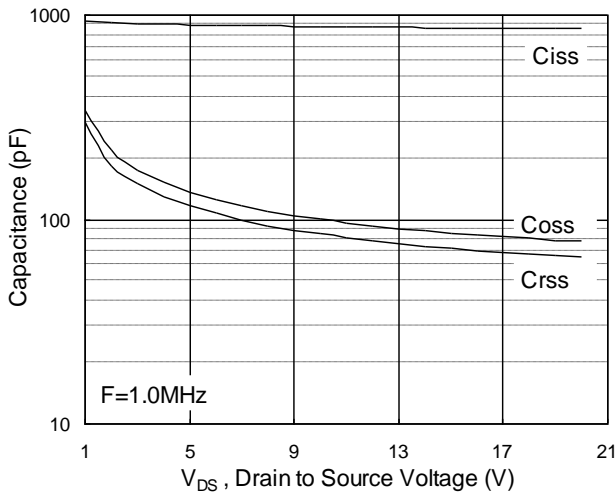


Fig.7 Capacitance

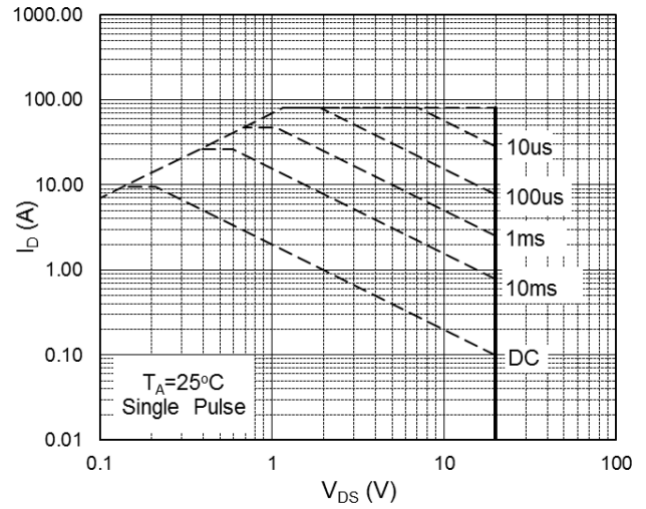


Fig.8 Safe Operating Area

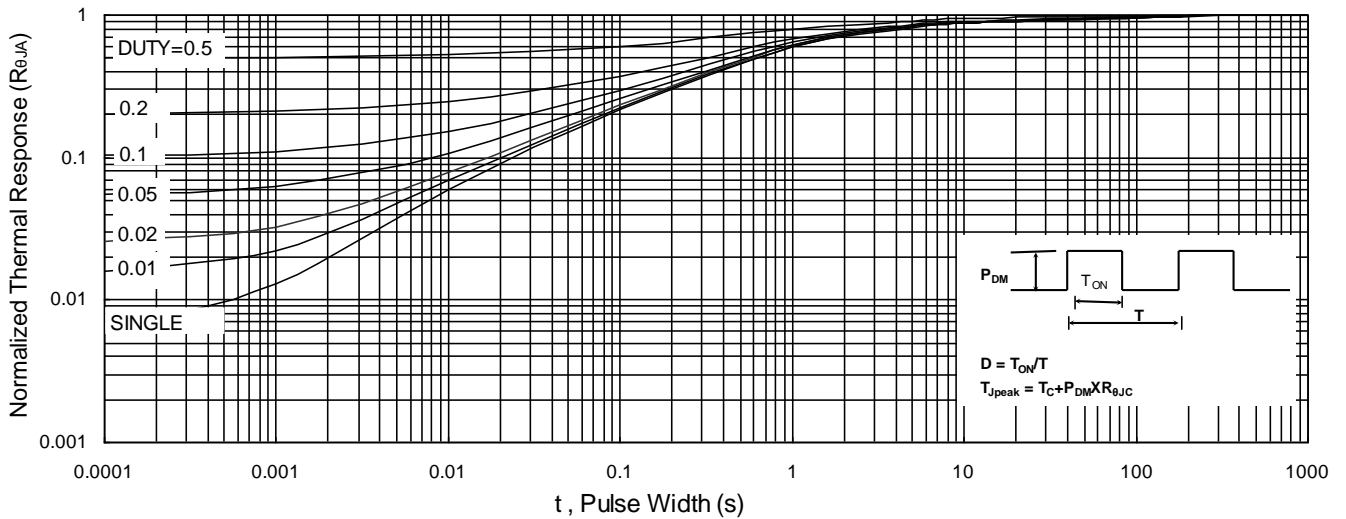


Fig.9 Normalized Maximum Transient Thermal Impedance

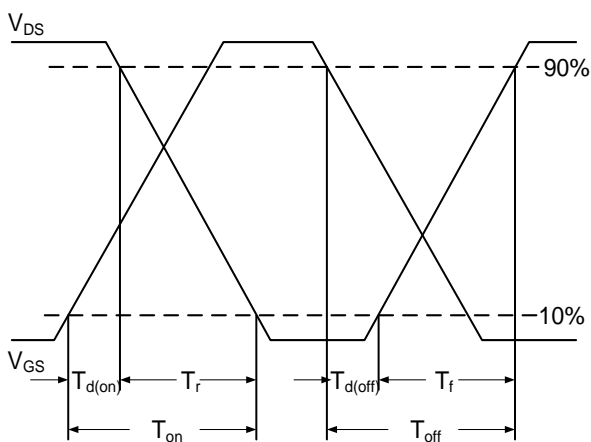


Fig.10 Switching Time Waveform

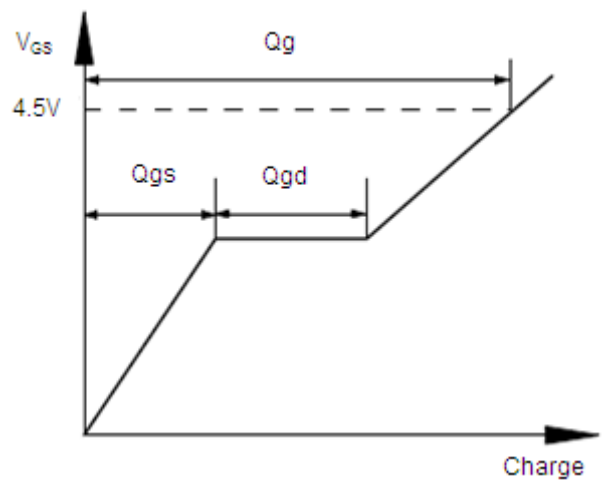
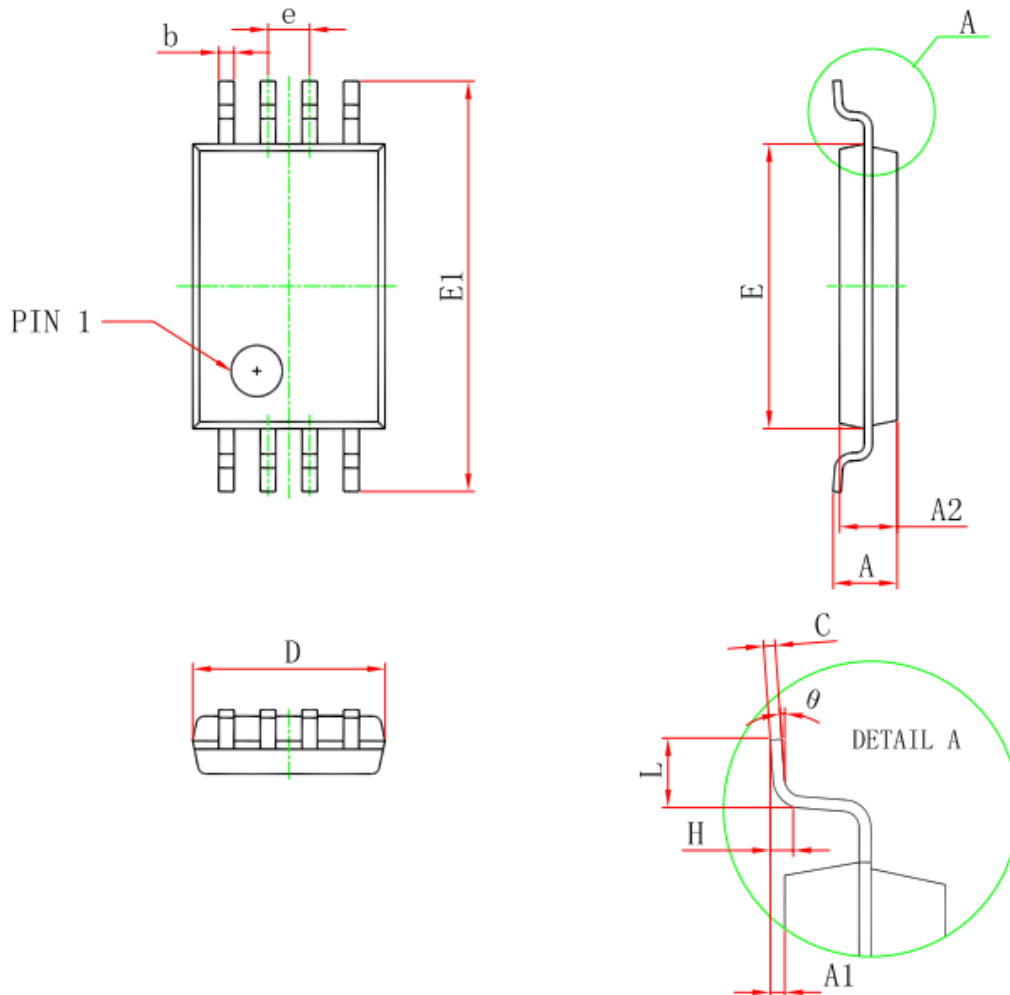


Fig.11 Gate Charge Waveform



## TSSOP8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
e	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
theta	1°	7°	1°	7°

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