

Description

HSP8N50 is Fortunatus high voltage MOSFET family based on advanced planar stripe DMOS technology. This advanced MOSFET family has optimized on-state resistance, and also provides superior switching performance and higher avalanche energy strength. This device family is suitable for high efficiency switch mode power supplies.

- High Efficiency
- 100% EAS Guaranteed
- Improved dv/dt, di/dt capability
- Green Device
- Low Crss(typical 10pF)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	500	V
V _{GS}	Gate-Source Voltage	±30	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ₁	8	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ₁	5.1	A
I _{DM}	Pulsed Drain Current ₂	32	A
Dv/dt	Peak Diode Recovery dv/dt (Note3)	3.5	V/ns
EAS	Single Pulse Avalanche Energy ₃	320	mJ
P _D @T _C =25°C	Total Power Dissipation ₄	142	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

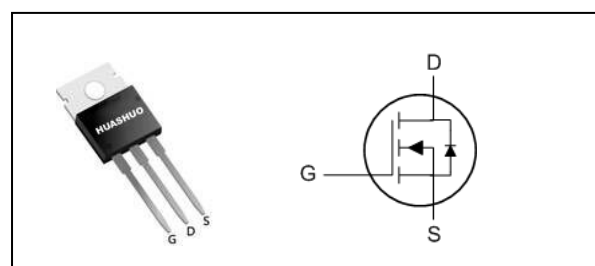
Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ₁	---	62.5	°C/W
R _{θJC}	Thermal Resistance Junction-Case ₁	---	0.88	°C/W

Product Summary

V _{DS}	500	V
R _{DS(ON),typ}	850	mΩ
I _D	8	A

TO220 Pin Configuration



Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	500	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.0193	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =4A	---	---	850	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	2	---	4	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-3.97	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =500V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =400V, V _{GS} =0V, T _J =125°C	---	---	100	
G _{fs}	Forward Transconductance (Note4)	V _{DS} =50V, I _D =4A	---	7.2	---	S
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±30V, V _{DS} =0V	---	---	±100	nA
Q _g	Total Gate Charge (4.5V)	V _{DD} =400V, V _{GS} =10V, I _D =8A	---	23	---	nC
Q _{gs}	Gate-Source Charge		---	6.2	---	
Q _{gd}	Gate-Drain Charge		---	11	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =250V, V _{GS} =10V, R _G =10Ω I _D =8A	---	24	---	ns
T _r	Rise Time		---	16	---	
T _{d(off)}	Turn-Off Delay Time		---	40	---	
T _f	Fall Time		---	16	---	
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz	---	980	---	pF
C _{oss}	Output Capacitance		---	110	---	
C _{rss}	Reverse Transfer Capacitance		---	10	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	8	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	32	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.4	V
t _{rr}	Reverse Recovery Time	I _F =8A, dI/dt=100A/μs, T _J =25°C	---	360	---	nS
Q _{rr}	Reverse Recovery Charge		---	3.5	---	nC



Typical Characteristics

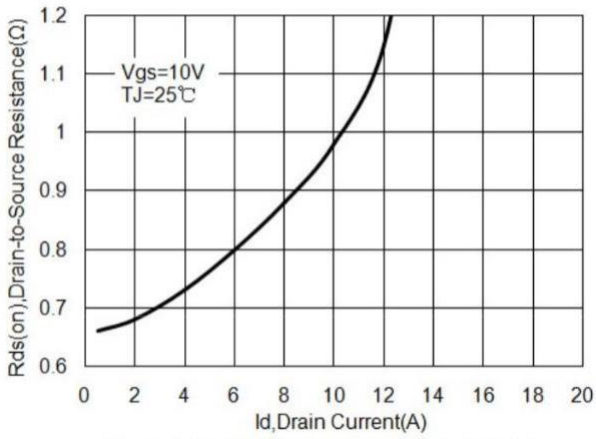
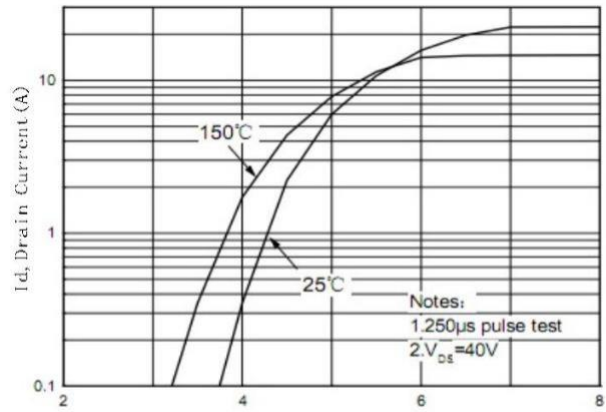
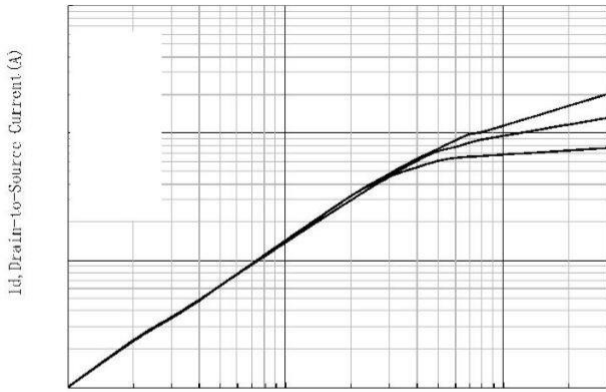
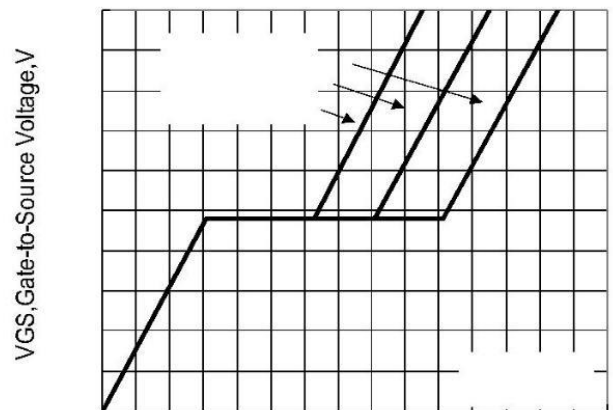
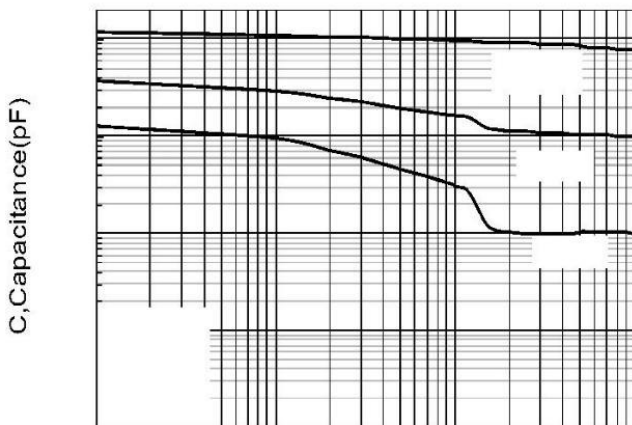
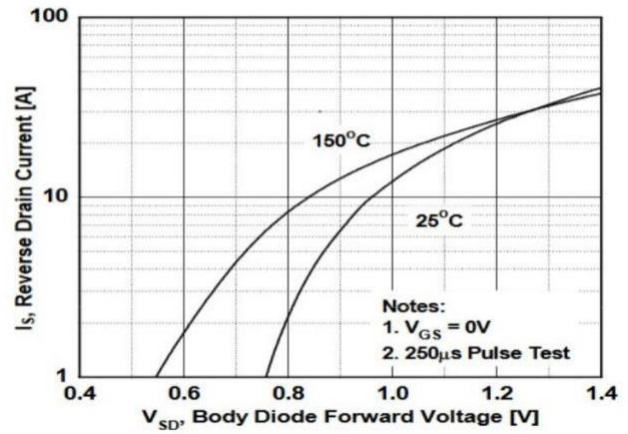


Figure 3. On-Resistance versus Drain Current



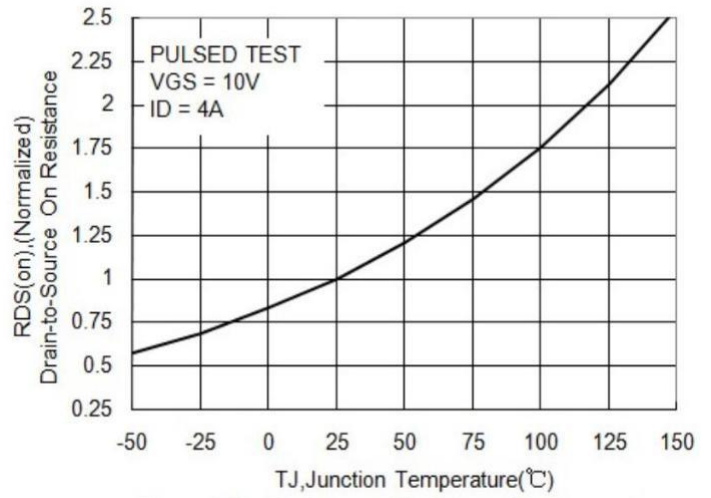
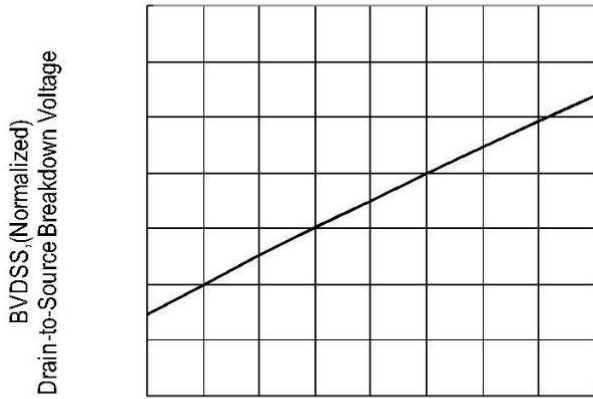


Figure 8. On-Resistance Variation with Temperature

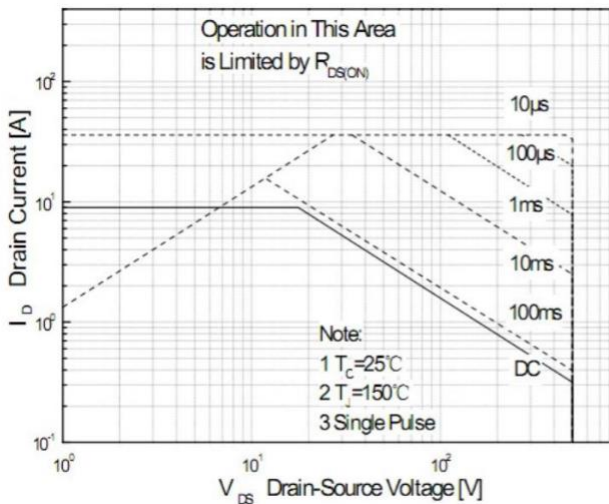


Figure 9. Maximum Safe Operating Area For FX8N50BUG/DG/PG

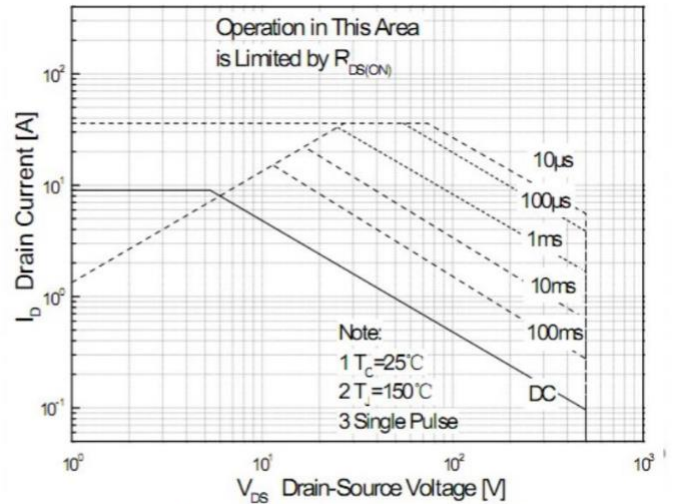
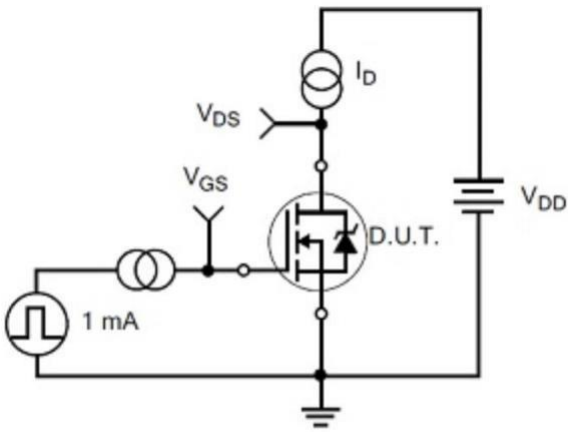
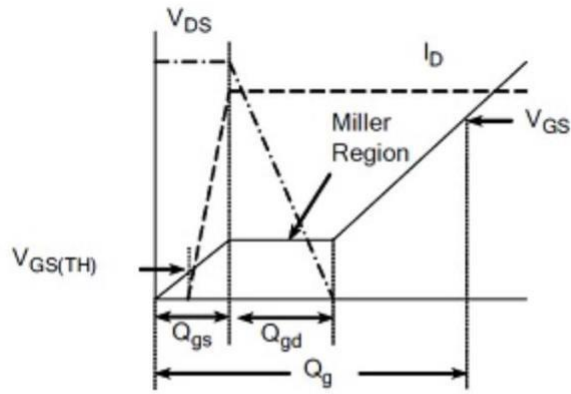


Figure 9. Maximum Safe Operating Area For FX8N50BFG

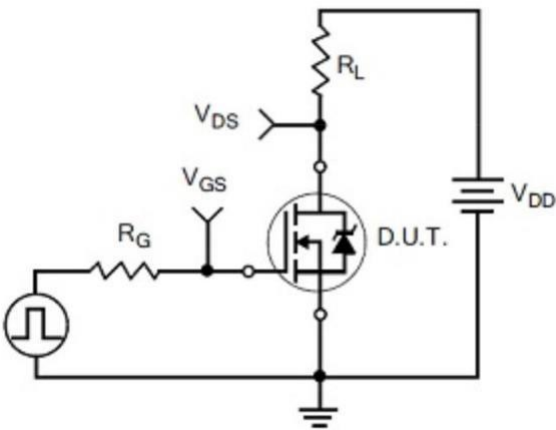




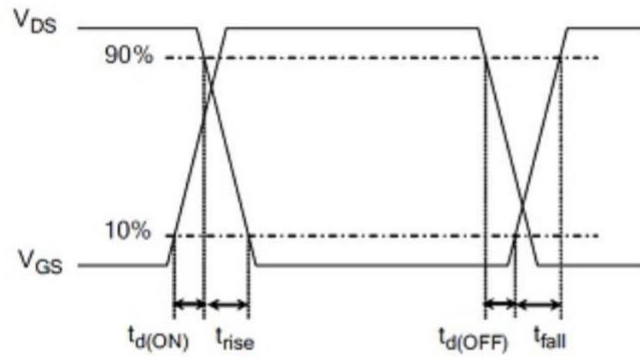
Gate Charge Test Circuit



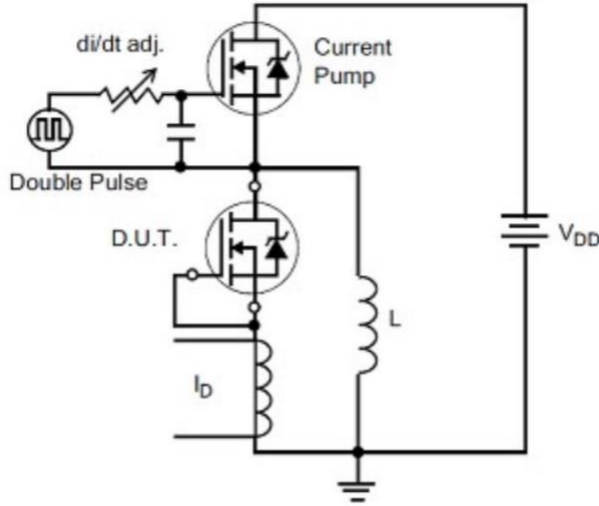
Gate Charge Waveform



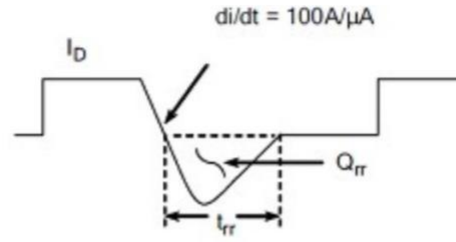
Resistive Switching Test Circuit



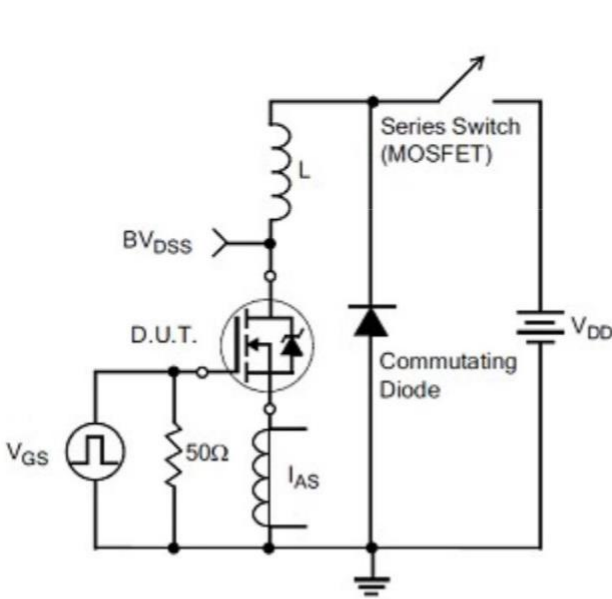
Resistive Switching Waveforms



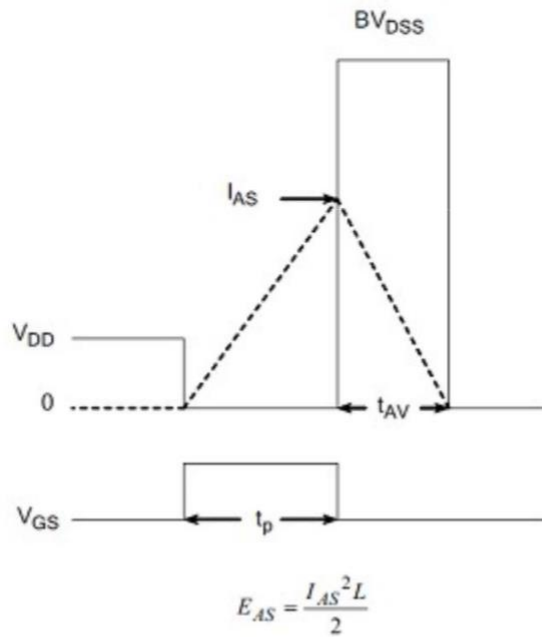
Diode Reverse Recovery Test Circuit



Diode Reverse Recovery Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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