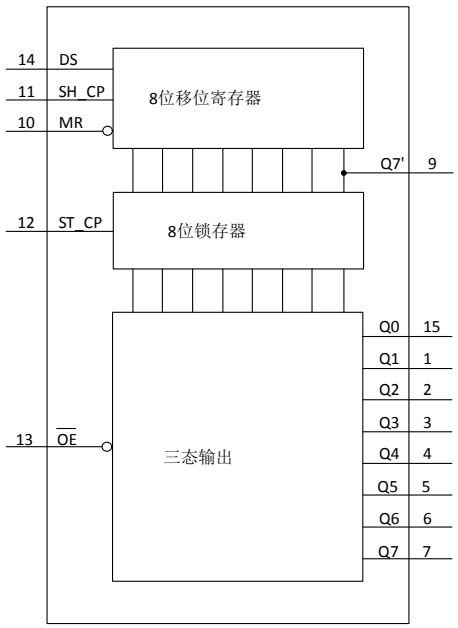
概述

74HC595D是高速硅栅COMS器件，且其引脚兼容低功耗肖特基TTL。74HC595D中由一个8位移位寄存器和一个带有三态并行输出的8位D型锁存器组成。移位寄存器接收串行数据，并提供串行或并行输出。移位寄存器也给8位锁存器提供并行数据。移位寄存器和锁存器有独立的CLK输入端。该元器件还有一个对移位寄存器的异步复位端。

特点

- 8位移位寄存器（串行输入，串行或并行输出）
- 具有三态输出的锁存器
- 60MHz(典型值)的移位输出频
- 率ESD保护
- 封装形式：DIP16、SOP16

功能图



IEC逻辑图

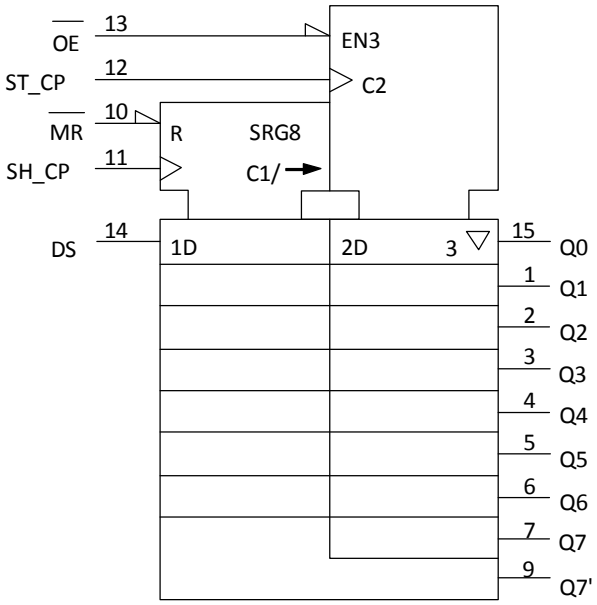
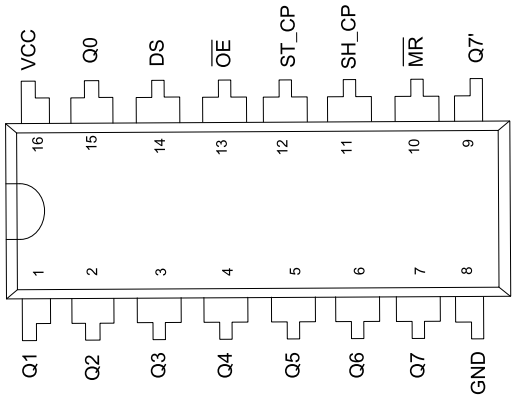


图 1　74HC595D功能图

引脚配置

订购信息

芯片型号	封装形式	采购代号
74HC595D	DIP-16	595DIP16
74HC595D	SOP-16	595SOP16



引脚功能描述

引脚编号	引脚名称	引脚功能
1~7	Q1、Q2、Q3、Q4、Q5、Q6、Q7	并行数据输出
8	GND	接地
9	Q7’	串行数据输出
10	$\overline{MR}$	主复位（低电平有效）
11	SH_CP	移位寄存器时钟输入
12	ST_CP	锁存器时钟输入
13	$\overline{OE}$	输出势能（低电平有效）
14	DS	串行数据输入
15	Q0	并行数据输出
16	VCC	正电源电压

极限参数

除非有特殊要求，GND=0V。

参数名称	符号	条件	最小	最大	单位
电源电压	V_{CC}		-0.5	+6.5	V
输入二极管电流	I_{IK}	V_I＜-0.5V~V_I＞V_{CC}+0.5V	-	±20	mA
输出二极管电流	I_{OK}	V_I＜-0.5V~V_I＞V_{CC}+0.5V	-	±20	mA
输出电源电流或灌电流	I_O	V_I＜-0.5V~V_I＞V_{CC}+0.5V Q7’标准输出 Qn总线驱动输出	 - -	 +25 +35	mA
电源电流或地电流	V_{CC}、I_{GND}		-	±70	mA
功耗	P_D	Tamb=-40~+125°C	500		mW
贮存温度	Tstg		-65	+150	°C

推荐工作范围

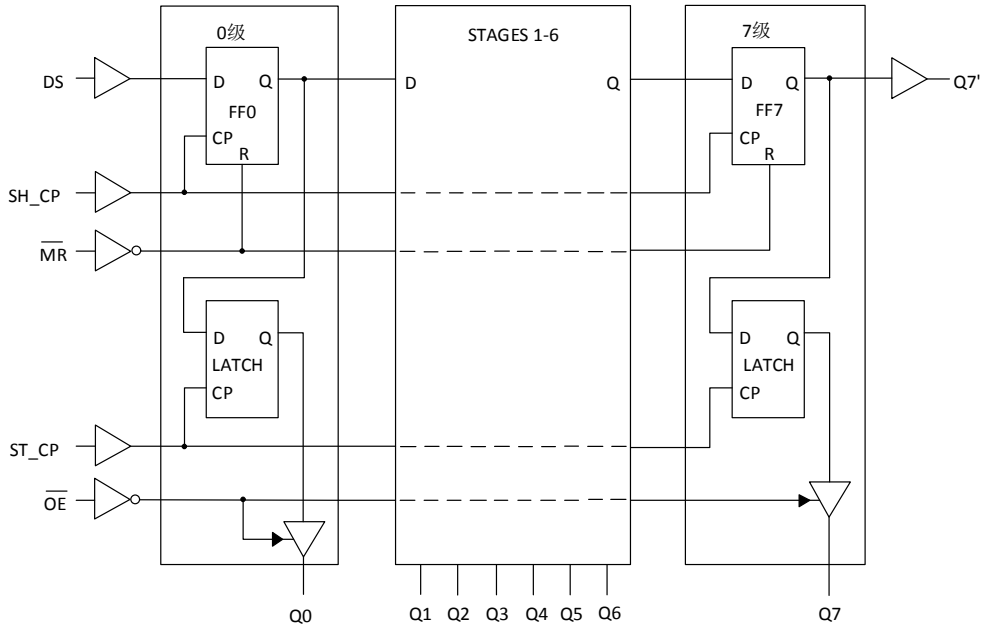
参数	符号/条件	最小值	典型值	最大值	单位
电源电压	V_{CC}	2.0	5.0	6.0	V
输入电压	V_I	0	-	V_{CC}	V
输出电压	V_O	0	-	V_{CC}	V
环境温度	Tamb	-40	-	+125	°C
输入上升时间Tr和下降时间Tf	V_{CC}=2.0V	-	-	1000	ns
	V_{CC}=4.5V	-	6.0	500	ns
	V_{CC}=6.0V	-	-	400	ns

电参数：

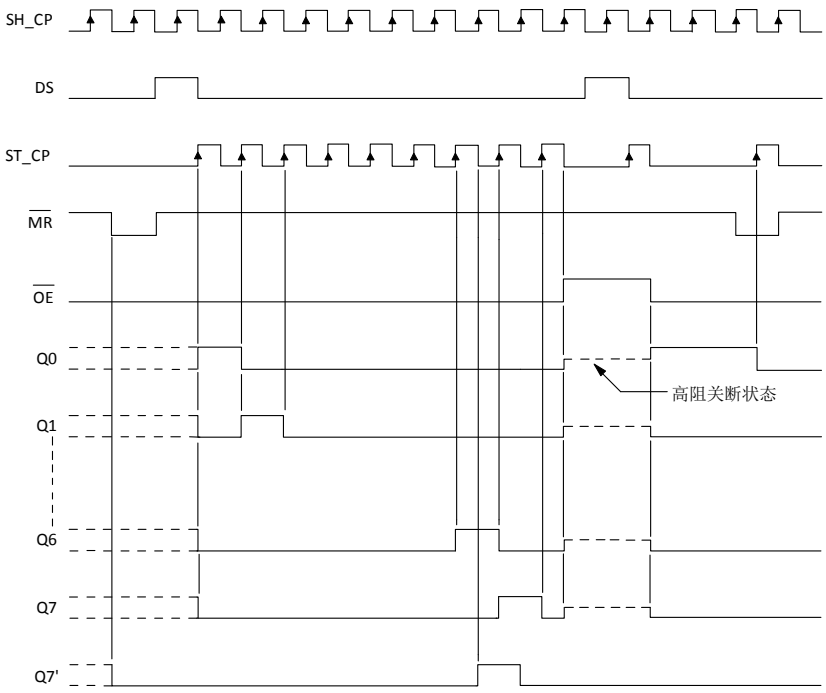
除非有特殊要求，T_A=-40°~+85° C，GND=0V。

特性	符号	条件		最小值	典型值	最大值	单位
		其他	V_{CC}（V）				
输入高电平电压	V_{IH}		2.0	1.4	-	-	V
			4.5	3.15	-	-	
			6.0	4.2	-	-	
输入低电平电压	V_{IL}		2.0	-	-	0.6	V
			4.5	-	-	1.35	
			6.0	-	-	1.8	
输出高电平电压	V_{OH}	V_I= V_{IH}或V_{IL}					V
		所有输出 I_O=-20uA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	- - -	
		Q7’标准输出 I_O=-4.0mA I_O=-5.2mA	 4.5 6.0	 3.84 5.34	 4.32 5.81	 - -	
		Qn总线驱动输出 I_O=-6.0mA I_O=-7.8mA	 4.5 6.0	 3.84 5.34	 4.32 5.81	 - -	
输出低电平电压	V_{OL}	V_I=V_{IH}或V_{IL}					V
		所有输出 I_O=-20A	 2.0 4.5 6.0	 - - -	 0 0 0	 0.1 0.1 0.1	
		Q7’标准输出 I_O=-4.0mA I_O=-5.2mA	 4.5 6.0	 - -	 0.15 0.16	 0.33 0.33	
		Qn总线驱动输出 I_O=-6.0mA I_O=-7.8mA	 4.5 6.0	 - -	 0.16 0.16	 0.33 0.33	
输入漏电流	I_I	V_I=V_{CC}或GND	6.0	-	-	±1.0	uA
三态输出关断电流	I_{OZ}	VI=VIH或VIL VO=VCC或GND	6.0	-	-	±5.0	uA
静态电流	ICC	VI= VCC或GND IO=0		6.0	-	80	uA

逻辑图


0级
STAGES 1-6
7级
DS
SH_CP
MR
ST_CP
OE
D Q
FF0
CP R
LATCH
FF7
Q7'
Q0
Q1 Q2 Q3 Q4 Q5 Q6
Q7

时序图


SH_CP
DS
ST_CP
MR
OE
Q0
Q1
Q6
Q7
Q7'
高阻关断状态

参考测量资料

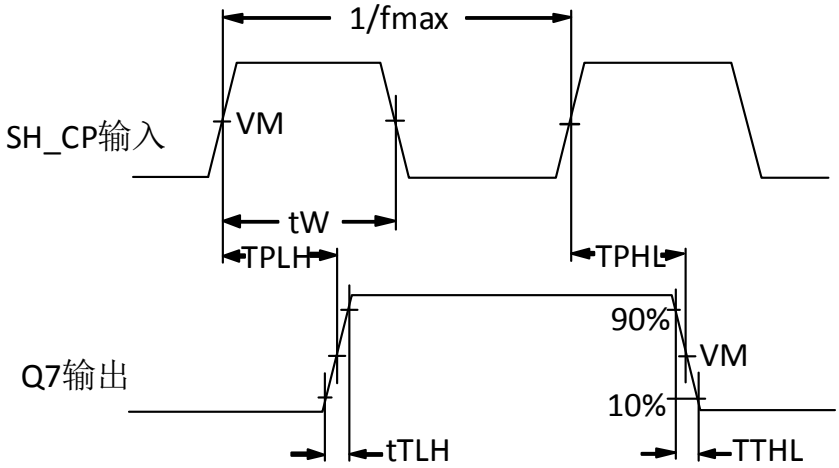


图 1　SH_CP 至 Q7'的传播时延、移位寄存器时钟宽度及最大移位时钟频率的波形图

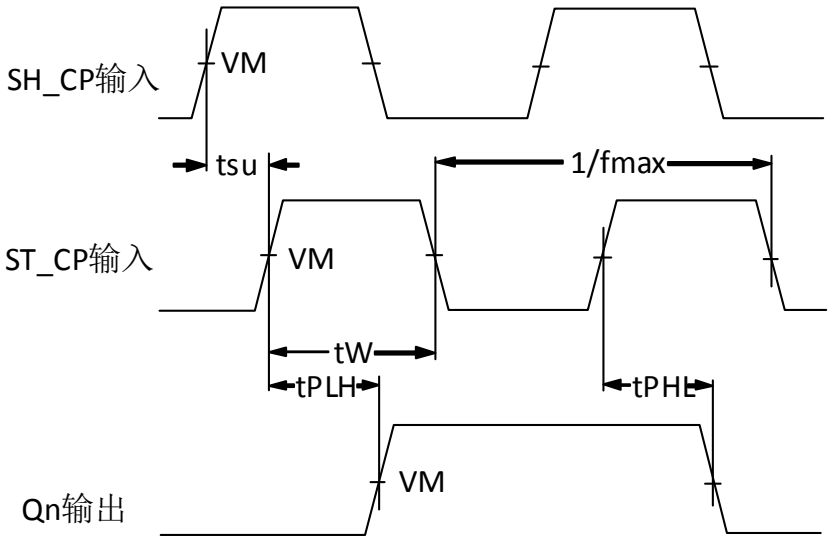


图 2 ST_CP 至 Qn 传播时延、锁存器脉冲宽度及移位寄存器 CLK 到锁存器 CLK 的建立时间

参考测量资料

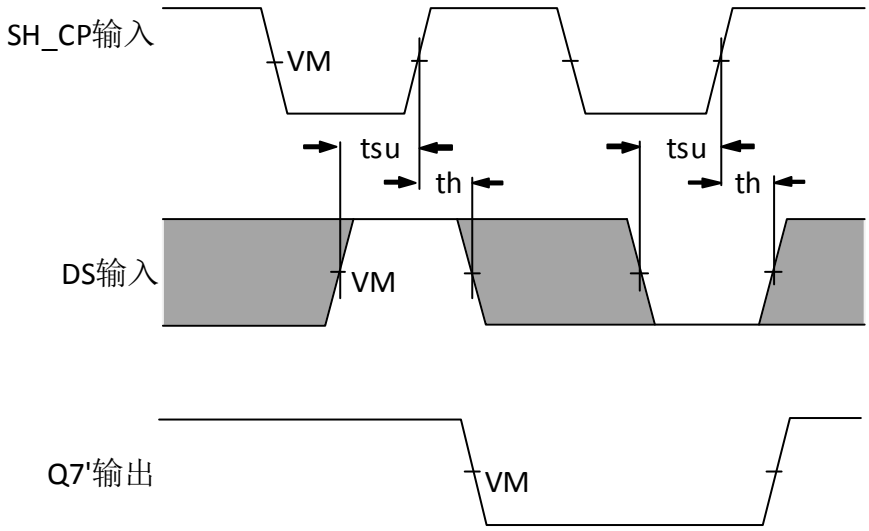


图 3　DS 输入数据的建立、持续时间

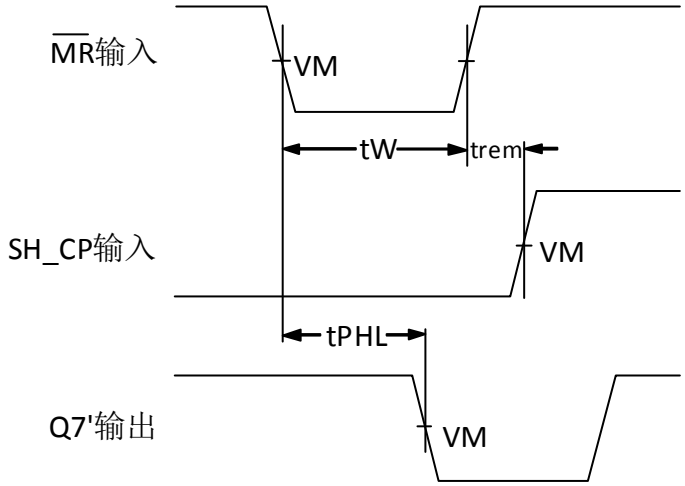


图 4　MR 脉冲宽度、MR 至 Q7'的传播时延及 MR 至 SH_CP 的时间

参考测量资料

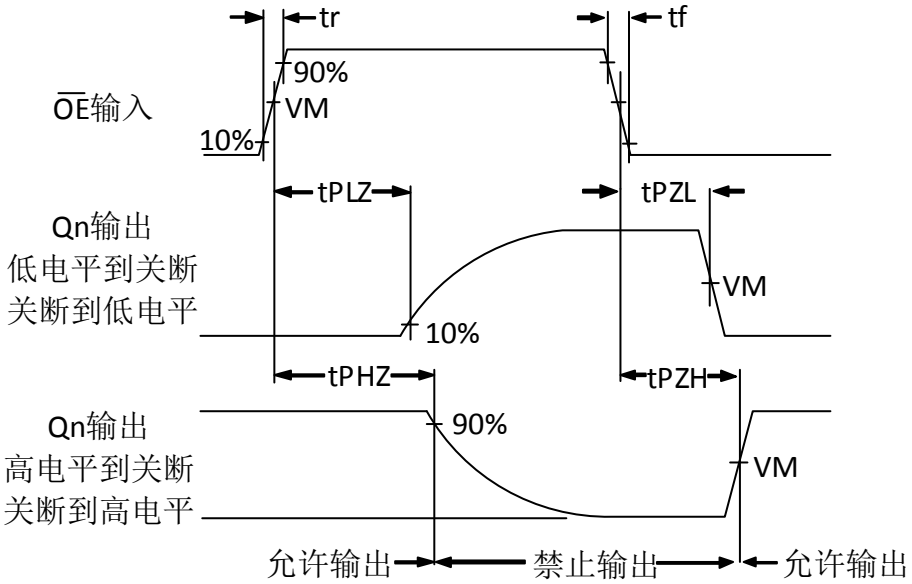


图 5　OE 输入端的三态允许、禁止输出时间波形

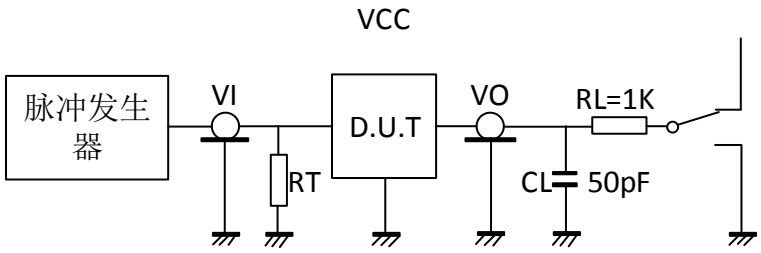
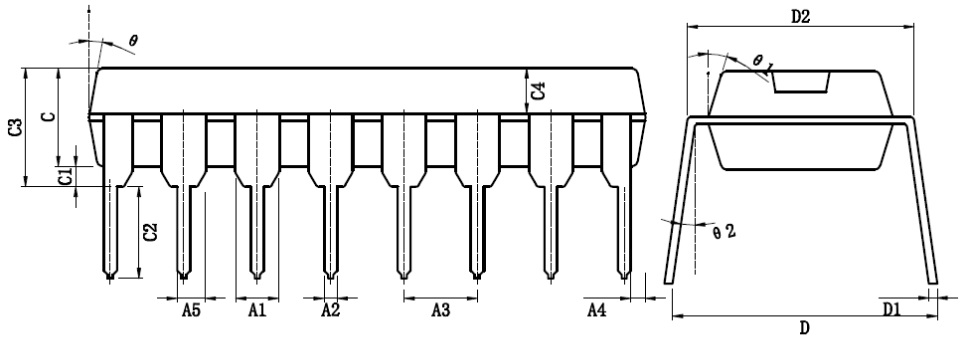
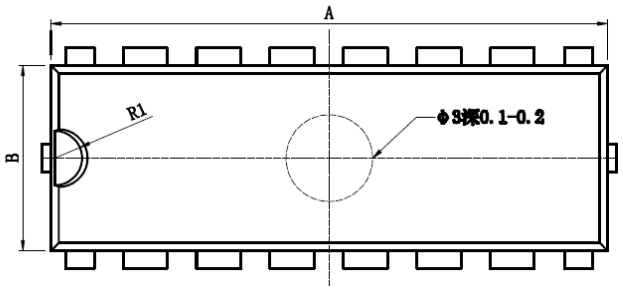


图 6　3 态输出的测试电路图

外形封装图

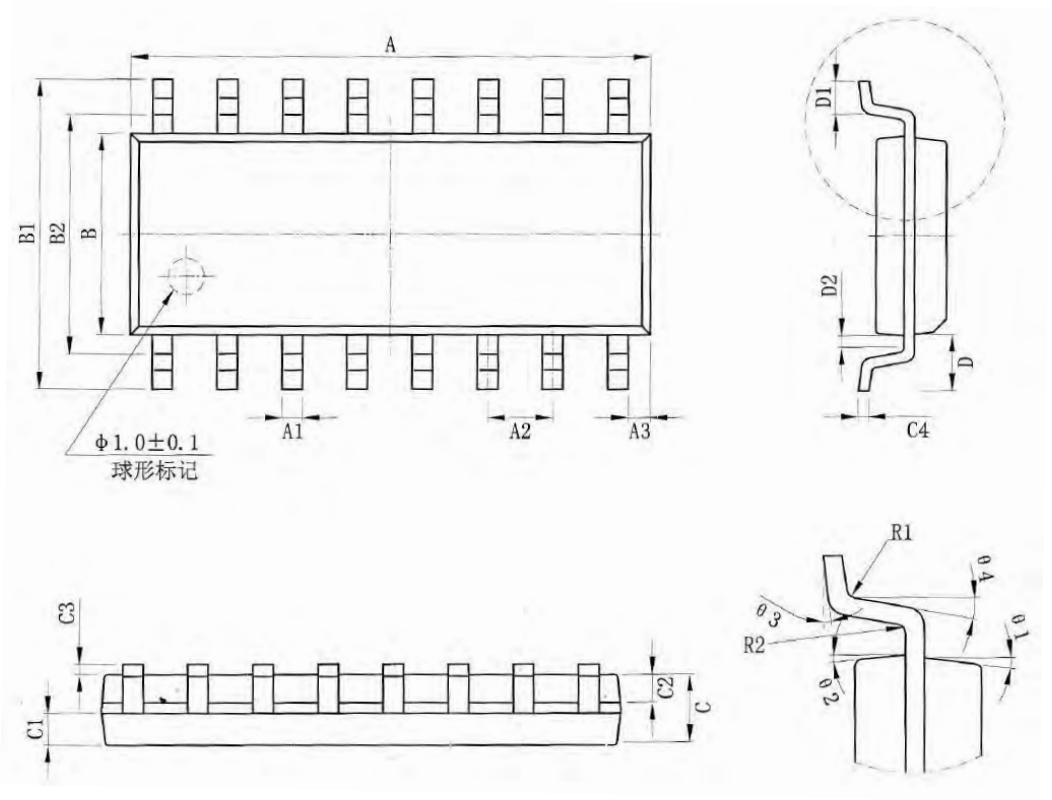
DIP-16 封装





符号	尺寸（mm）		符号	尺寸（mm）	
	最小	最大		最小	最大
A	19.00	19.20	C3	3.85	4.45
A1	1.524TYP		C4	1.40	1.50
A2	0.41	0.51	D	8.20	8.80
A3	2.54TYP		D1	0.20	0.35
A4	0.38TYP		D2	7.74	8.00
A5	0.99TYP		θ	10°TYP	
B	6.30	6.50	Θ1	17°TYP	
C	3.00	3.20	Θ2	6°TYP	
C1	0.51TYP		R1	1.27TYP	
C2	3.00	3.60			

SOP-16 封装



符号	尺寸（mm）		符号	尺寸（mm）	
	最小	最大		最小	最大
A	9.80	10.00	C3	0.05	0.25
A1	0.356	0.456	C4	0.203	0.233
A2	1.27TYP		D	0.15TYP	
A3	0.302TYP		D1	0.40	0.70
B	3.85	3.95	D2	0.15	0.25
B1	5.84	6.24	R1	0.20TYP	
B2	5.00TYP		R2	0.20TYP	
C	1.40	1.60	Θ1	8°~12°TYP	
C1	0.61	0.71	Θ2	8°~12°TYP	
C2	0.54	0.64	Θ3	0°~12°	
			Θ4	4°~12°	

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