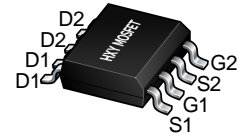




## Description

The 9926A uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8

## General Features

$V_{DS} = 20V$   $I_D = 6A$

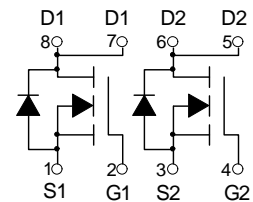
$R_{DS(ON)} < 25m\Omega$  @  $V_{GS}=4.5V$

## Application

Battery protection

Load switch

Uninterruptible power supply



Dual N-Channel MOSFET

## Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
9926A	SOP-8	9926 XXX YYYY	3000

## Absolute Maximum Ratings@ $T_J=25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	20	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	V
$I_D@T_A=25^\circ C$	Drain Current, $V_{GS}$ @ 4.5V <sup>3</sup>	6	A
$I_D@T_A=70^\circ C$	Drain Current, $V_{GS}$ @ 4.5V <sup>3</sup>	4.8	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	26	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	2	W
	Linear Derating Factor	0.016	W/ $^\circ C$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{thj-a}$	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	62.5	$^\circ C/W$



**Electrical Characteristics@T<sub>j</sub>=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	20	-	-	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =6A	-	21	25	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =4A	-	32	45	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	-	1.2	3	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =6A	-	6	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	-	-	25	uA
	Drain-Source Leakage Current (T <sub>j</sub> =70°C)	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	-	-	250	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	I <sub>D</sub> =6A	-	11	17.6	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =16V	-	1.1	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =4.5V	-	4.1	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time <sup>2</sup>	V <sub>DS</sub> =10V	-	4.2	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =1A	-	9	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω, V <sub>GS</sub> =10V	-	23	-	ns
t <sub>f</sub>	Fall Time	R <sub>D</sub> =10Ω	-	3.5	-	ns
C <sub>iss</sub>	Input Capacitance		-	570	910	pF
C <sub>oss</sub>	Output Capacitance	V <sub>GS</sub> =0V	-	90	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	V <sub>DS</sub> =20V f=1.0MHz	-	85	-	pF
R <sub>g</sub>	Gate Resistance	f=1.0MHz	-	1.6	2.4	Ω
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =1.7A, V <sub>GS</sub> =0V	-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time <sup>2</sup>	I <sub>S</sub> =6A, V <sub>GS</sub> =0V, dI/dt=100A/μs	-	21	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	14	-	nC

**Notes:**

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board, t ≤10sec ; 135 °C/W when mounted on Min. copper pad.

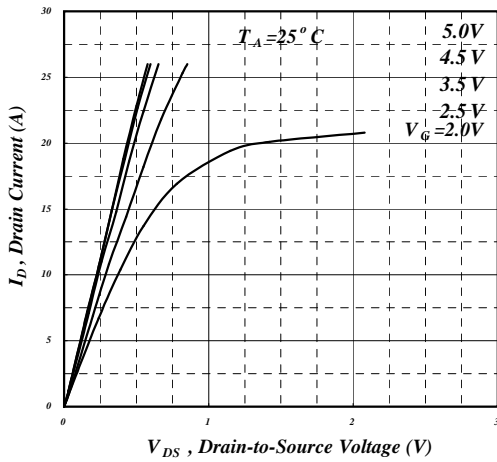


Fig 1. Typical Output Characteristics

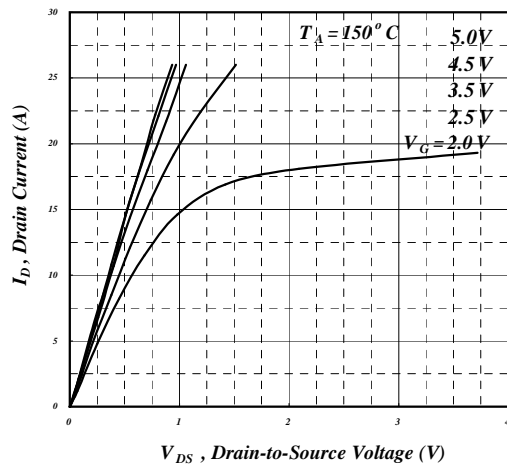


Fig 2. Typical Output Characteristics

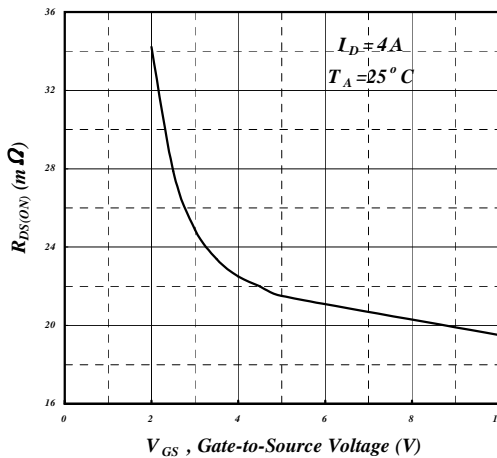


Fig 3. On-Resistance v.s. Gate Voltage

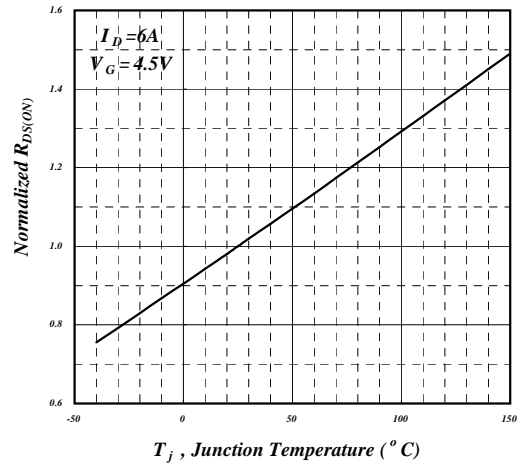


Fig 4. Normalized On-Resistance v.s. Temperature

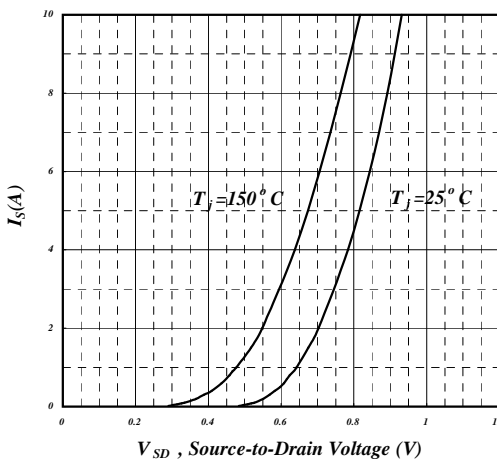


Fig 5. Forward Characteristic of Reverse Diode

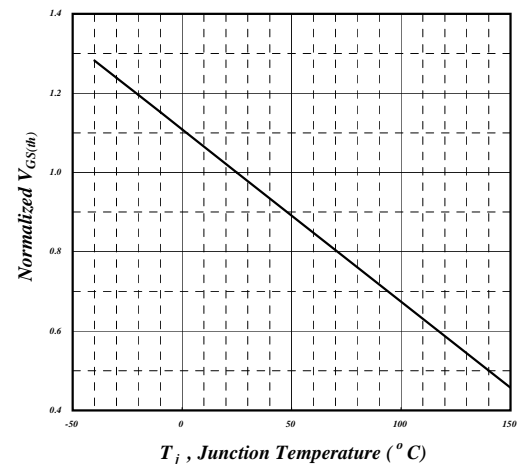


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

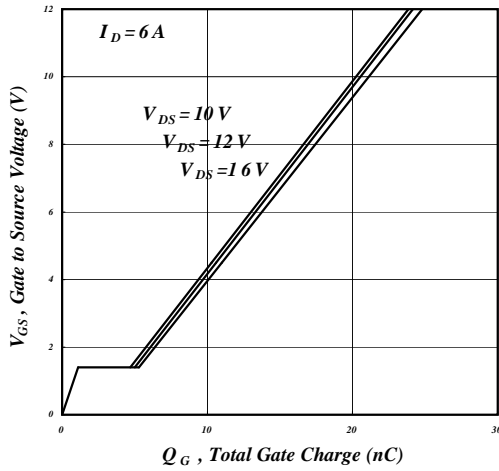


Fig 7. Gate Charge Characteristics

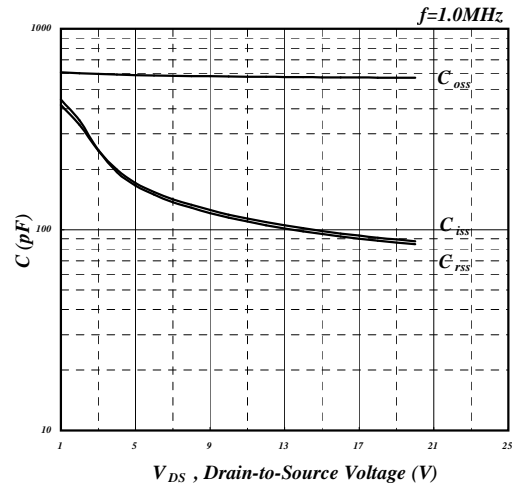


Fig 8. Typical Capacitance Characteristics

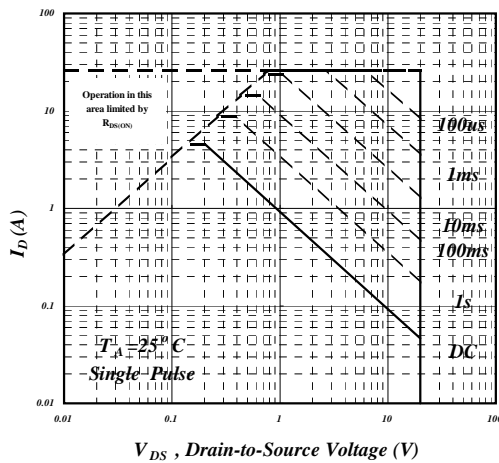


Fig 9. Maximum Safe Operating Area

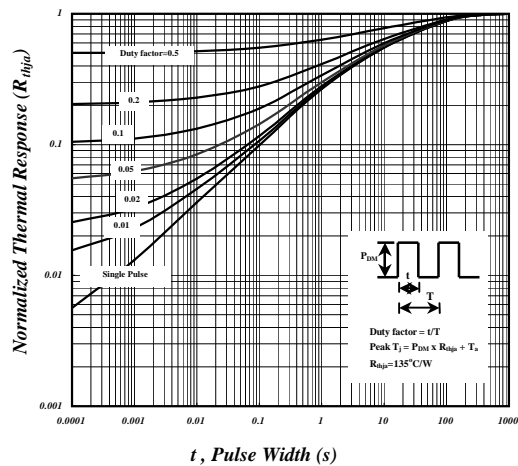


Fig 10. Effective Transient Thermal Impedance

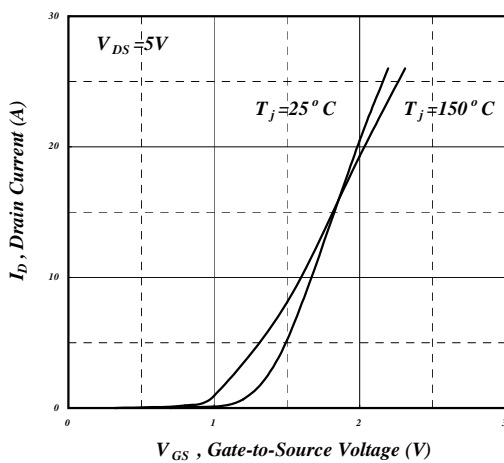


Fig 11. Transfer Characteristics

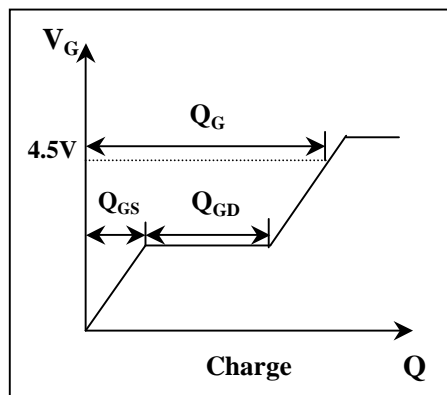
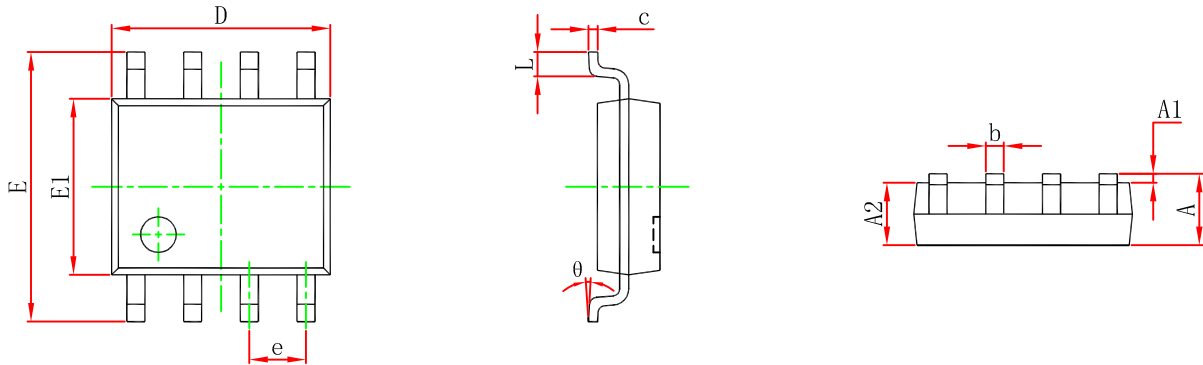


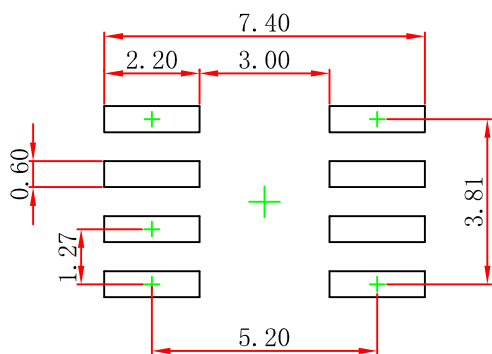
Fig 12. Gate Charge Waveform



### SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



- Note:
1. Controlling dimension: in millimeters.
  2. General tolerance:  $\pm 0.05\text{mm}$ .
  3. The pad layout is for reference purposes only.



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