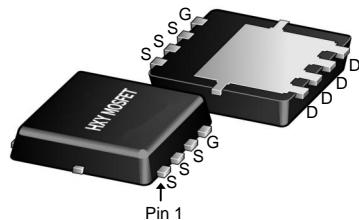




Description

The AONS21321 uses advanced trench technology excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a load switch or in PWM applications.



General Features

$V_{DS} = -30V$, $I_D = -50A$

$R_{DS(ON)} < 15m\Omega$ @ $V_{GS}=-10V$

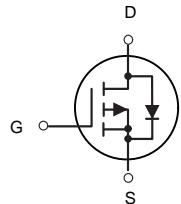
$R_{DS(ON)} < 25m\Omega$ @ $V_{GS}=-4.5V$

High Power and current handling capability

Lead free product is acquired

Surface mount package

DFN5X6-8L



P-Channel MOSFET

Application

PWM applications

Load switch

Power management

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
AONS21321	DFN5X6-8L	HXY MOSFET	5000

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous ($T_c=25^\circ C$)	-50	A
	Drain Current-Continuous ($T_c=100^\circ C$)	-24	
I_{DM}	Drain Current-Pulsed (Note 1)	-80	A
P_D	Maximum Power Dissipation ($T_c=25^\circ C$)	3	W
	Maximum Power Dissipation ($T_c=100^\circ C$)	1.3	
E_{AS}	Single pulse avalanche energy (Note 5)	231	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	°C
$R_{\theta JA}$	Thermal Resistance,Junction-to-Ambient (Note 2)	41.67	°C/W



Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-30	-33	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=-30\text{V}, V_{\text{GS}}=0\text{V}$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-1	-1.5	-3	V
Drain-Source On-State Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}}=-10\text{V}, I_{\text{D}}=-10\text{A}$	-	9	15	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}, I_{\text{D}}=-7\text{A}$	-	18	25	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$V_{\text{DS}}=-10\text{V}, I_{\text{D}}=-10\text{A}$	-	20	-	S
Input Capacitance	C_{iss}	$V_{\text{DS}}=-15\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	1750	-	PF
Output Capacitance	C_{oss}		-	215	-	PF
Reverse Transfer Capacitance	C_{rss}		-	180	-	PF
Turn-on Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}}=-15\text{V}, I_{\text{D}}=-10\text{A}, V_{\text{GS}}=-10\text{V}, R_{\text{GEN}}=1\Omega$	-	9	-	nS
Turn-on Rise Time	t_r		-	8	-	nS
Turn-Off Delay Time	$t_{\text{d(off)}}$		-	28	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	$V_{\text{DS}}=-15\text{V}, I_{\text{D}}=-10\text{A}, V_{\text{GS}}=-10\text{V}$	-	24	-	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	nC
Gate-Drain Charge	Q_{gd}		-	6	-	nC
Diode Forward Current (Note 2)	I_s		-	-	-12	A
Diode Forward Voltage (Note 3)	V_{SD}	$V_{\text{GS}}=0\text{V}, I_s=-12\text{A}$	-	-	-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: $T_j=25^\circ\text{C}, V_{\text{DD}}=-15\text{V}, V_G=10\text{V}, L=0.5\text{mH}, R_g=25\Omega, I_{\text{AS}}=-34\text{A}$



Typical Electrical and Thermal Characteristics

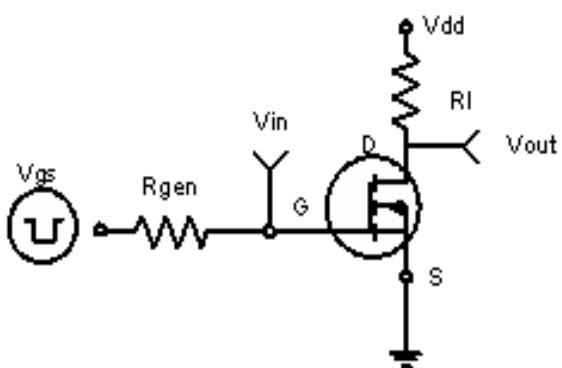


Figure 1:Switching Test Circuit

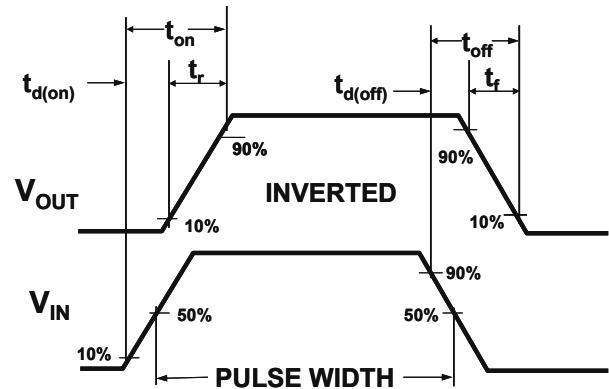


Figure 2:Switching Waveforms

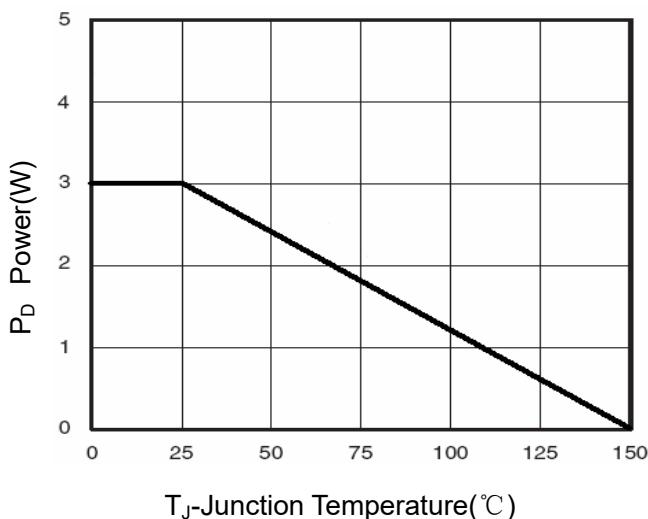


Figure 3 Power Dissipation

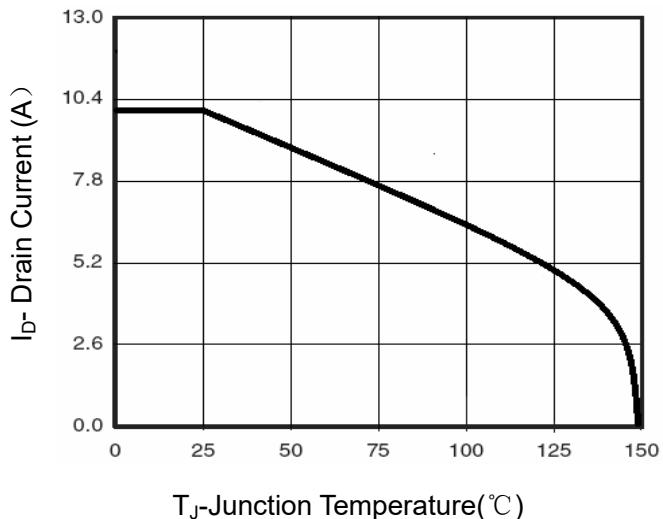


Figure 4 Drain Current

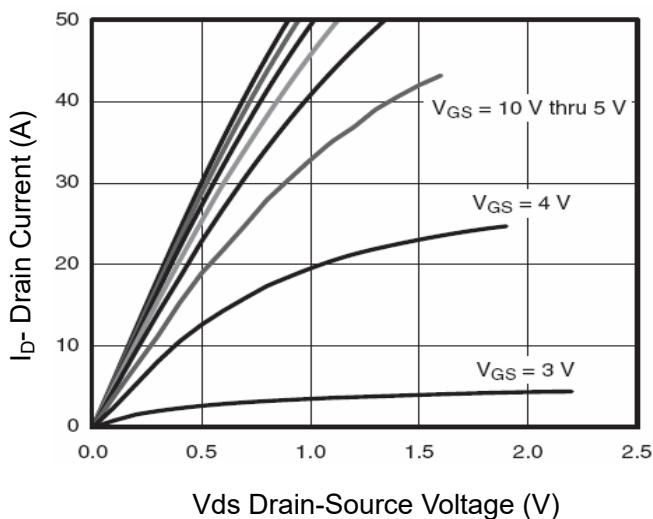


Figure 5 Output Characteristics

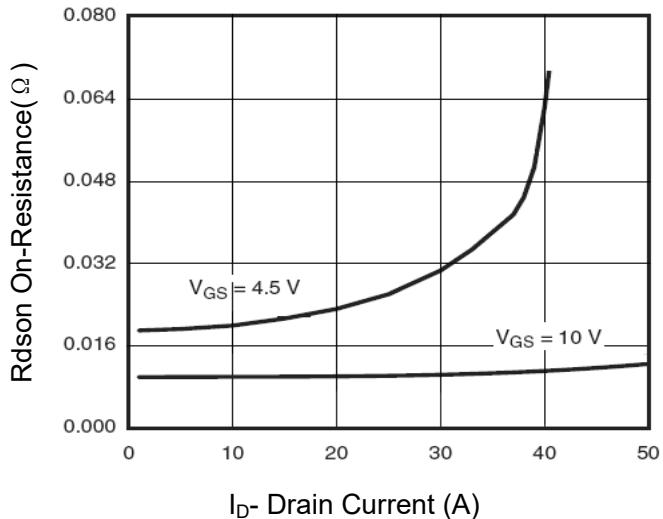


Figure 6 Drain-Source On-Resistance



Figure 5 Output Characteristics

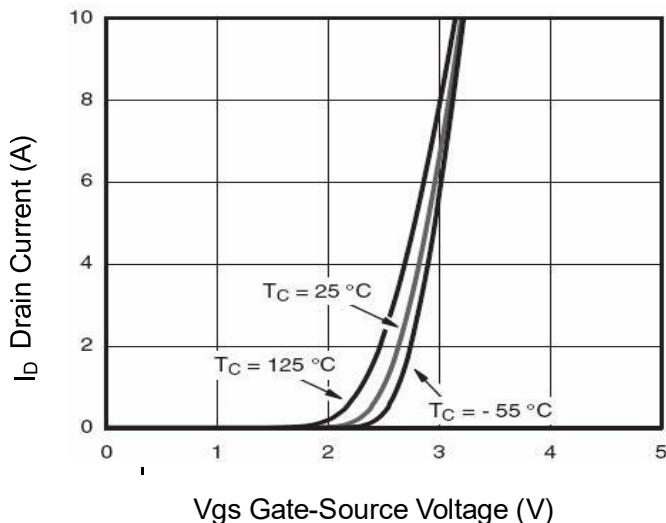


Figure 7 Transfer Characteristics

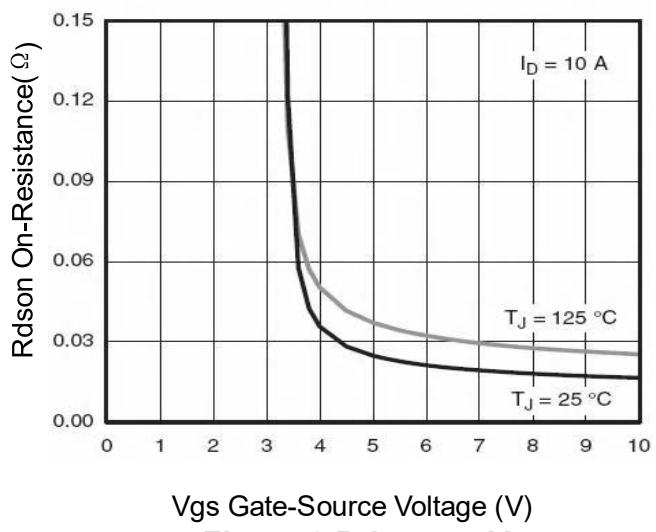


Figure 9 Rdson vs Vgs

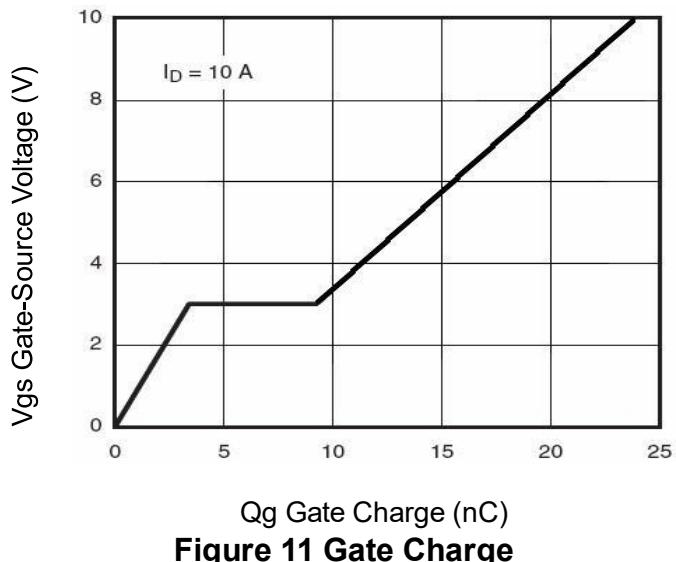


Figure 11 Gate Charge

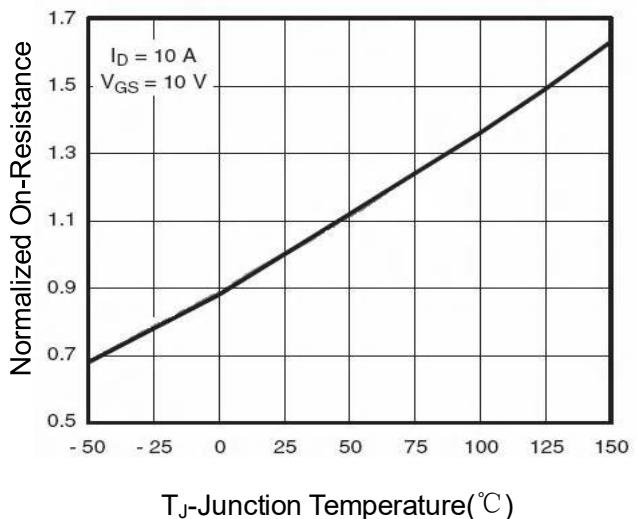


Figure 8 Drain-Source On-Resistance

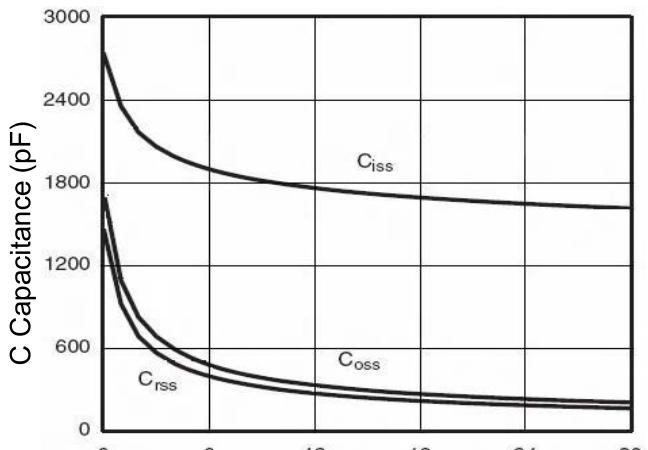


Figure 10 Capacitance vs Vds

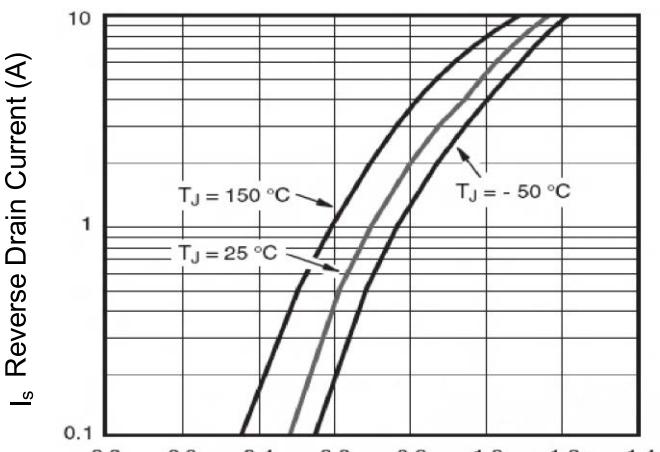


Figure 12 Source-Drain Diode Forward

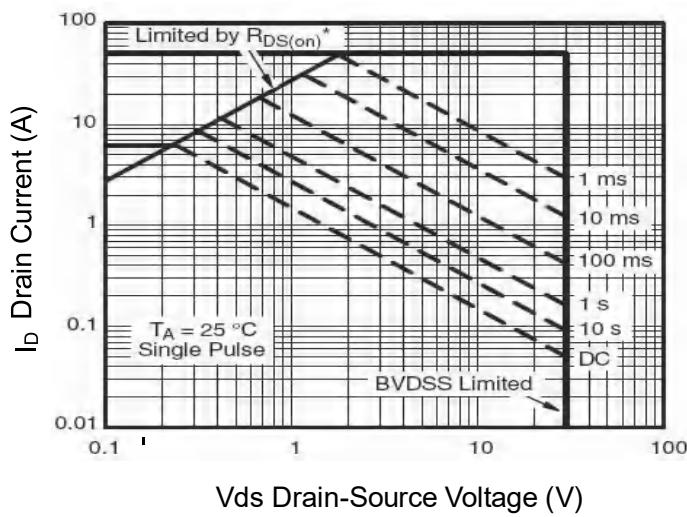


Figure 13 Safe Operation Area

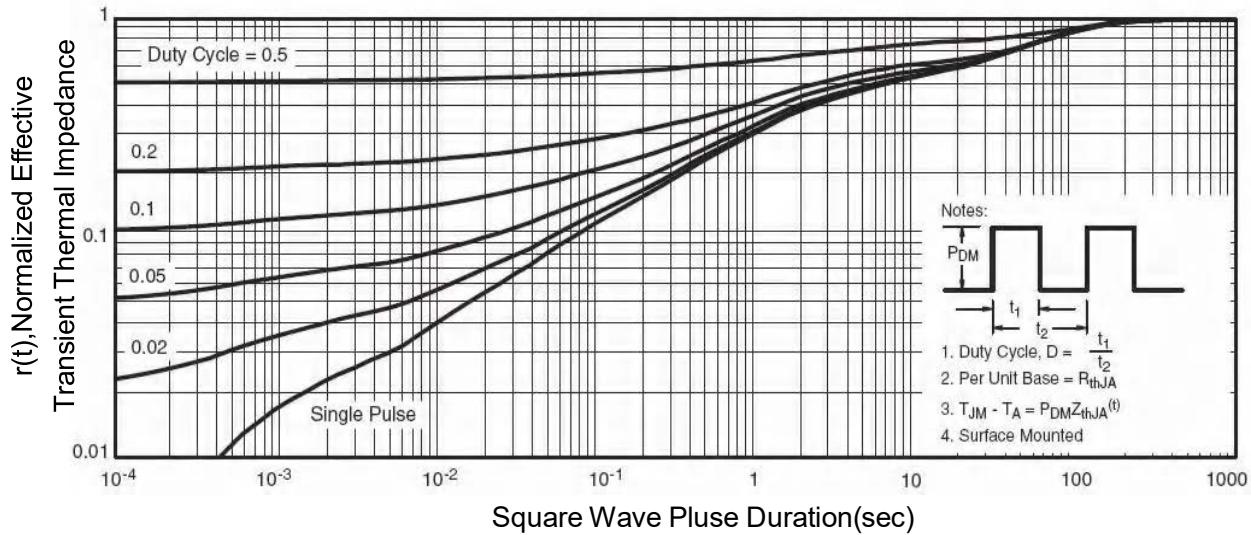
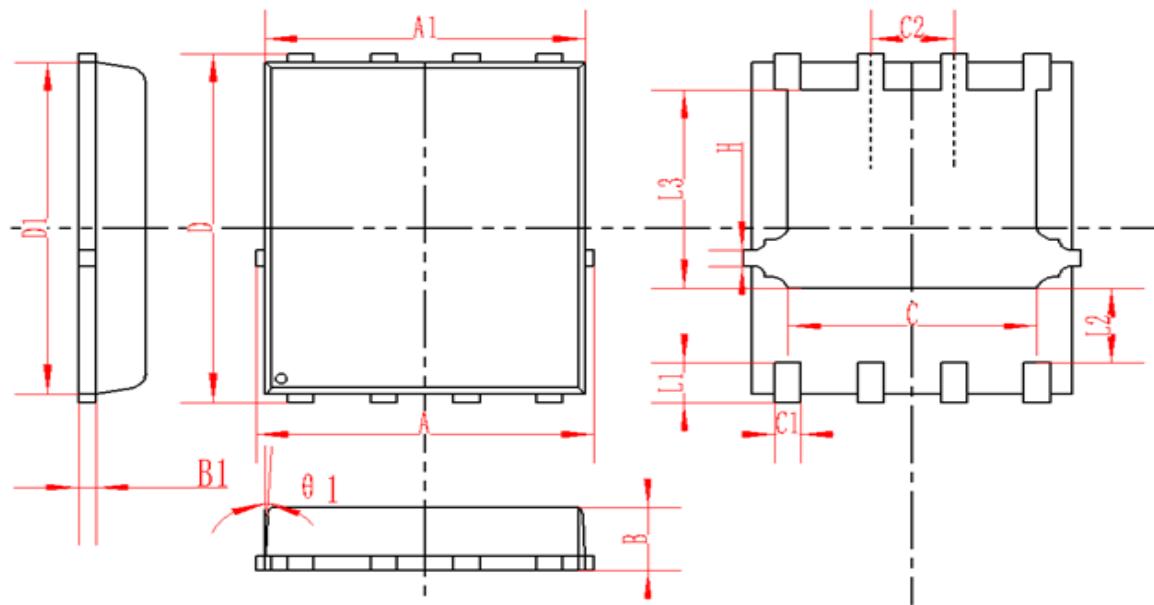


Figure 14 Normalized Maximum Transient Thermal Impedance



DFN5X6-8L Package Information



SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010



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