



### Description

The AUIRLR024N uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



**TO-252-2L**

### General Features

$V_{DS} = 60V$   $I_D = 20A$

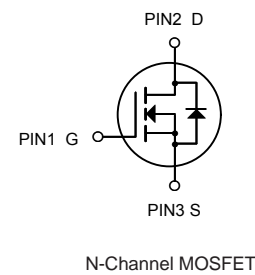
$R_{DS(ON)} < 32m\Omega$  @  $V_{GS}=10V$

### Application

Battery protection

Load switch

Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
AUIRLR024N	TO-252-2L	HXY MOSFET	2500

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	20	A
$I_D @ T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	10	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	80	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	38	mJ
$P_D @ T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	34.7	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$



**Electrical Characteristics (T<sub>J</sub> = 25°C, unless otherwise noted)**

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	60	-	-	V
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T <sub>J</sub> =25°C	I <sub>DSS</sub> V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V	-	-	1	μA
	T <sub>J</sub> =100°C		-	-	100	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.2	1.7	2.5	V
Drain-Source on-Resistance <sup>4</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A	-	25	32	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5A	-	31.5	40	
Forward Transconductance <sup>4</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 10A	-	15.5	-	S
<b>Dynamic Characteristics<sup>5</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V, f = 1MHz	-	1355	-	pF
Output Capacitance	C <sub>oss</sub>		-	60	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	49	-	
Gate Resistance	R <sub>G</sub>	f = 1MHz	-	1.2	-	Ω
<b>Switching Characteristics<sup>5</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 30V, I <sub>D</sub> = 10A	-	22	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	4.2	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	6.9	-	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 30V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = 10A	-	6.4	-	ns
Rise Time	t <sub>r</sub>		-	15.3	-	
Turn-off Delay Time	t <sub>d(off)</sub>		-	25	-	
Fall Time	t <sub>f</sub>		-	7.6	-	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 10A, dI <sub>F</sub> /dt = 100A/μs	-	26	-	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		-	45	-	nC
<b>Drain-Source Body Diode Characteristics</b>						
Diode Forward Voltage <sup>4</sup>	V <sub>SD</sub>	I <sub>S</sub> = 10A, V <sub>GS</sub> = 0V	-	-	1.2	V
Continuous Source Current	T <sub>C</sub> =25°C I <sub>S</sub>	-	-	-	20	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub> = 150°C
2. The EAS data shows Max. rating . The test condition is V<sub>DD</sub> = 25V, V<sub>GS</sub> = 10V, L = 0.4mH, I<sub>AS</sub> = 14A
3. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.



### Typical Characteristics

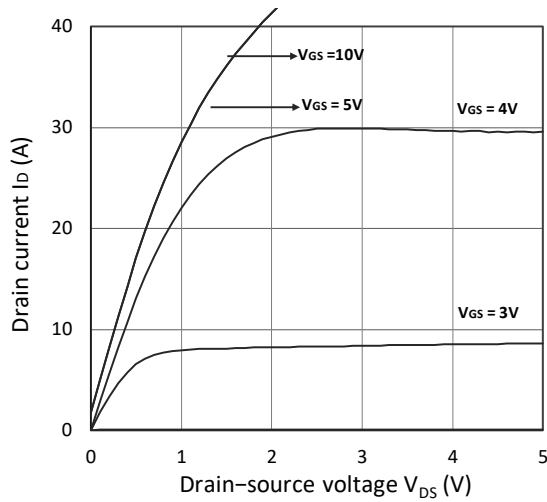


Figure 1. Output Characteristics

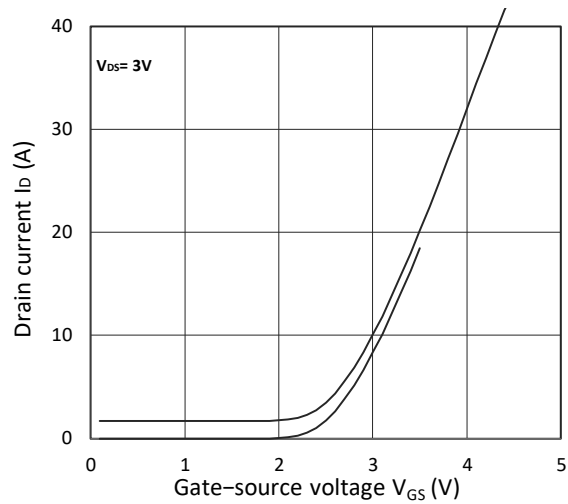


Figure 2. Transfer Characteristics

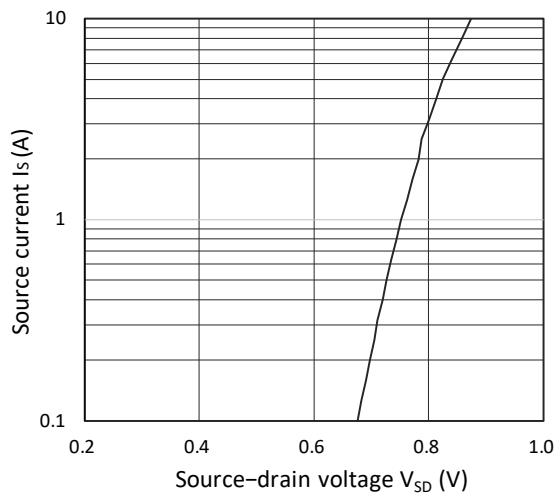


Figure 3. Forward Characteristics of Reverse

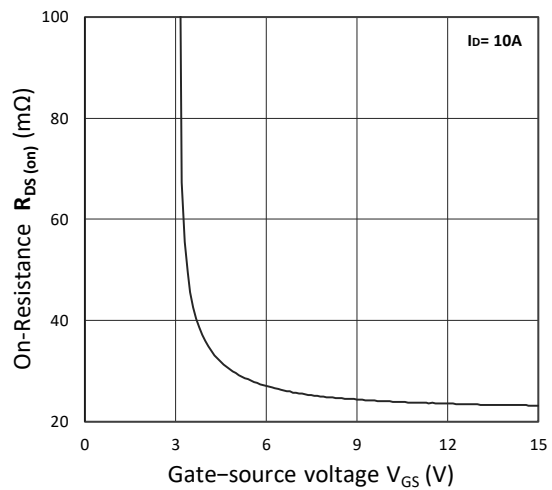


Figure 4.  $R_{DS(ON)}$  vs.  $V_{GS}$

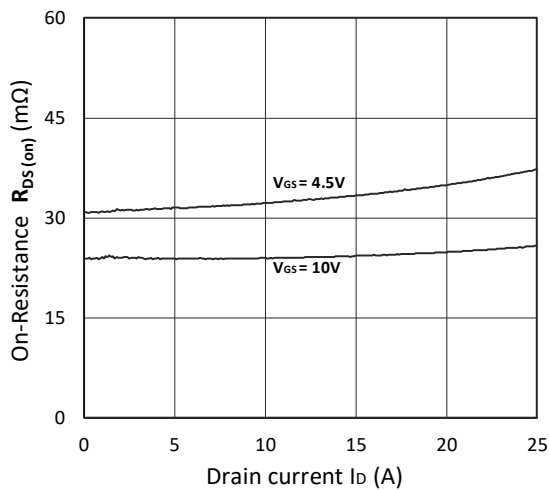


Figure 5.  $R_{DS(ON)}$  vs.  $I_D$

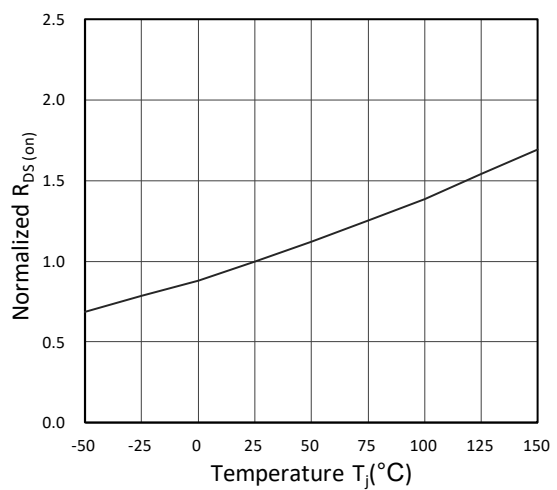


Figure 6. Normalized  $R_{DS(ON)}$  vs. Temperature

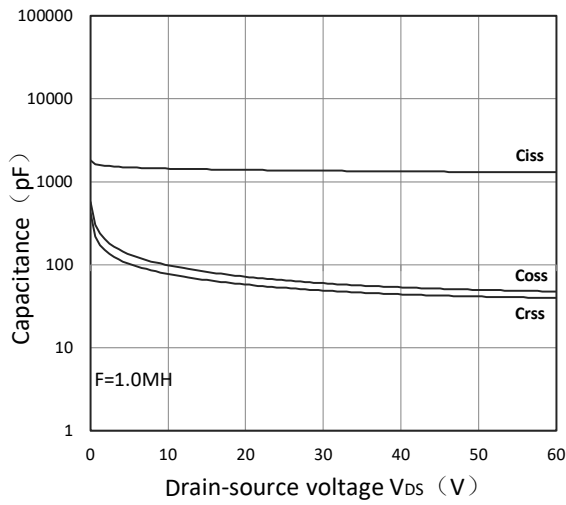


Figure 7. Capacitance Characteristics

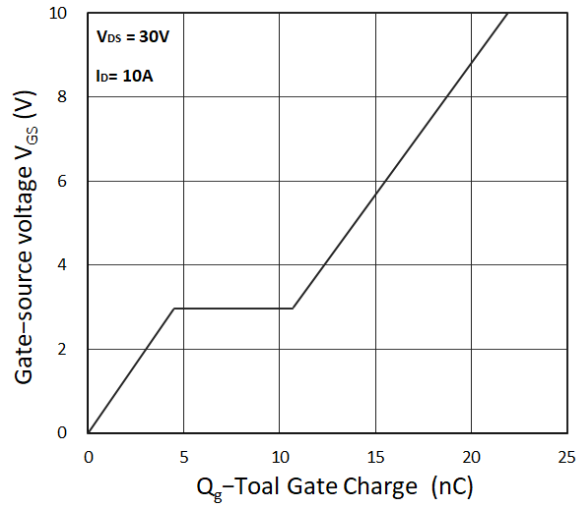


Figure 8. Gate Charge Characteristics

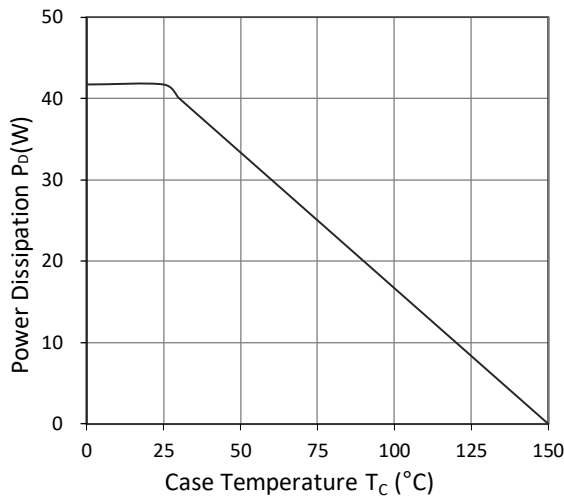


Figure 9. Power Dissipation

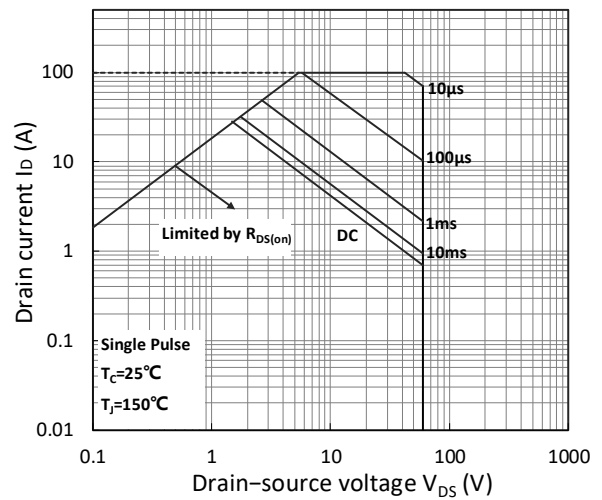


Figure 10. Safe Operating Area

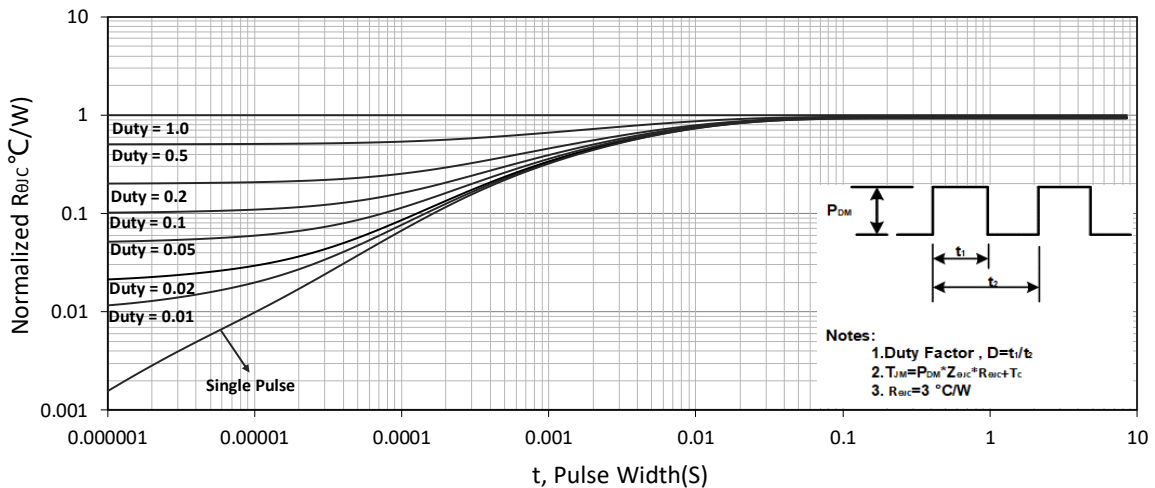


Figure 11. Normalized Maximum Transient Thermal Impedance





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