



Description

The DMC4050SSD uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8

General Features

$V_{DS} = 40V$ $I_D = 7.2A$

$R_{DS(ON)} < 26m\Omega$ @ $V_{GS}=10V$

$V_{DS} = -40V$ $I_D = 6.5A$

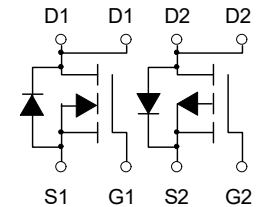
$R_{DS(ON)} < 44m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



N-Channel and P-Channel

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
DMC4050SSD	SOP-8	HXY MOSFET	3000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V_{DS}	Drain-Source Voltage	40	-40	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	7.2	-6.5	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	5.6	-5.1	A
I_{DM}	Pulsed Drain Current ²	23	-22	A
EAS	Single Pulse Avalanche Energy ³	16.2	39	mJ
I_{AS}	Avalanche Current	18	-28	A
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	1.67	1.67	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	75		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	30		$^\circ C/W$



N-Channel Electrical Characteristics ($T_J=25\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	---	---	V
BV_{DSS}/T_J	BVDSS Temperature Coefficient	Reference to $25\text{ }^\circ\text{C}$, $I_D=1mA$	---	0.034	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=5A$	---	20	26	$m\Omega$
		$V_{GS}=4.5V, I_D=4A$	---	28	33	
$V_{GS(th)}$	Gate Threshold Voltage		1.0	---	2.5	V
$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient	$V_{GS}=V_{DS}, I_D=250\mu A$	---	-4.56	---	$mV/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=32V, V_{GS}=0V, T_J=25\text{ }^\circ\text{C}$	---	---	1	μA
		$V_{DS}=32V, V_{GS}=0V, T_J=55\text{ }^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=5A$	---	14	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	2.6	---	
Q_g	Total Gate Charge (4.5V)		---	5.5	---	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=20V, V_{GS}=4.5V, I_D=5A$	---	1.25	---	
Q_{gd}	Gate-Drain Charge		---	2.5	---	
$T_{d(on)}$	Turn-On Delay Time		---	8.9	---	ns
T_r	Rise Time	$V_{DD}=20V, V_{GS}=10V, R_g=3.3$	---	2.2	---	
$T_{d(off)}$	Turn-Off Delay Time	$I_D=1A$	---	41	---	
T_f	Fall Time		---	2.7	---	
C_{iss}	Input Capacitance		---	593	---	pF
C_{oss}	Output Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	---	76	---	
C_{rss}	Reverse Transfer Capacitance		---	56	---	
I_S	Continuous Source Current ^{1,5}		---	---	6.1	A
I_{SM}	Pulsed Source Current ^{2,5}	$V_G=V_D=0V$, Force Current	---	---	23	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25\text{ }^\circ\text{C}$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=18A$
- 4.The power dissipation is limited by $150\text{ }^\circ\text{C}$ junction temperature
- 5 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



P-Channel Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =-250uA	-40	---	---	V
BV _{DSS} / T _J	BV _{DSS} Temperature Coefficient	Reference to 25°C , I _D =-1mA	---	-0.02	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V , I _D =-6A	---	35	44	mΩ
		V _{GS} =-4.5V , I _D =-4A	---	55	68	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.0	---	-2.5	V
V _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	3.72	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-32V , V _{GS} =0V , T _J =25°C	---	---	1	uA
		V _{DS} =-32V , V _{GS} =0V , T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V , V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V , I _D =-6A	---	13	---	S
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-20V , V _{GS} =-4.5V , I _D =-6A	---	11.5	---	nC
Q _{gs}	Gate-Source Charge		---	3.5	---	
Q _{gd}	Gate-Drain Charge		---	3.3	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-15V , V _{GS} =-10V , R _G =3.3 Ω , I _D =-1A	---	22	---	ns
T _r	Rise Time		---	15.7	---	
T _{d(off)}	Turn-Off Delay Time		---	59	---	
T _f	Fall Time		---	5.5	---	
C _{iss}	Input Capacitance	V _{DS} =-15V , V _{GS} =0V , f=1MHz	---	1415	---	pF
C _{oss}	Output Capacitance		---	134	---	
C _{rss}	Reverse Transfer Capacitance		---	102	---	
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V , Force Current	---	---	-6	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	-22	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V , I _S =-1A , T _J =25°C	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V_{DD}=-25V,V_{GS}=-10V,L=0.1mH,I_{AS}=-28A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



N-Channel Typical Characteristics

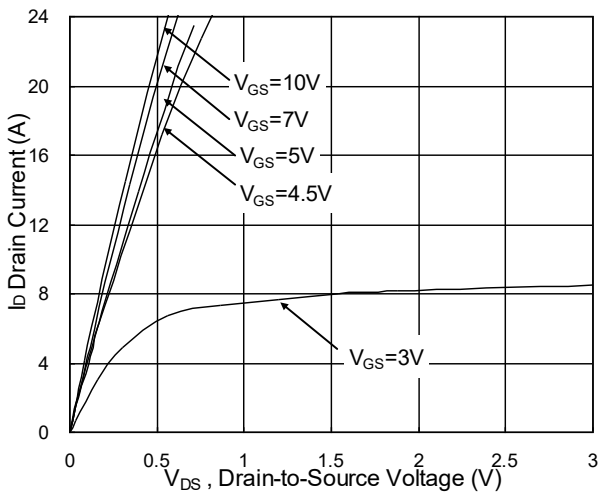


Fig.1 Typical Output Characteristics

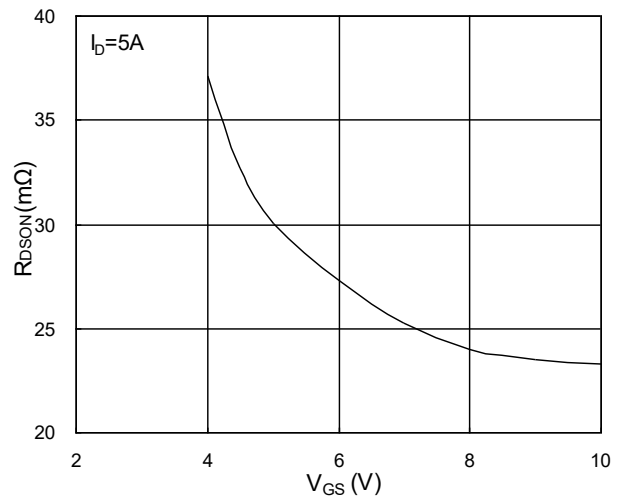


Fig.2 On-Resistance vs. G-S Voltage

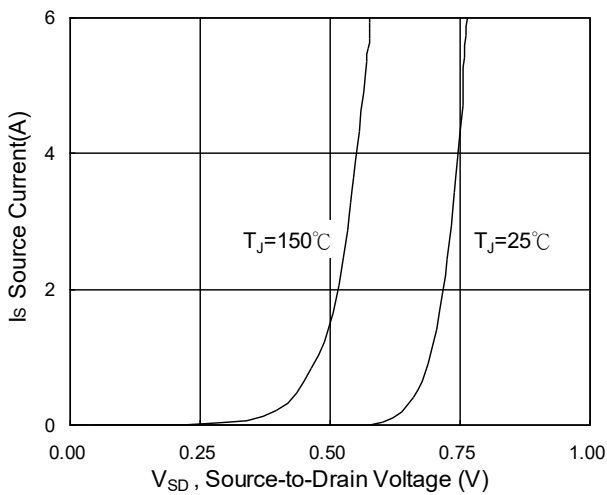


Fig.3 Forward Characteristics of Reverse

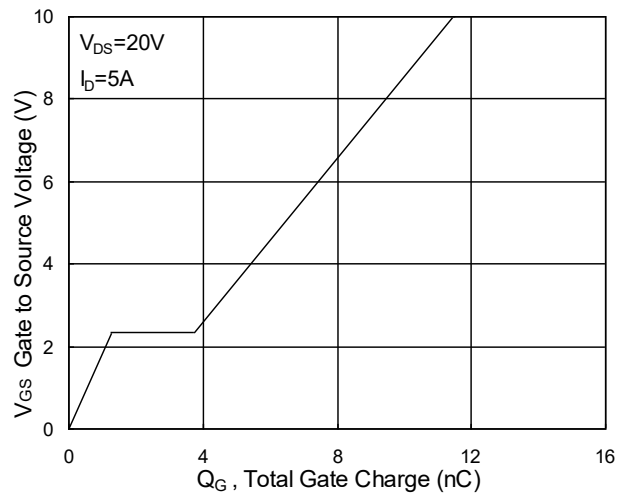


Fig.4 Gate-Charge Characteristics

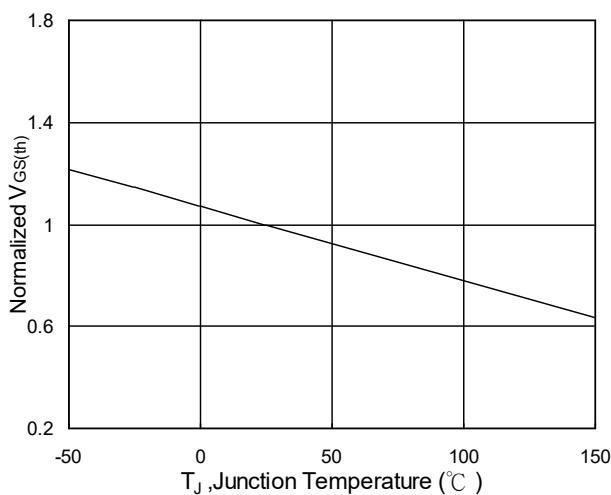


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

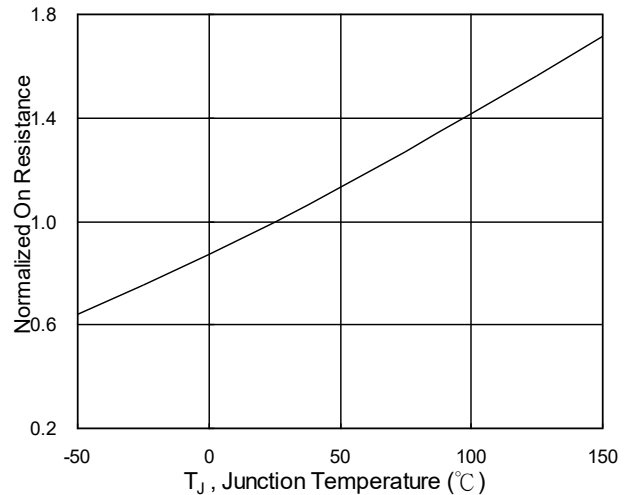


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

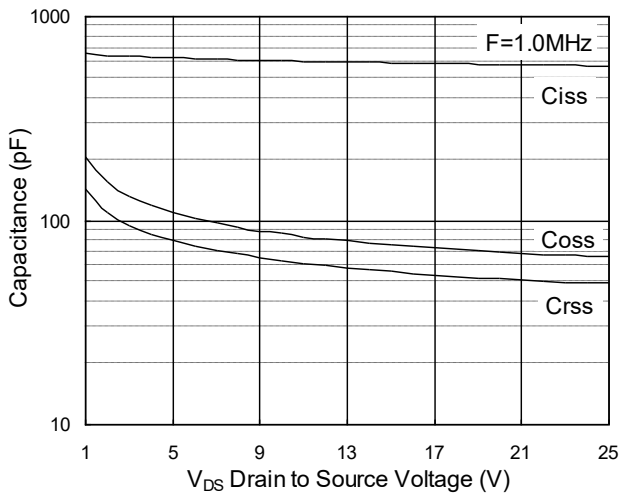


Fig.7 Capacitance

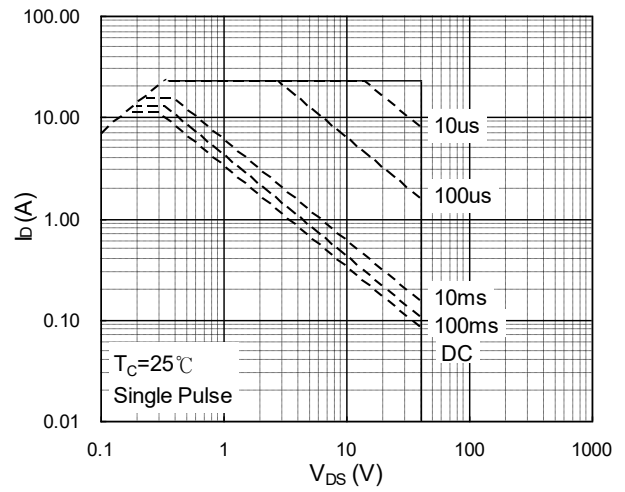


Fig.8 Safe Operating Area

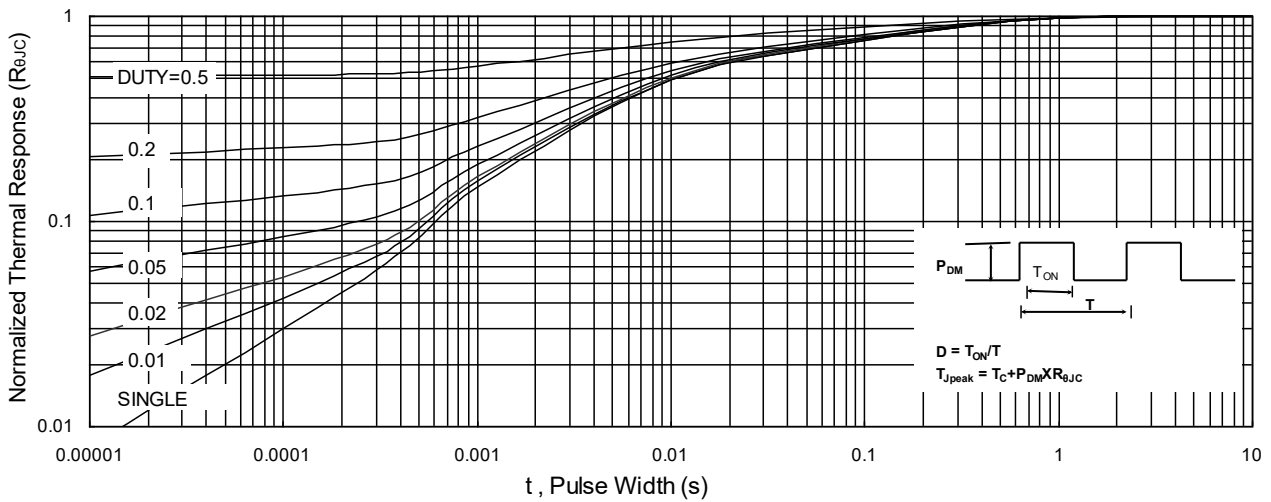


Fig.9 Normalized Maximum Transient Thermal Impedance

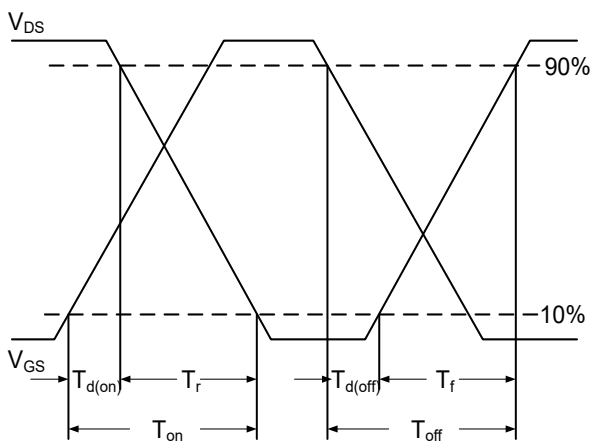


Fig.10 Switching Time Waveform

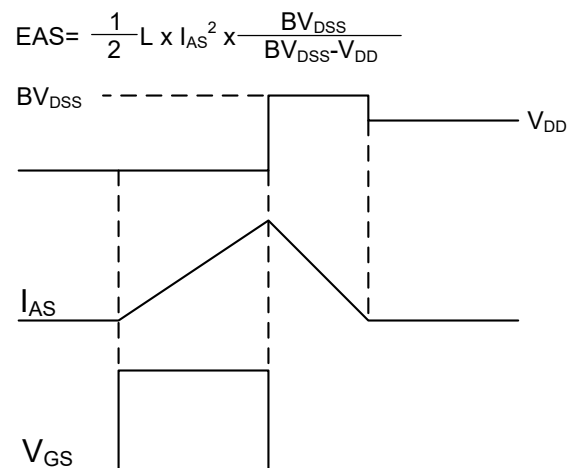


Fig.11 Unclamped Inductive Switching Wave



P-Channel Typical Characteristics

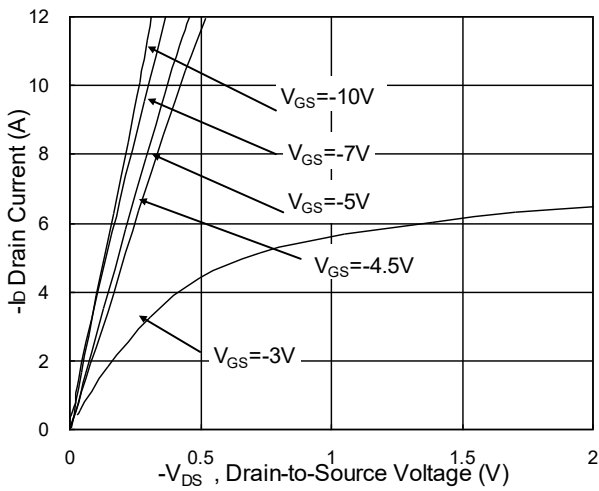


Fig.1 Typical Output Characteristics

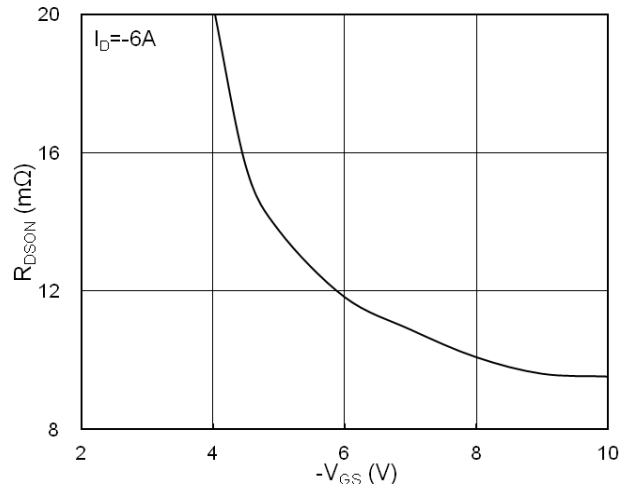


Fig.2 On-Resistance v.s Gate-Source

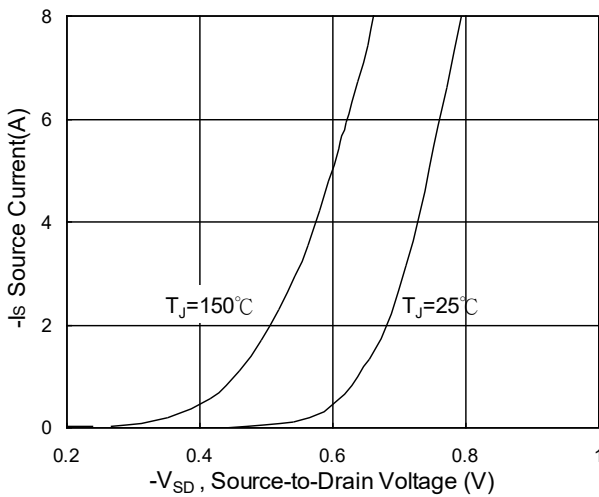


Fig.3 Forward Characteristics of Reverse

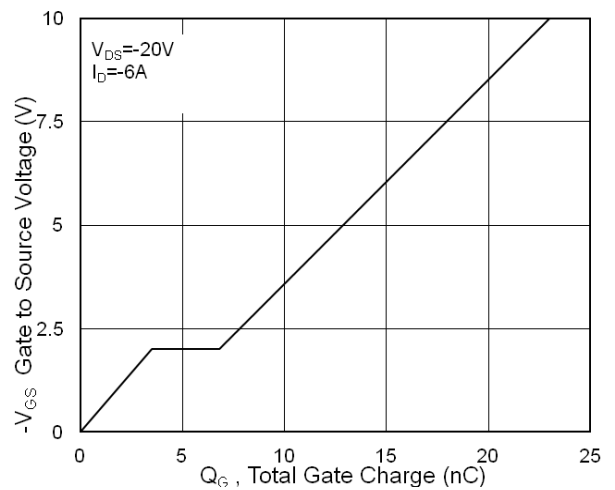


Fig.4 Gate-Charge Characteristics

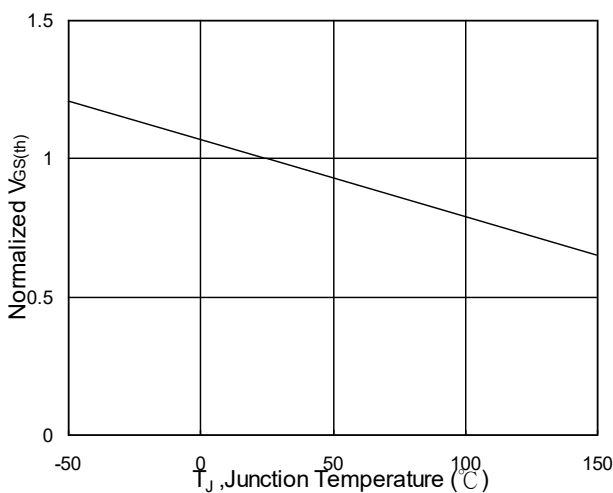


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

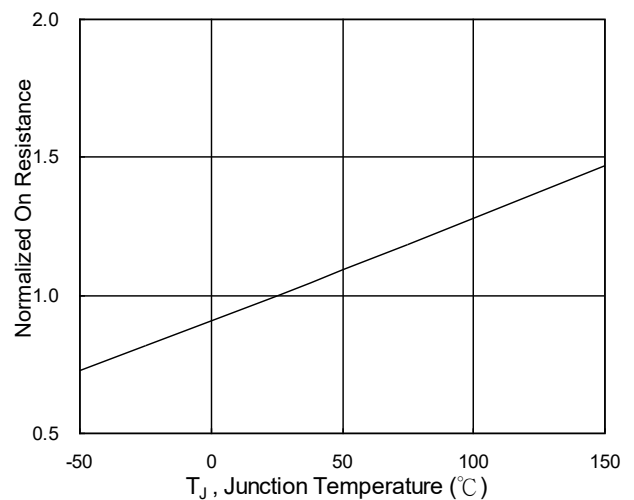


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

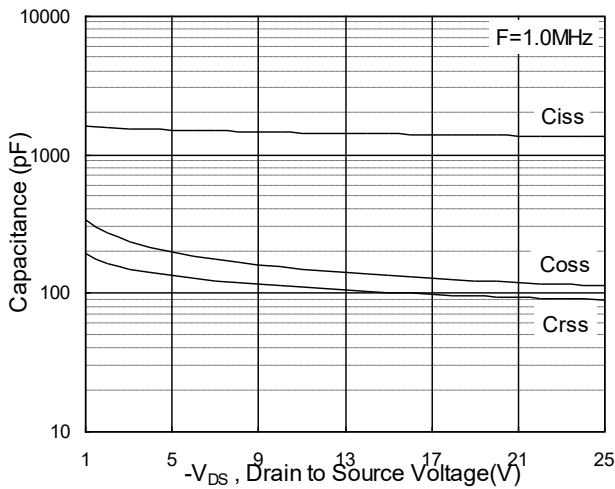


Fig.7 Capacitance

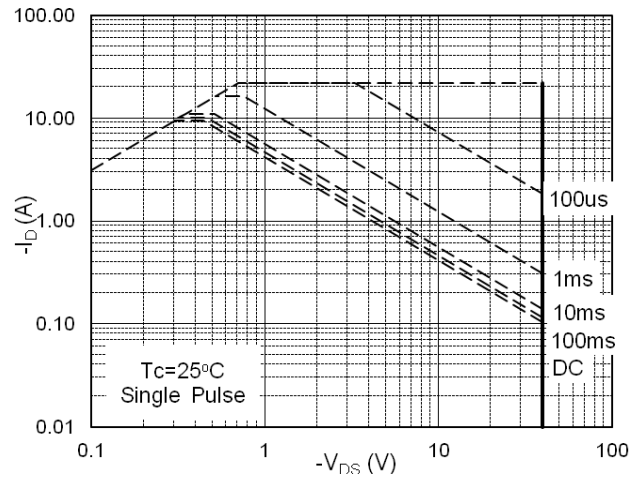


Fig.8 Safe Operating Area

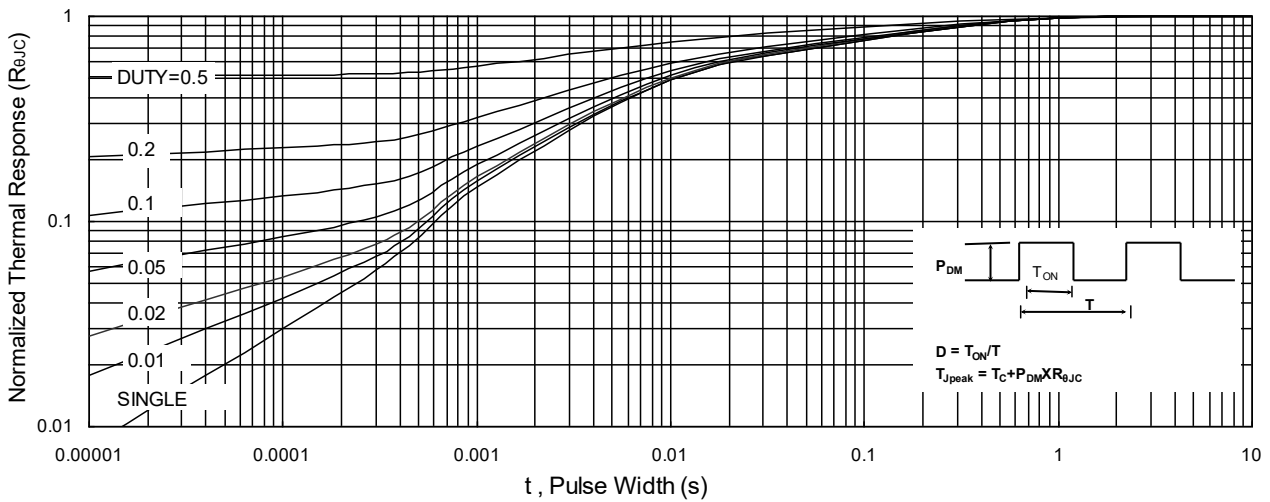


Fig.9 Normalized Maximum Transient Thermal Impedance

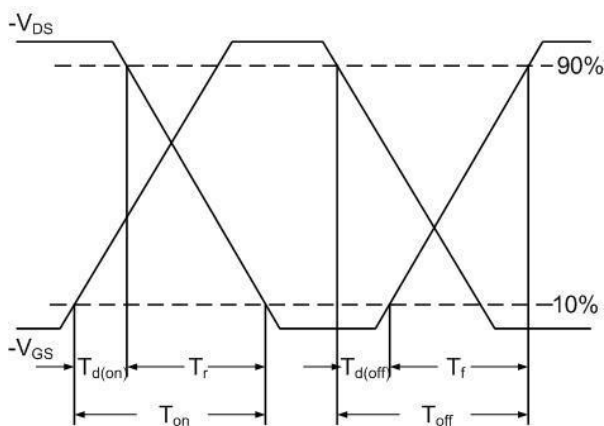


Fig.10 Switching Time Waveform

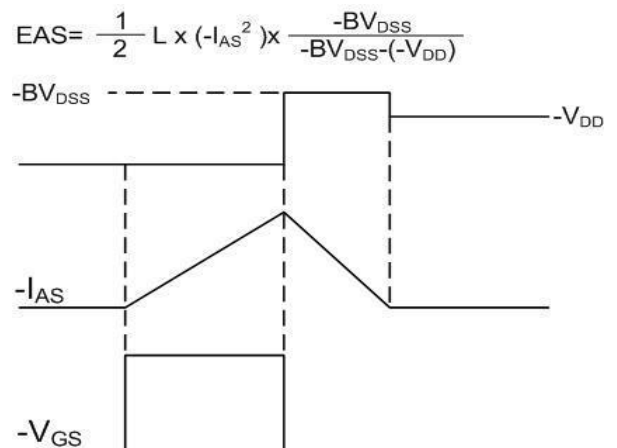
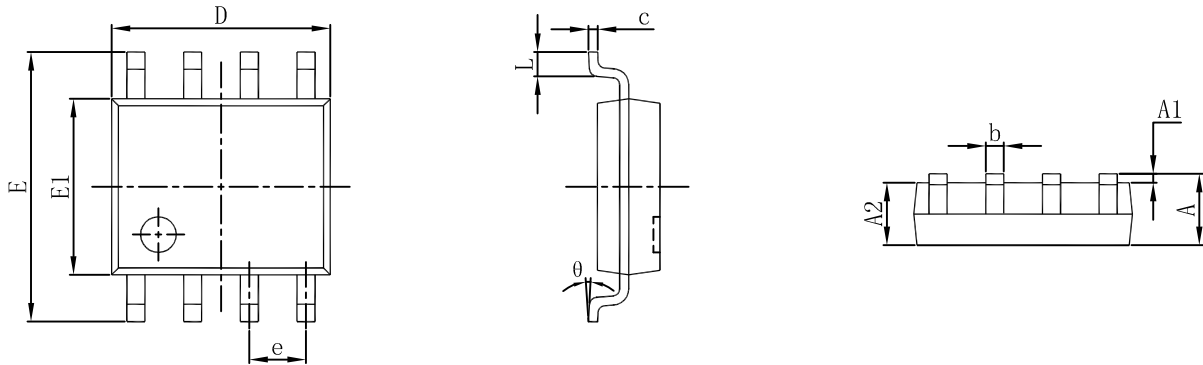


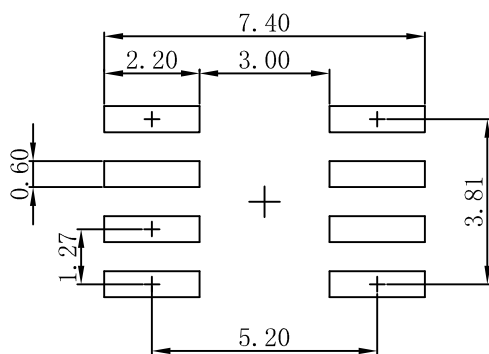
Fig.11 Unclamped Inductive Waveform



SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.



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