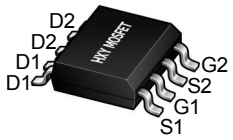
## Description

The DMP3036SSD uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.



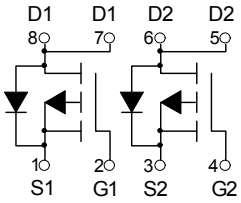

SOP-8

## General Features

$V_{DS}$ = -30V,$I_D$ = -11A

$R_{DS(ON)}$ < 18m @ $V_{GS}$=-10V

$R_{DS(ON)}$ < 27m @ $V_{GS}$=-4.5V




Dual P-Channel MOSFET

## Application

PWM application

Load switch

### Package Marking and Ordering Information

| Product ID | Pack | Brand | Qty(PCS) |
|---|---|---|---|
| DMP3036SSD | SOP-8 | HXY MOSFET | 3000 |

### Absolute Maximum Ratings ($T_A$=25℃unless otherwise noted)

| Symbol | Parameter | Limit | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | -30 | V |
| $V_{GS}$ | Gate-Source Voltage | ±20 | V |
| $I_D$ | Drain Current-Continuous | -11 | A |
| $I_{DM}$ | Drain Current-Pulsed (Note 1) | -40 | A |
| $P_D$ | Maximum Power Dissipation | 3.7 | W |
| $T_J$,$T_{STG}$ | Operating Junction and Storage Temperature Range | -55 To 150 | ℃ |
| $R_{\theta JA}$ | Thermal Resistance,Junction-to-Ambient (Note 2) | 33.8 | ℃/W |

## Electrical Characteristics ($T_J$=25℃ unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_D$= -250μA | -30 | - | - | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$= -30V, $V_{GS}$=0V, | - | - | -1 | μA |
| $I_{GSS}$ | Gate to Body Leakage Current | $V_{DS}$=0V, $V_{GS}$= ±20V | - | - | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$= -250μA | -1.0 | -1.6 | -2.5 | V |
| $R_{DS(on)}$ | Static Drain-Source on-Resistance Note3 | $V_{GS}$= -10V, $I_D$= -10A | - | 14 | 18 | mΩ |
| | | $V_{GS}$= -4.5V, $I_D$= -5A | - | 20 | 27 | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$= -15V, $V_{GS}$=0V, f=1.0MHz | - | 1330 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 183 | - | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 156 | - | pF |
| $Q_g$ | Total Gate Charge | $V_{DS}$= -15V, $I_D$= -5A, $V_{GS}$= -10V | - | 22 | - | nC |
| $Q_{gs}$ | Gate-Source Charge | | - | 1.0 | - | nC |
| $Q_{gd}$ | Gate-Drain(“Miller”) Charge | | - | 1.8 | - | nC |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD}$= -15V, $I_D$= -10A, $V_{GS}$=-10V, $R_{GEN}$=2.5Ω | - | 9 | - | ns |
| $t_r$ | Turn-on Rise Time | | - | 13 | - | ns |
| $t_{d(off)}$ | Turn-off Delay Time | | - | 48 | - | ns |
| $t_f$ | Turn-off Fall Time | | - | 20 | - | ns |
| $I_S$ | Maximum Continuous Drain to Source Diode Forward Current | | - | - | -11 | A |
| $I_{SM}$ | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | -40 | A |
| $V_{SD}$ | Drain to Source Diode Forward Voltage | $V_{GS}$=0V, $I_S$= -15A | - | -0.8 | -1.2 | V |
| trr | Reverse Recovery Time | $T_J$=25℃, $V_{DD}$= -24V,$I_F$=-2.8A, dI/dt=-100A/μs | - | 64 | - | ns |
| Qrr | Reverse Recovery Charge | | - | 25 | - | nC |

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J$=25℃, $V_{GS}$=10V, $R_G$=25Ω, L=0.5mH, $I_{AS}$=-12.7A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

## Typical Performance Characteristics

**Figure1:** Output Characteristics

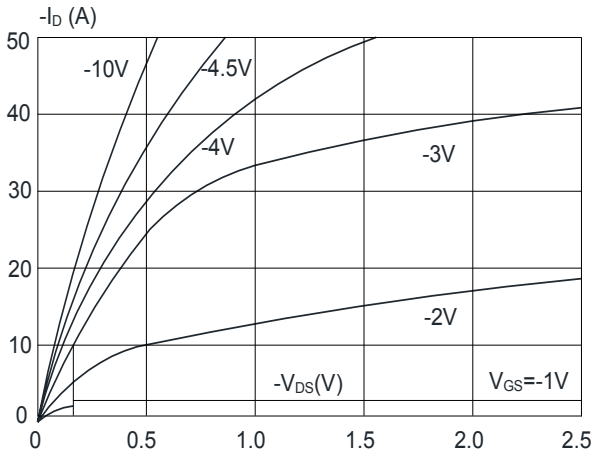



**Figure 2:** Typical Transfer Characteristics

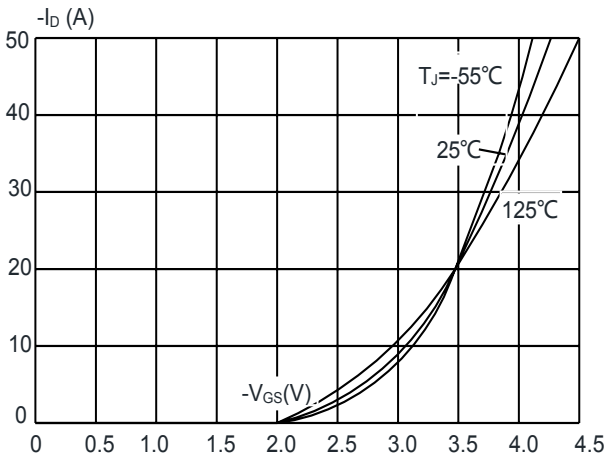



**Figure 3:**On-resistance vs. Drain Current

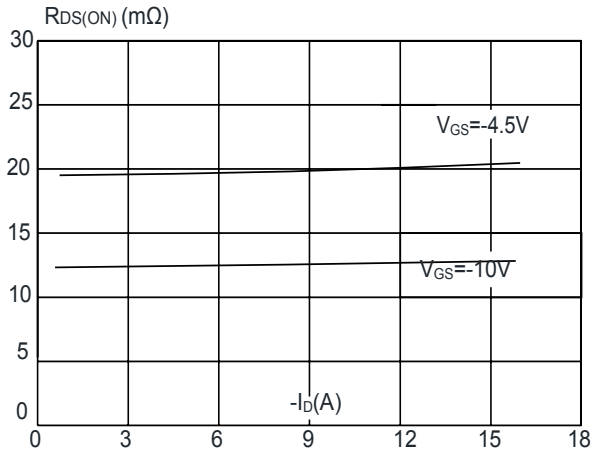



**Figure 4**: Body Diode Characteristics

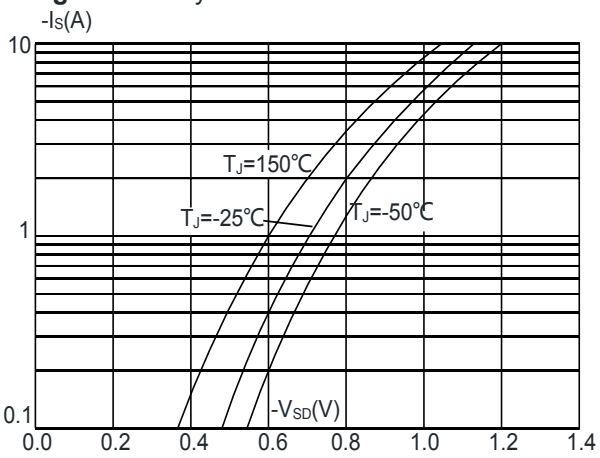



**Figure 5:** Gate Charge Characteristics

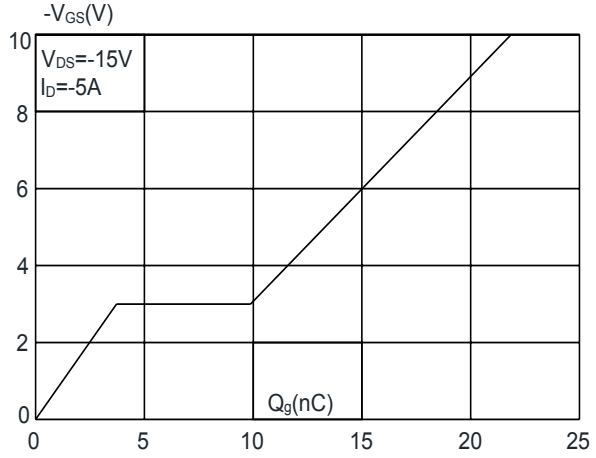



**Figure 6:** Capacitance Characteristics

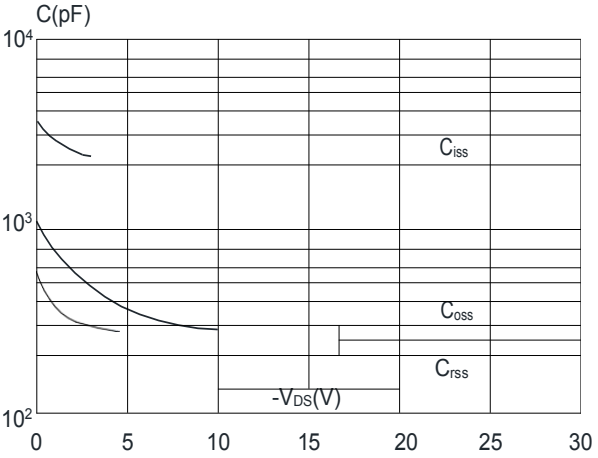


**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature

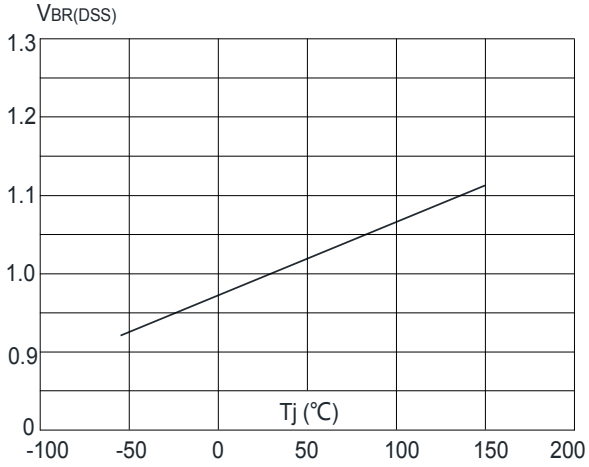



**Figure 8:** Normalized on Resistance vs. Junction Temperature

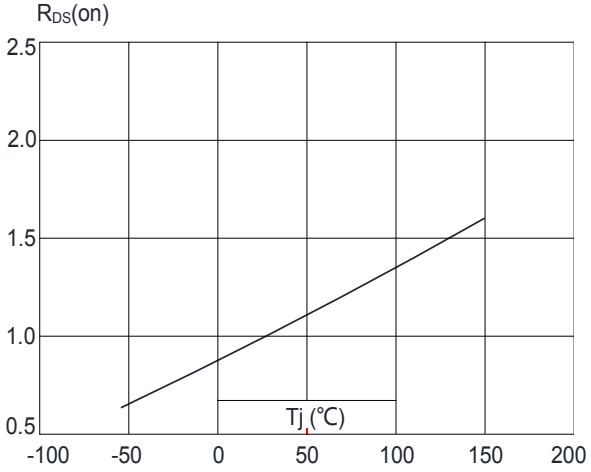



**Figure 9:** Maximum Safe Operating Area

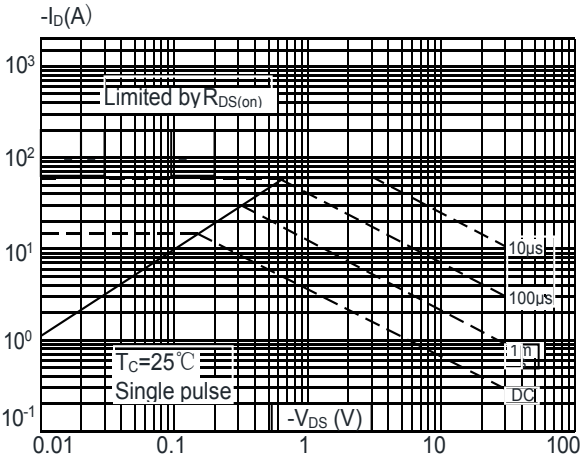



**Figure 10:** Maximum Continuous Drain Current vs. Ambient Temperature

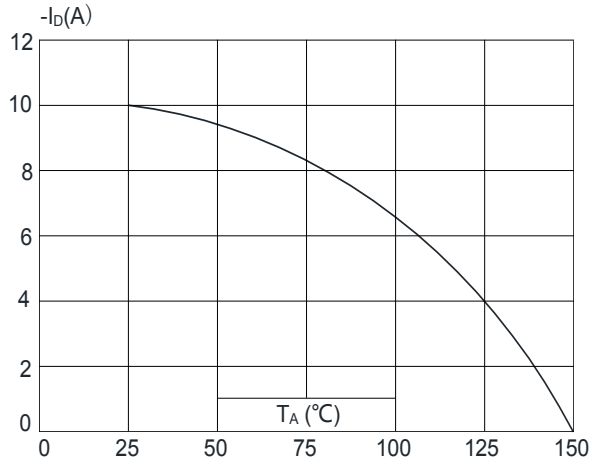
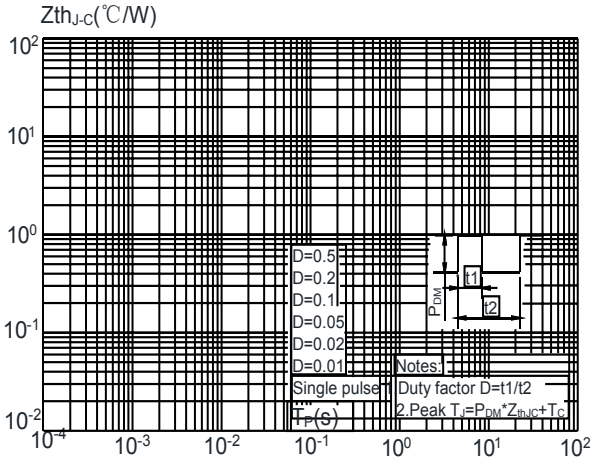
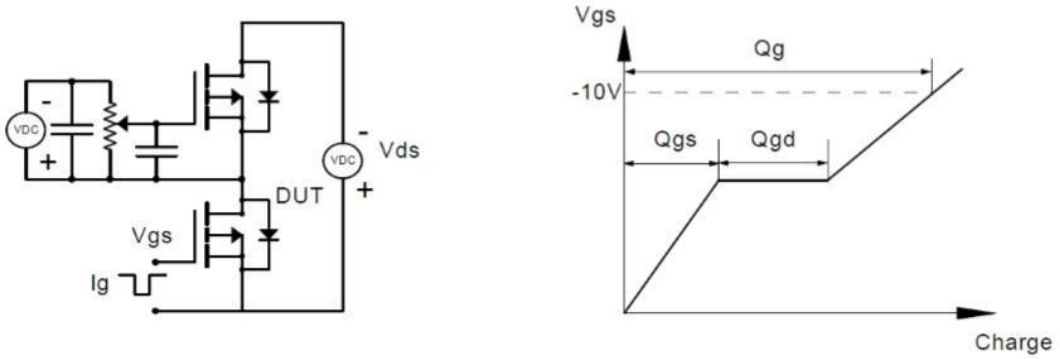



**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case

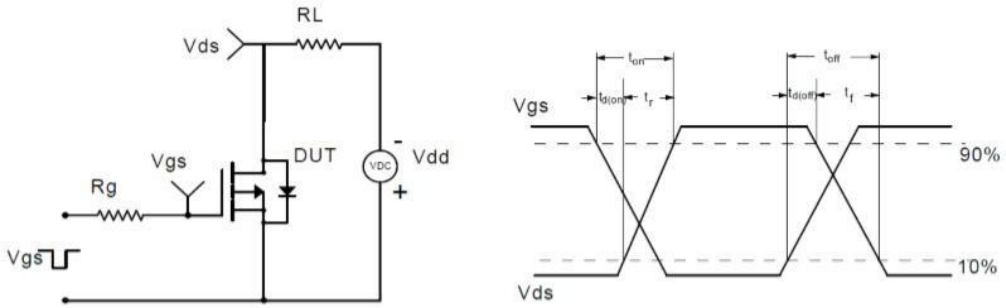


## Test Circuit

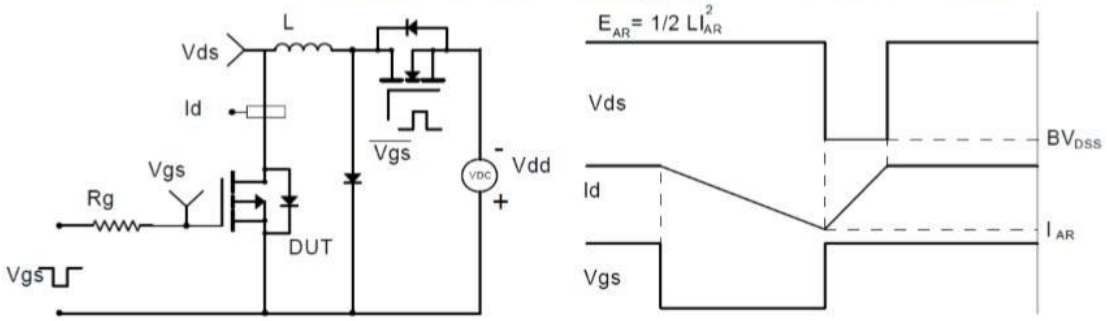
Gate Charge Test Circuit & Waveform



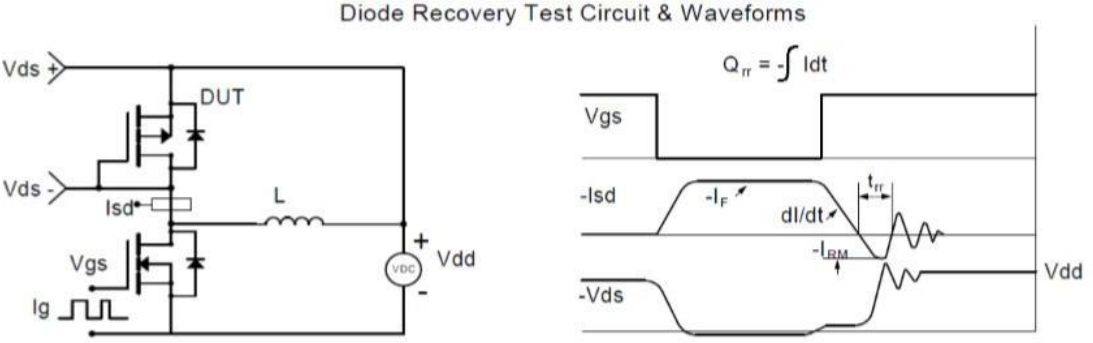

Resistive Switching Test Circuit & Waveforms



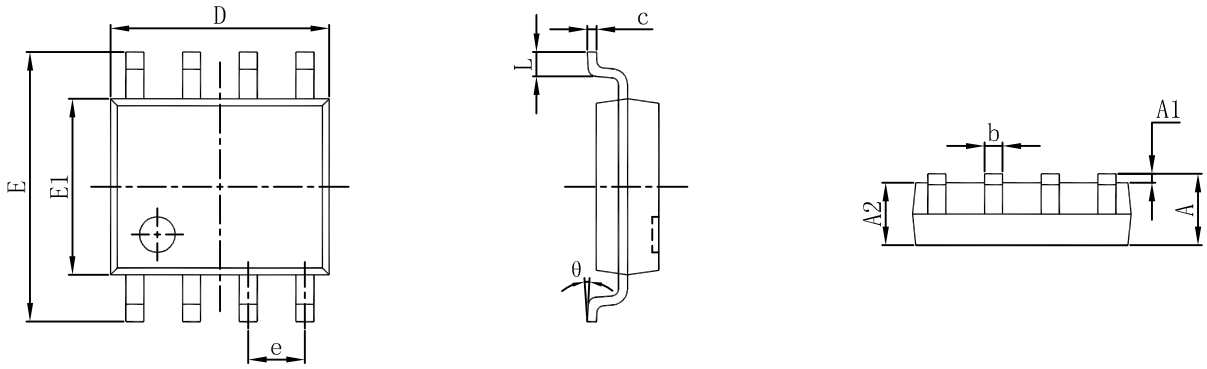

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



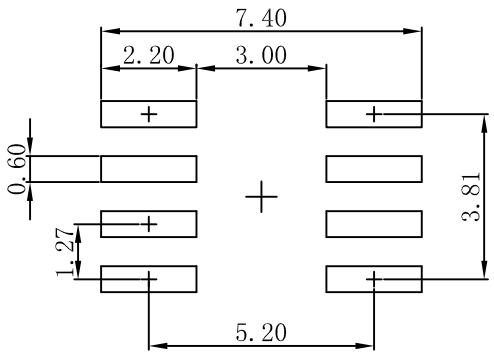

Diode Recovery Test Circuit & Waveforms



## SOP-8 Package Outline Dimensions




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.007 | 0.010 |
| D | 4.800 | 5.000 | 0.189 | 0.197 |
| e | 1.270 (BSC) | | 0.050 (BSC) | |
| E | 5.800 | 6.200 | 0.228 | 0.244 |
| E1 | 3.800 | 4.000 | 0.150 | 0.157 |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |




Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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