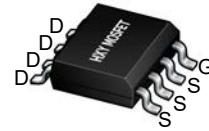




Description

The DMP3056LSS uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8

General Features

$V_{DS} = -30V$ $I_D = -6A$

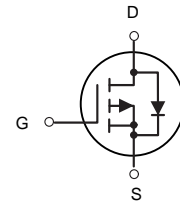
$R_{DS(ON)} < 48m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



P-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
DMP3056LSS	SOP-8	HXY MOSFET	3000

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	- 30	V
V_{GS}	Gate-Source Voltage	±20	V
$I_D@T_A=25^\circ C$	Drain Current ³ , V_{GS} @ 10V	-6	A
I_{DM}	Pulsed Drain Current ¹	-30	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	3.1	W
	Linear Derating Factor	0.02	W/°C
TSTG	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	40	°C/W



Electrical Characteristics Ta = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{DSS}	I _D =-250 μ A, V _{GS} =0V	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V			-1	uA
		V _{DS} =-30V, V _{GS} =0V, T _J =55°C			-5	
Gate-Body leakage current	I _{GSS}	V _{DS} =0V, V _{GS} = ± 12V			± 100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} I _D =-250 μ A	-0.5		-1.3	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-6A			48	m Ω
		V _{GS} =-10V, I _D =-6A T _J =125°C			72	
		V _{GS} =-4.5V, I _D =-4A			57	
		V _{GS} =-2.5V, I _D =-2A			80	
On state drain current	I _{D(ON)}	V _{GS} =-4.5V, V _{DS} =-5V	-30			A
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-6A		19		S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =-15V, f=1MHz		645	780	pF
Output Capacitance	C _{oss}			80		
Reverse Transfer Capacitance	C _{rss}			55		
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz	4		12	Ω
Total Gate Charge	Q _g	V _{GS} =-4.5V, V _{DS} =-15V, I _D =-6A		7		nC
Gate Source Charge	Q _{gs}			1.5		
Gate Drain Charge	Q _{gd}			2.5		
Turn-On DelayTime	t _{d(on)}	V _{GS} =-10V, V _{DS} =-15V, R _L =2.5Ω, R _{GEN} =6Ω		6.5		ns
Turn-On Rise Time	t _r			3.5		
Turn-Off DelayTime	t _{d(off)}			41		
Turn-Off Fall Time	t _f			9		
Body Diode Reverse Recovery Time	t _{rr}	I _F =-6A, di/dt=100A/us		11		nC
Body Diode Reverse Recovery Charge	Q _{rr}			3.5		
Maximum Body-Diode Continuous Current	I _S				-3.5	A
Diode Forward Voltage	V _{SD}	I _S =-1A, V _{GS} =0V			-1	V

Note : The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.



Typical Characteristics

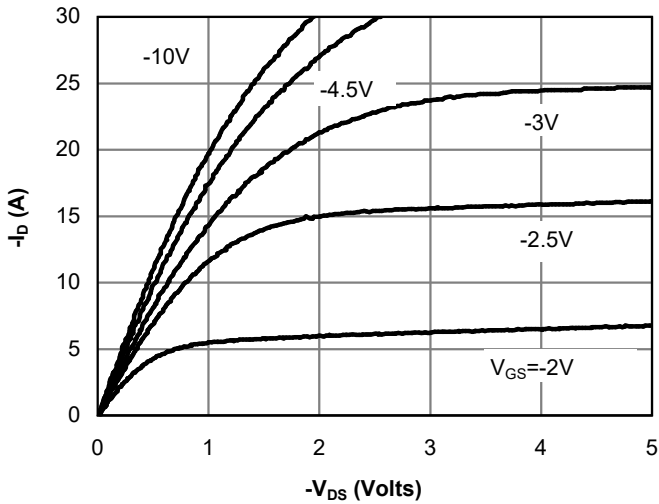


Fig 1: On-Region Characteristics (Note E)

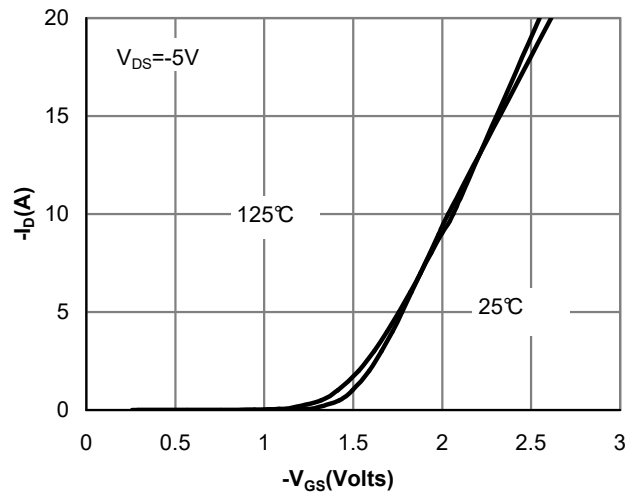


Figure 2: Transfer Characteristics (Note E)

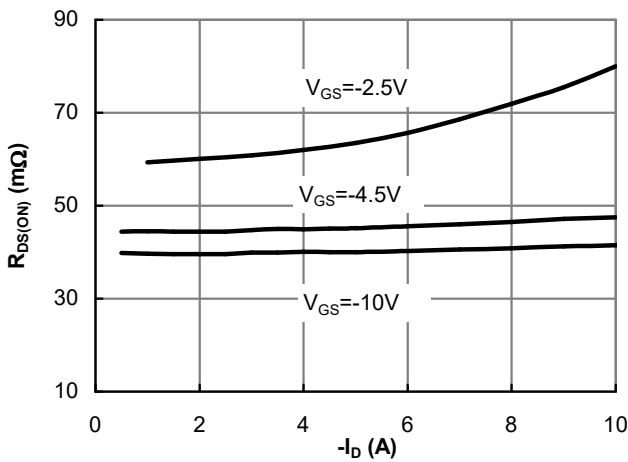


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

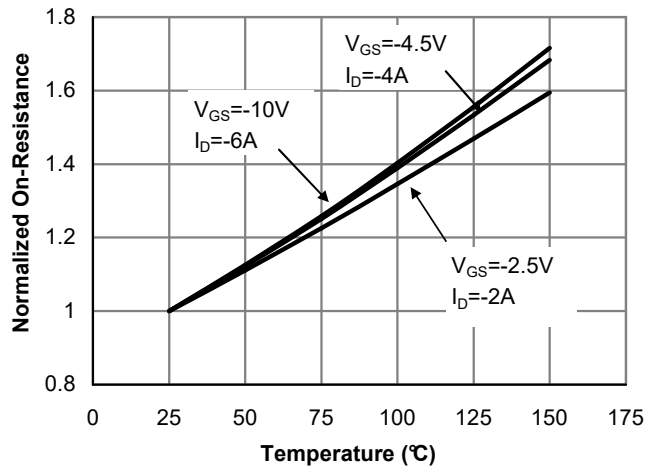


Figure 4: On-Resistance vs. Junction Temperature

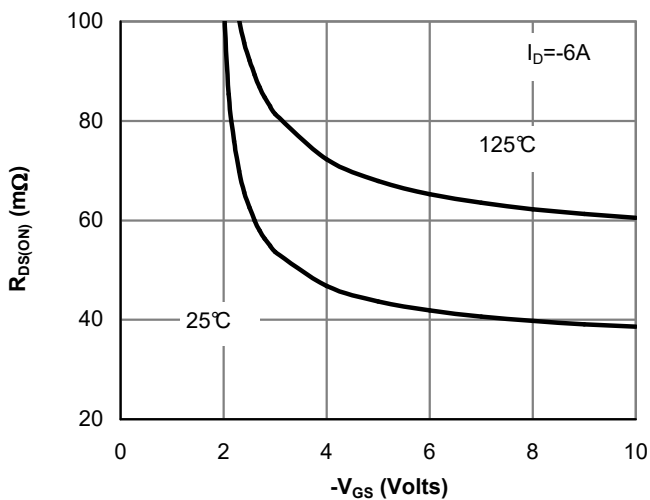


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

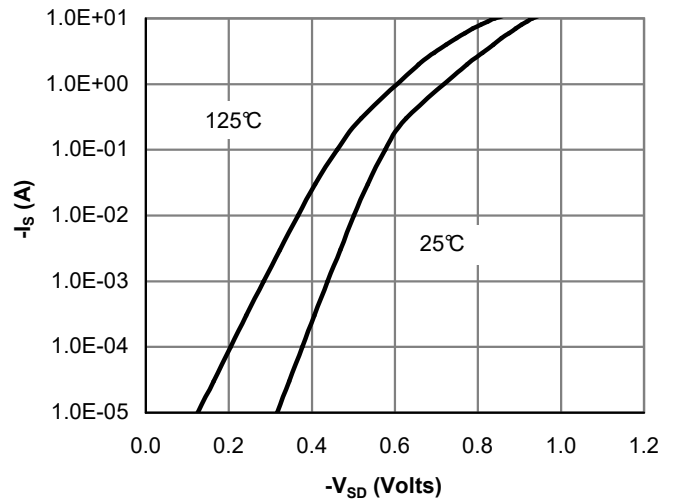


Figure 6: Body-Diode Characteristics (Note E)

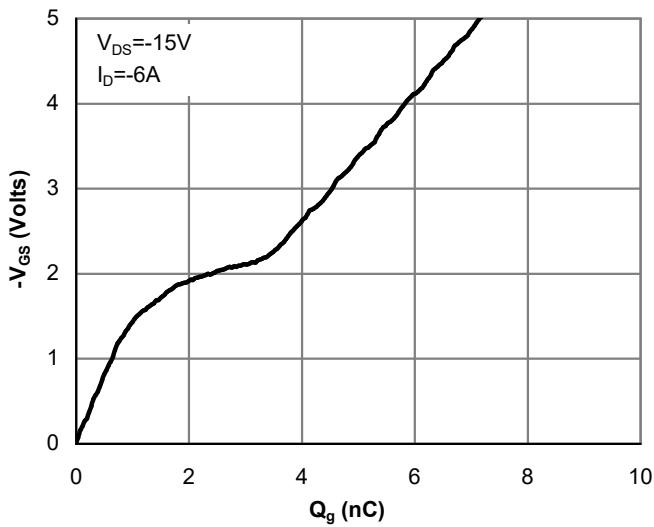


Figure 7: Gate-Charge Characteristics

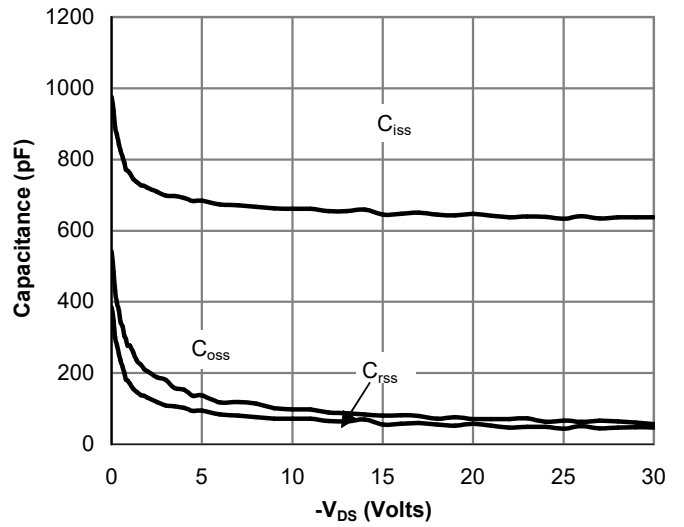


Figure 8: Capacitance Characteristics

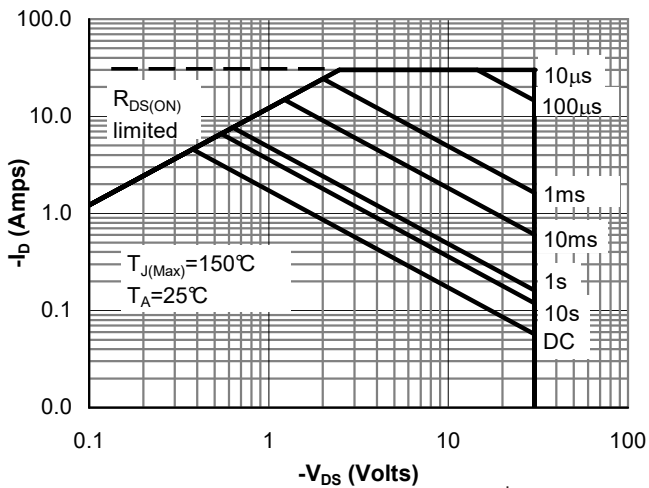


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

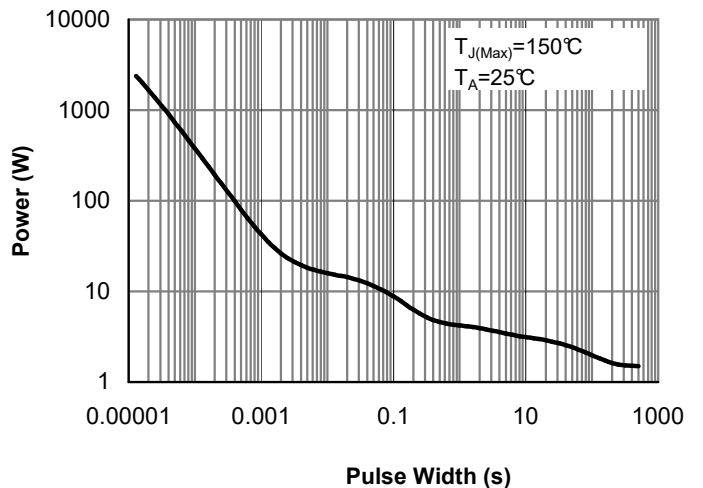


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

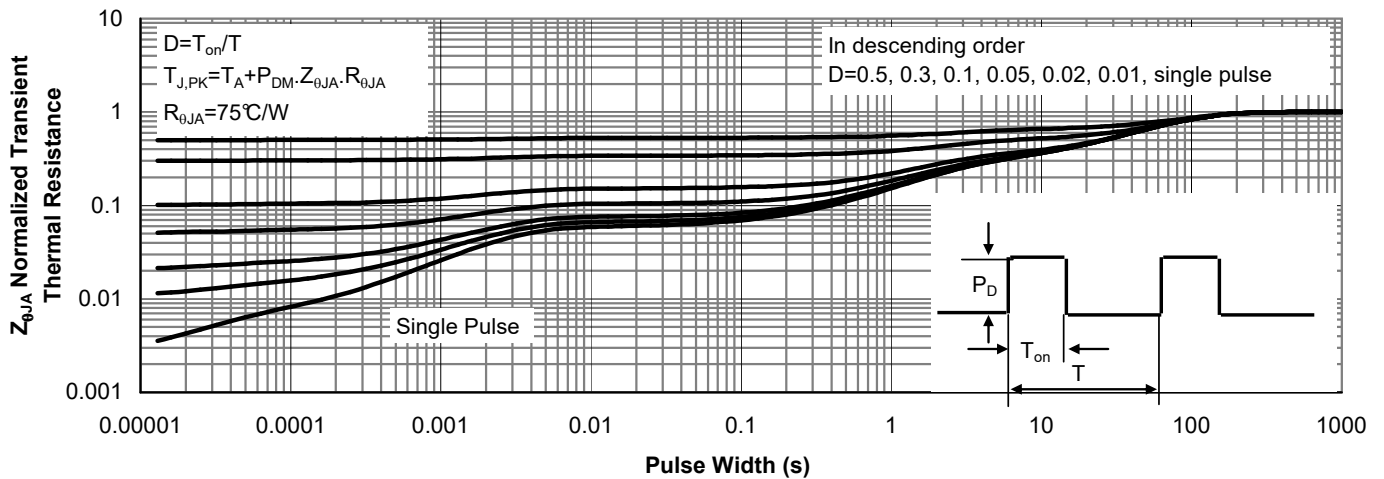
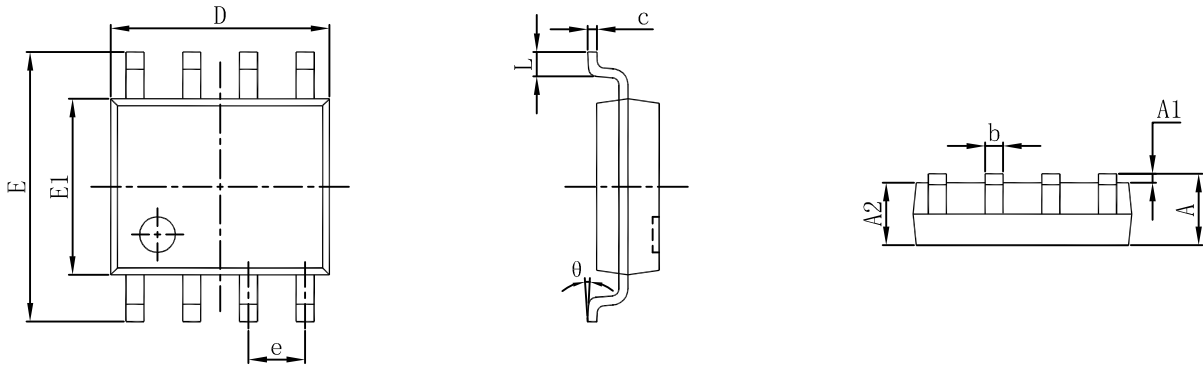


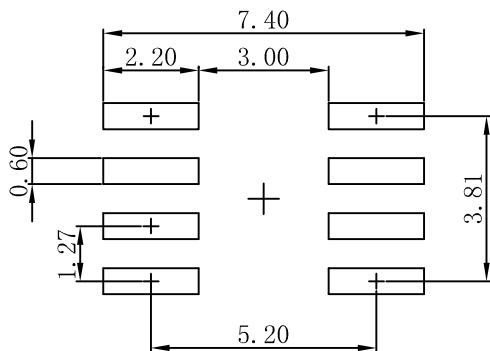
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.



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