

### **Description**

The DMP510DL uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

# D. G. S

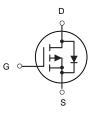
### SOT-23

### **General Features**

 $V_{DS} = -50V, I_{D} = -0.1A$ 

 $R_{DS(ON)}$  <5  $\Omega$  @  $V_{GS}$ =-10V

 $R_{DS(ON)}$  <6  $\Omega$  @  $V_{GS}$ =-4.5V



#### P-Channel MOSFET

### **Application**

Power switching application
Hard switched and high frequency circuits

DC-DC converter

# **Package Marking and Ordering Information**

Product ID	Pack	Brand	Qty(PCS)
DMP510DL	SOT-23	HXY MOSFET	3000

### Absolute Maximum Ratings (T<sub>A</sub>=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	-50	V
Gate-Source Voltage	V <sub>G</sub> s	±20	V
Drain Current-Continuous	I <sub>D</sub>	-0.1	А
Pulsed Drain Current	I <sub>DM</sub>	-0.5	А
Maximum Power Dissipation	P <sub>D</sub>	0.35	W
Operating Junction and Storage Temperature Range	$T_{J}$ , $T_{STG}$	-55 To 150	$^{\circ}$
Thermal Resistance ,Junction-to-Ambient <sup>(Note 2)</sup>	R <sub>0JA</sub>	62.5	°C/W

# DMP510DL

### **Electrical Characteristics (Ta=25℃ unless otherwise specified)**

Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
Static						
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> =0, I <sub>D</sub> =250μA	-50			V
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS}=V_{GS}$ , $I_{D}=-250\mu A$	-0.8		-2.0	V
I <sub>GSS</sub>	Gate-body leakage current	V <sub>DS</sub> =0, V <sub>GS</sub> =±10V			±10	μA
	Zero gate voltage drain current	V <sub>DS</sub> =-50V, V <sub>GS</sub> =0V			-10	μA
I <sub>DSS</sub>		V <sub>DS</sub> =-40V, V <sub>GS</sub> =0V			-100	nA
D	Drain-source on-resistance <sup>a</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-0.13A		2	5	Ω
R <sub>DS(on)</sub>		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-0.13A		2.5	6	Ω
<b>g</b> FS	Forward transconductance <sup>a</sup>	V <sub>DS</sub> =-25V, I <sub>D</sub> =-0.13A	50			mS
$V_{SD}$	Diode forward voltage	I <sub>S</sub> =-0.13A,V <sub>GS</sub> =0V			-1.0	V
Dynamic						
C <sub>iss</sub>	Input capacitance			25		
Coss	Output capacitance	$V_{DS}$ =-25V, $V_{GS}$ =0V, f=1MHz		15		pF
Crss	Reverse transfer capacitance <sup>b</sup>			3.5		
Switching	Switching <sup>b</sup>					
t <sub>d(on)</sub>	Turn-on delay time			16.7		
t <sub>r</sub>	Rise time	V <sub>GS</sub> =-10V,V <sub>DS</sub> =-15V		8.6		nS
t <sub>d(off)</sub>	Turn-off delay time	$I_D$ =-200mA, $R_{GEN}$ =25 $\Omega$		17.9		
t <sub>f</sub>	Fall time			5.3		

Notes:

a. Pulse Test : Pulse width≤300µs, duty cycle ≤2%. b. Guaranteed by design, not subject to producting.



### **TypicalCharacteristics**

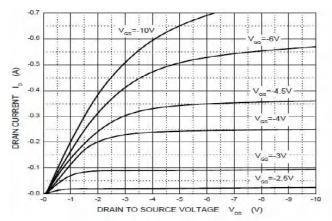


Figure 1. Output Characteristics

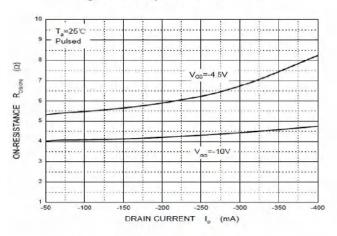


Figure3. Drain-Source on Resistance

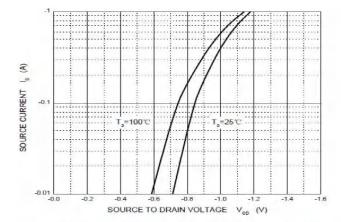


Figure 5. Diode Forward Voltage vs. current

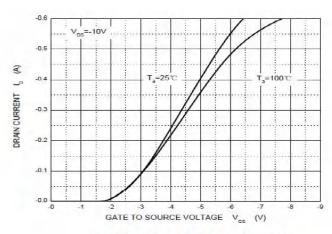


Figure 2. Transfer Characteristics

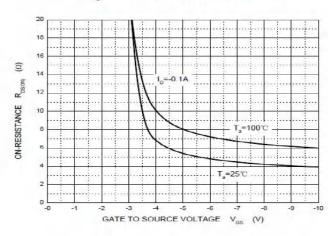


Figure 4. Drain-Source on Resistance

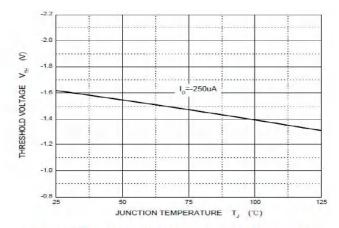
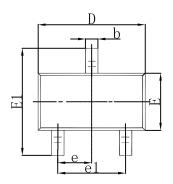
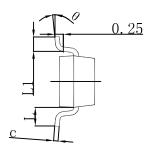


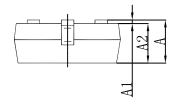
Figure 6. Gate Threshold vs. Junction Temperature



## **SOT-23 Package Outline Dimensions**

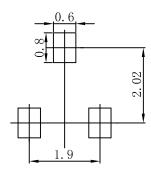






Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
Α	0.900	1.150	0.035	0.045	
A1	0.000	0.100	0.000	0.004	
A2	0.900	1.050	0.035	0.041	
b	0.300	0.500	0.012	0.020	
С	0.080	0.150	0.003	0.006	
D	2.800	3.000	0.110	0.118	
E	1.200	1.400	0.047	0.055	
E1	2.250	2.550	0.089	0.100	
е	0.950 TYP		0.037 TYP		
e1	1.800	2.000	0.071	0.079	
L	0.550 REF		0.022 REF		
L1	0.300	0.500	0.012	0.020	
θ	0°	8°	0°	8°	

## **SOT-23 Suggested Pad Layout**



### Note:

- 1.Controlling dimension:in millimeters.
- 2.General tolerance:± 0.05mm.
  3.The pad layout is for reference purposes only.



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