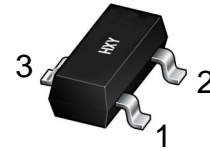




### Discription

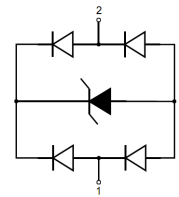
The ESD5302F protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. Excellent clamping capability, low leakage, low capacitance, and fast response time provide best in class protection on designs that are exposed to ESD.



SOT-23

### Features

- Stand-off voltage: 5V Max
- Transient protection for each line according to IEC61000-4-2 (ESD):  $\pm 20\text{kV}$  (contact and air discharge)  
IEC61000-4-4 (EFT): 40A (5/50ns)  
IEC61000-4-5 (surge): 4A (8/20 $\mu\text{s}$ )
- Ultra-low capacitance:  $C_J = 0.4\text{pF}$  typ.
- Ultra-low leakage current:  $I_R < 1\text{nA}$  typ.
- Low clamping voltage:  $V_{CL} = 20\text{V}$  @  $I_{PP} = 16\text{A}$ (TLP)
- Solid-state silicon technology



Circuit Diagram

### Ordering information

Product ID	Pack	Qty(PCS)
ESD5302F	SOT-23	3000

### Absolute Ratings ( $T_{amb}=25^{\circ}\text{C}$ )

Symbol	Parameter	Value	Units
$P_{PP}$	Peak Pulse Power ( $t_p = 8/20\mu\text{s}$ )	60	W
$T_L$	Maximum lead temperature for soldering during 10s	260	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-55 to +150	$^{\circ}\text{C}$
$T_{op}$	Operating Temperature Range	-40 to +125	$^{\circ}\text{C}$
$T_j$	Maximum junction temperature	150	$^{\circ}\text{C}$
	IEC61000-4-2 (ESD)	air discharge contact discharge	$\pm 20$ $\pm 20$ KV



**Electrical characteristics** ( $T_A=25\text{ }^\circ\text{C}$ , unless otherwise noted)

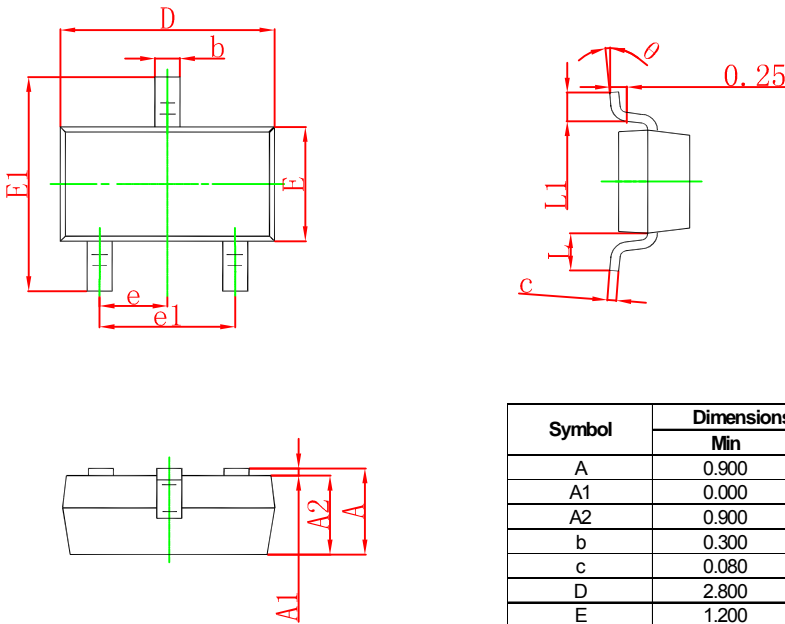
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse maximum working voltage	$V_{RWM}$				5.0	V
Reverse leakage current	$I_R$	$V_{RWM} = 5V$		<1	100	nA
Reverse breakdown voltage	$V_{BR}$	$I_T = 1mA$	7.0	8.0	9.0	V
Forward voltage	$V_F$	$I_T = 10mA$	0.6	0.9	1.2	V
Clamping voltage <sup>1)</sup>	$V_{CL}$	$I_{PP} = 16A, t_p = 100ns$		20		V
Dynamic resistance <sup>1)</sup>	$R_{DYN}$			0.65		$\Omega$
Clamping voltage <sup>2)</sup>	$V_{CL}$	$I_{PP} = 1A, t_p = 8/20\mu s$			11	V
		$I_{PP} = 4A, t_p = 8/20\mu s$			15	V
Junction capacitance	$C_J$	$V_R = 0V, f = 1MHz$ Any I/O pin to GND		0.40	0.65	pF
		$V_R = 0V, f = 1MHz$ Between any I/O pin		0.25	0.40	pF

Notes:

- 1) TLP parameter:  $Z_0 = 50\ \Omega$ ,  $t_p = 100ns$ ,  $t_r = 2ns$ , averaging window from 60ns to 80ns.  $R_{DYN}$  is calculated from 4A to 16A.
- 2) According to IEC61000-4-5.

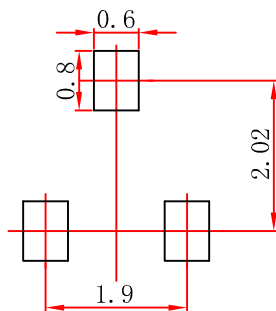


### SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

### SOT-23 Suggested Pad Layout



- Note:
1. Controlling dimension: in millimeters.
  2. General tolerance:  $\pm 0.05\text{mm}$ .
  3. The pad layout is for reference purposes only.



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