



## Description

The FDS6679AZ uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8

## General Features

$V_{DS} = -30V$   $I_D = -15A$

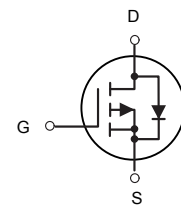
$R_{DS(ON)} < 8.7m\Omega @ V_{GS}=10V$

## Application

Battery protection

Load switch

Uninterruptible power supply



P-Channel MOSFET

## Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
FDS6679AZ	SOP-8	HXY MOSFET	3000

## Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-15	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-11	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-56	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	151	mJ
$I_{AS}$	Avalanche Current	-55	A
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>4</sup>	1.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup> ( $t \leq 10s$ )	40	$^\circ C/W$
	Thermal Resistance Junction-Ambient <sup>1</sup>	75	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	24	$^\circ C/W$



**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-30	---	---	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =-1mA	---	-0.018	---	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V , I <sub>D</sub> =-12A	---	5.8	8.7	mΩ
		V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-10A	---	8.5	13.5	
V <sub>GS(th)</sub>	Gate Threshold Voltage		-1.2	---	-2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	---	5.04	---	mV/°C
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-24V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C	---	---	-1	uA
		V <sub>DS</sub> =-24V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C	---	---	-5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =-5V , I <sub>D</sub> =-12A	---	25	---	S
Q <sub>g</sub>	Total Gate Charge (-4.5V)		---	30	---	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =-15V , V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-12A	---	10	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	10.4	---	
T <sub>d(on)</sub>	Turn-On Delay Time		---	9.4	---	ns
T <sub>r</sub>	Rise Time	V <sub>DD</sub> =-15V , V <sub>GS</sub> =-10V , R <sub>G</sub> =3.3 ,	---	10.2	---	
T <sub>d(off)</sub>	Turn-Off Delay Time	I <sub>D</sub> =-1A	---	117	---	
T <sub>f</sub>	Fall Time		---	24	---	
C <sub>iss</sub>	Input Capacitance		---	3448	---	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =-15V , V <sub>GS</sub> =0V , f=1MHz	---	508	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	421	---	
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>		---	---	-14	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	---	---	-56	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , T <sub>J</sub> =25°C	---	---	-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> =-10A , di/dt=100A/μs ,	---	19.4	---	nS
Q <sub>rr</sub>	Reverse Recovery Charge	T <sub>J</sub> =25°C	---	9.1	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=-25V,V<sub>GS</sub>=-10V,L=0.1mH,I<sub>AS</sub>=-55A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.



### Typical Characteristics

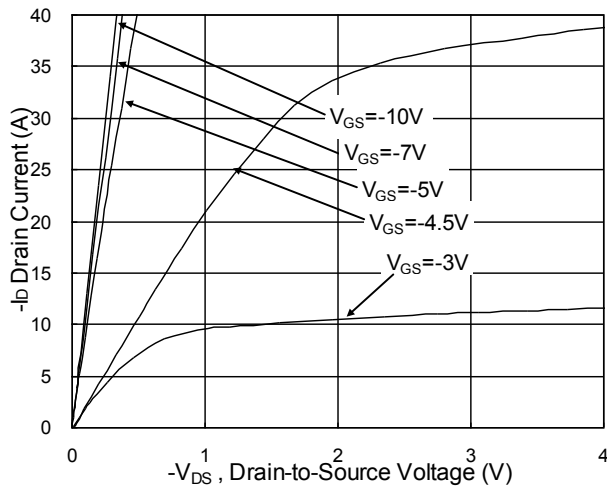


Fig.1 Typical Output Characteristics

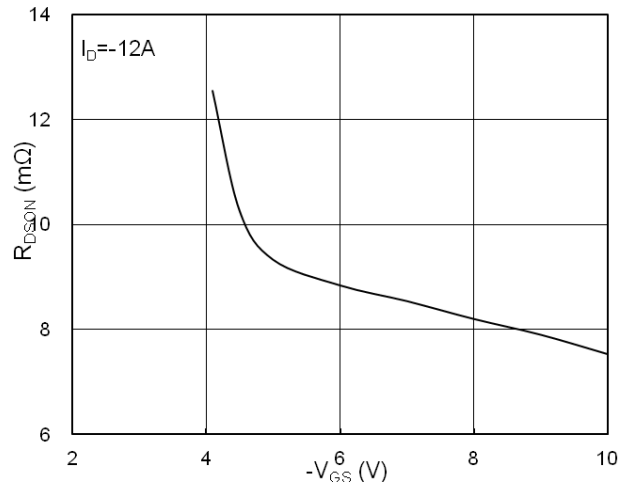


Fig.2 On-Resistance v.s Gate-Source

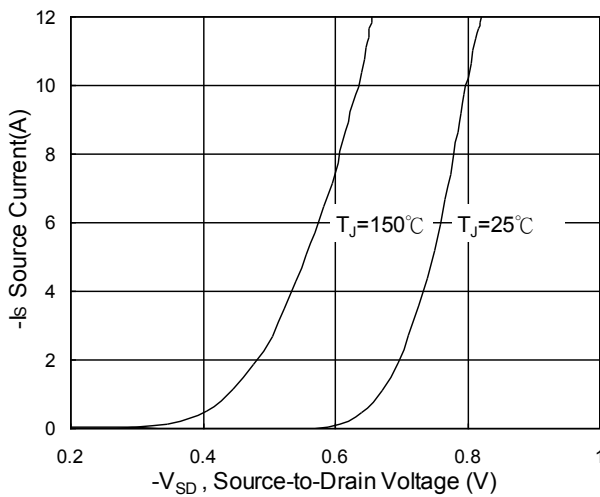


Fig.3 Forward Characteristics Of Reverse

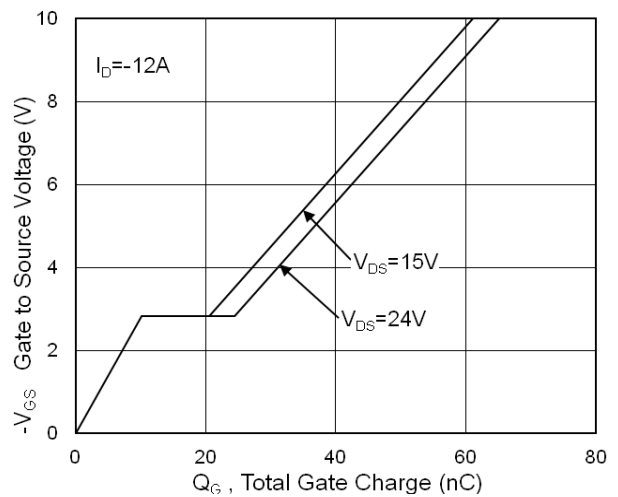


Fig.4 Gate-Charge Characteristics

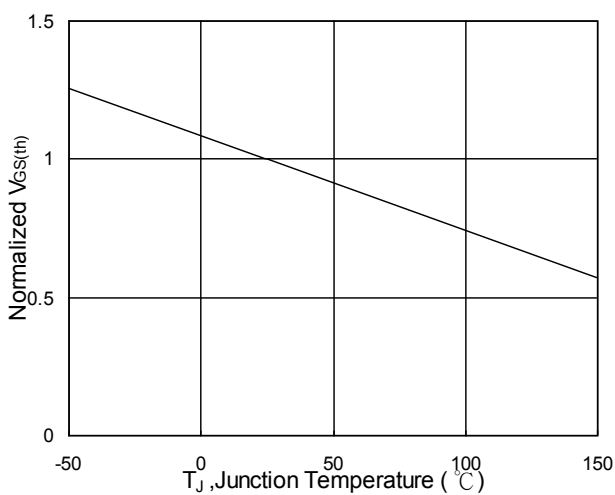


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

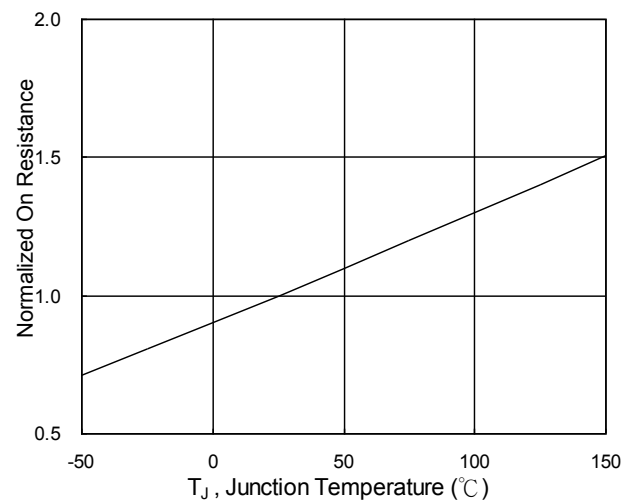


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$

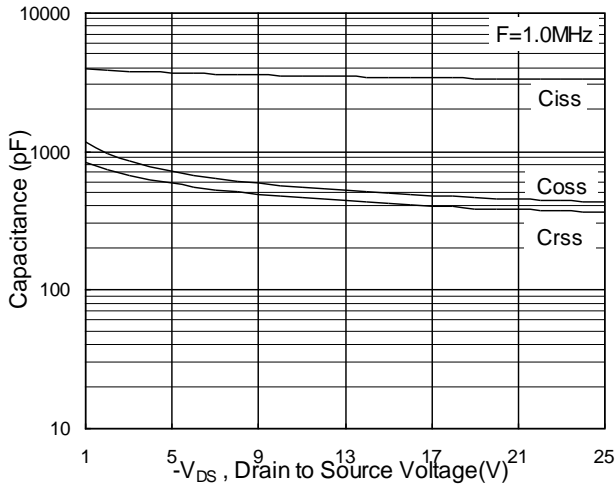


Fig.7 Capacitance

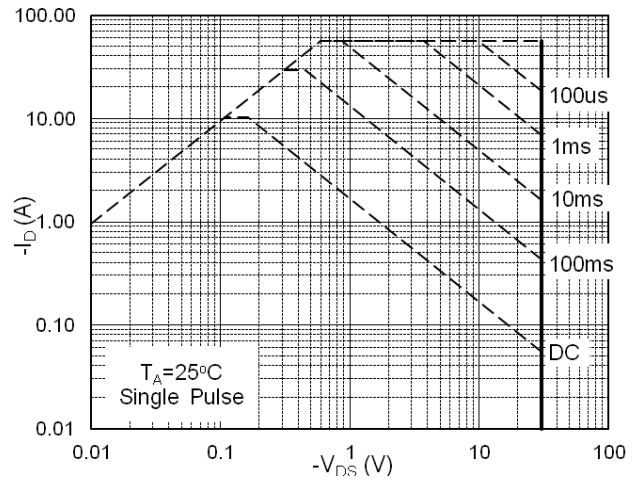


Fig.8 Safe Operating Area

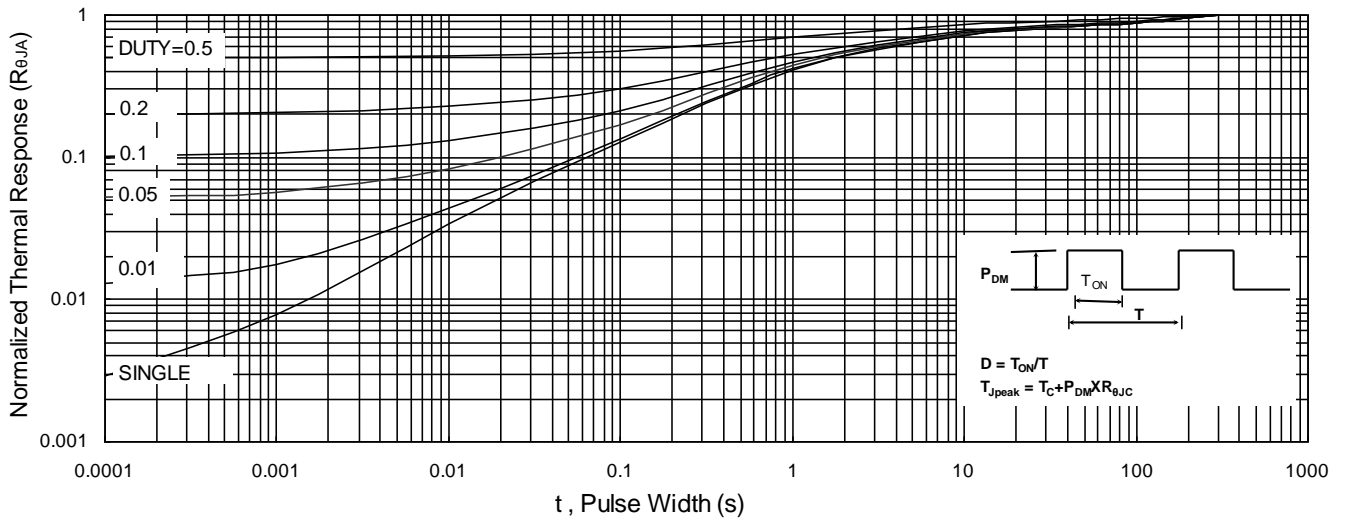


Fig.9 Normalized Maximum Transient Thermal Impedance

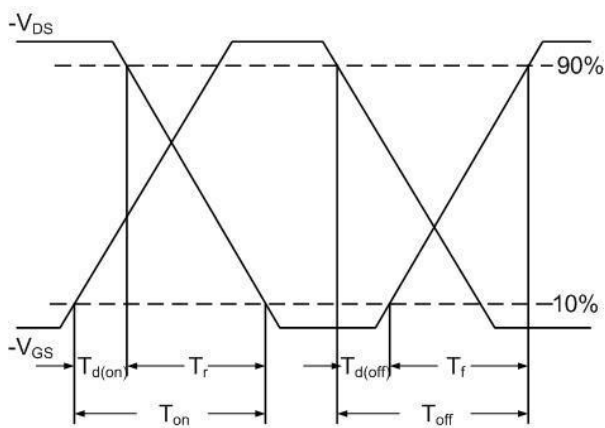


Fig.10 Switching Time Waveform

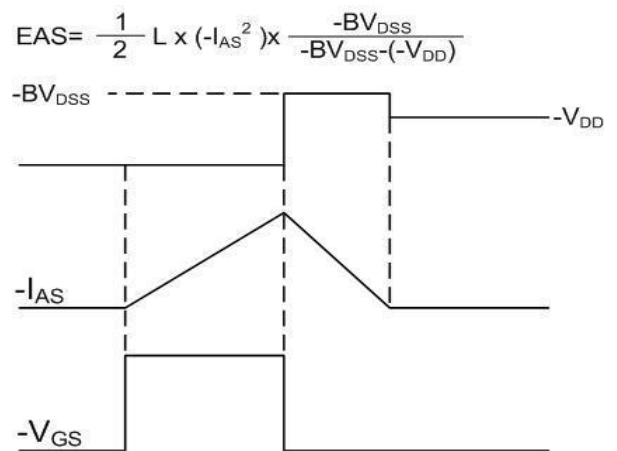
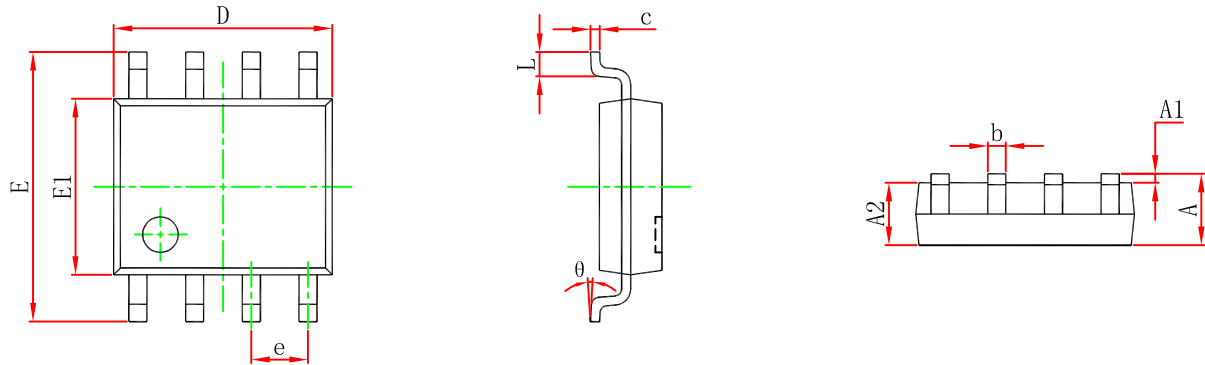


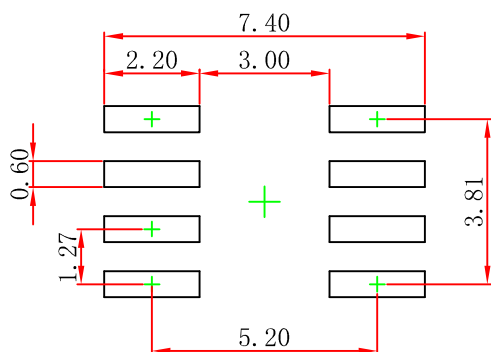
Fig.11 Unclamped Inductive Switching Waveform



### SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.05\text{mm}$ .  
 3. The pad layout is for reference purposes only.



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