DESCRIPTION

The HSN75176ADR used for RS-485/RS-422 communication is a 10Mbps high-speed transceiver for half duplex communication, which includes one driver Device and a receiver.

Equippedwith ± 8kV human mode ESD protection and failure protection circuit,ensuring that when the receiver input is open or short circuited Receiver output logic high level.

If all transmitters attached to the terminal matching bus are disabled (high resistance), the receiver will output logic high Level.

The HSN75176ADR driver does not limit the swing rate and can ensure a communication rate of up to 10Mbps.

HSN75176ADR has a receiver with 1 Unit load input impedance, up to 32 transceivers can be connected to the bus.

In addition, HSN75176ADR also has an built-in over-temperature protection circuit to ensure the chip is not damaged under high temperature conditions.

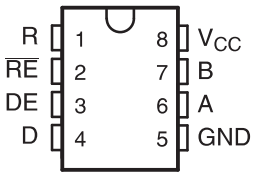
FEATURES

- Provide low current shutdown mode
- Provide industry standard 8-pin SOP packaging
- Up to 32 transceivers are allowed to be mounted on the bus
- True fail safe receiver compatible with EIA/TIA-485
- Built in over temperature protection circuit ensures that the chip is not damaged due to High temperatures
- Provide enhanced ESD protection for RS-485/ RS-422 A/B pins

APPLICATIONS

- SCSI "Fast 40" Drivers and Receivers
- Motor Controller/Position Encoder Systems
- Factory Automation

PIN CONFIGURATION

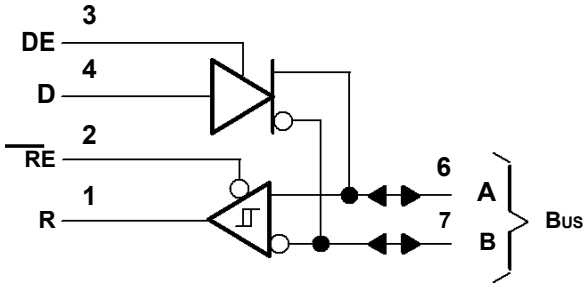


SOP-8

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Active-HIGH driver enable
GND	5	Reference potential	Local device ground
R	1	Digital output	Receiver data output
$\overline{RE}$	2	Digital input	Active-LOW receiver enable
V_{CC}	8	Supply	4.75-V to 5.25-V supply

LOGIC DIAGRAM



FEATUER DESCRIPTION

DRIVER FUNCTION TABLE

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

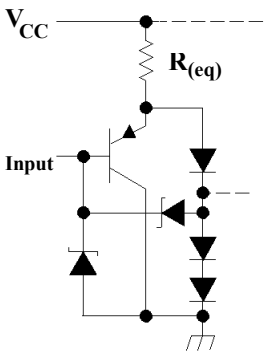
H = high level,
L = low level,
X = irrelevant,
Z = high impedance (off)

RECEIVER FUNCTION TABLE

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	?

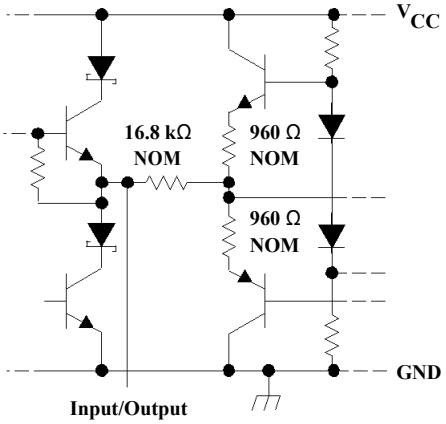
H = high level,
L = low level,
? = indeterminate,
X = irrelevant,
Z = high impedance (off)

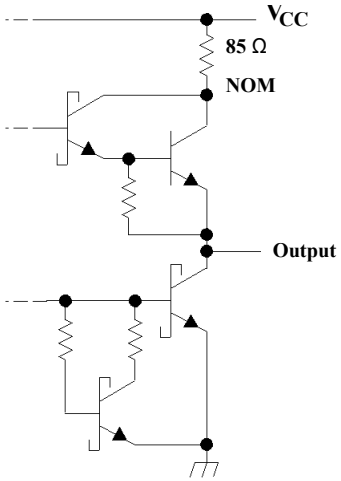
EQUIVALENT OF EACH INPUT



Driver input: $R_{(eq)}$ = 3 kΩ NOM
Enable inputs: $R_{(eq)}$ = 8 kΩ NOM

$R_{(eq)}$ = Equivalent Resistor





ABSOLUTE MAXIMUM RATINGS

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)
over operating free-air temperature range (unless otherwise noted)(1)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{cc}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	–10	15	V
V_I	Enable input voltage		5.5	V
θ_{JA}	Package thermal impedance(3)(4)		85	°C/W
T_J	Operating virtual junction temperature		150	℃
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	℃
T_{stg}	Storage temperature range	–65	150	℃

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
(3) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)				12	V
					–7	
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage(1)				±12	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	μA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature		0		70	℃

(1) Differential input/output bus voltage is measured at the noninverting terminal A, with respect to the inverting terminal B.

DRVER SECTION
Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5	3.6	6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω		1/2 V_{OD1} or 2 (3)			V
		R_L = 54 Ω		1.5	2.5	5	
V_{OD3}	Differential output voltage	See (4)		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(5)	R_L = 54 Ω or 100 Ω				±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω				+3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(5)	R_L = 54 Ω or 100 Ω				±0.2	V
I_O	Output current	Output disabled(6)	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	μA
I_{OS}	Short-circuit output current	V_O = –7 V				–250	mA
		V_O = 0				–150	
		$V_O = V_{CC}$				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

(1) The power-off measurement in ANSI Standard TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
(4) See ANSI Standard TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.
(5) $|V_{OD}|$ and $|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(6) This applies for both power on and off; refer to ANSI Standard TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

Switching Characteristics

V_{CC} = 5 V, R_L = 110 Ω, T_A = 25°C (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω		15	22	ns
$t_{t(OD)}$	Differential-output transition time	R_L = 54 Ω		20	30	ns
t_{PZH}	Output enable time to high level			85	120	ns
t_{PZL}	Output enable time to low level			40	60	ns
t_{PHZ}	Output disable time from high level			150	250	ns
t_{PLZ}	Output disable time from low level			20	30	ns

Symbol Equivalents

DATA SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (test termination measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION
Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V, I_O = –0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O= 0.5 V, I_O = 8 mA		–0.2(2)			V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Enable Input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –400 uA		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V(3)	V_I = 12 V			1	mA
			V_I = –7 V			–0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				–100	μA
r_I	Input resistance	V_I = 12 V		12			kΩ
I_{OS}	Short-circuit output current			–15		–85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for both power on and power off. Refer to EIA Standard TIA/EIA-485-A for exact conditions.

Switching Characteristics

V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 to 3 V		21	35	ns
t_{PHL}	Propagation delay time, high- to low-level output			23	35	
t_{PZH}	Output enable time to high level			10	20	ns
t_{PZL}	Output enable time to low level			12	20	
t_{PHZ}	Output disable time from high level			20	35	ns
t_{PLZ}	Output disable time from low level			17	25	

Parameter Measurement Information

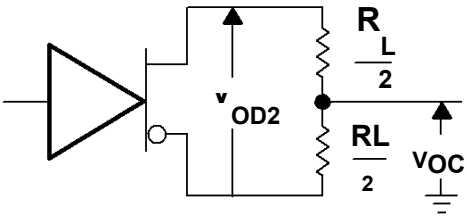


Figure 1. Driver V_{OD} and V_{OC}

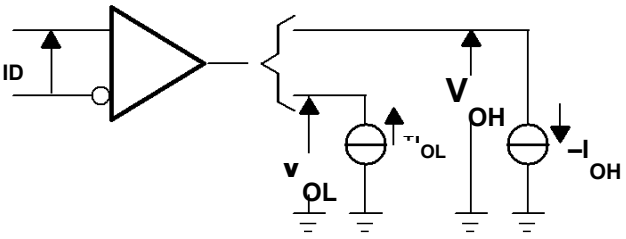
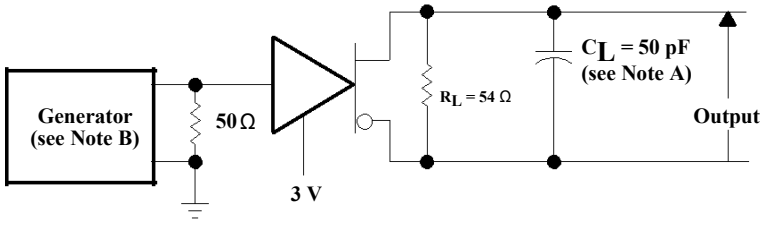
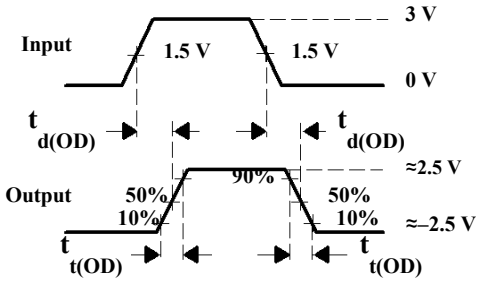


Figure 2. Receiver V_{OH} and V_{OL}



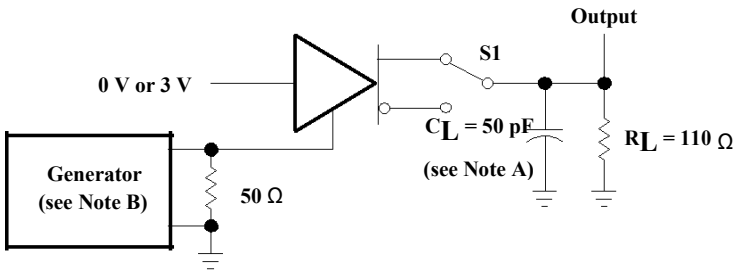
TEST CIRCUIT



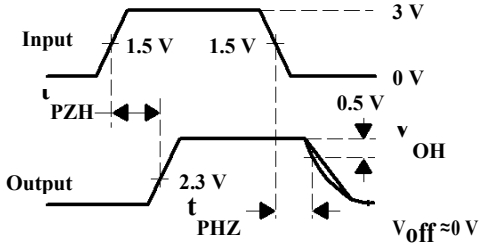
VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

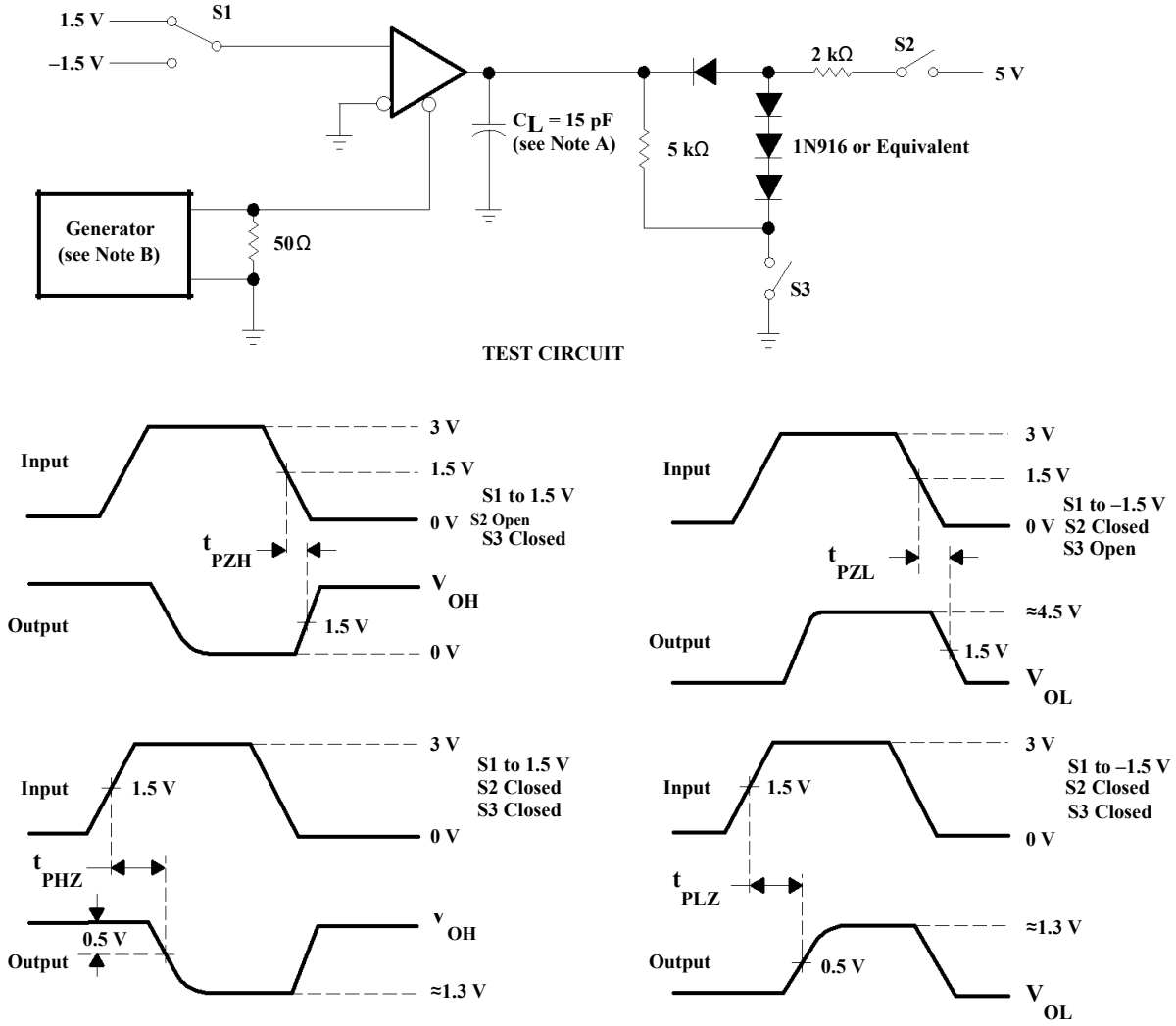


VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 4. Driver Test Circuit and Voltage Waveforms

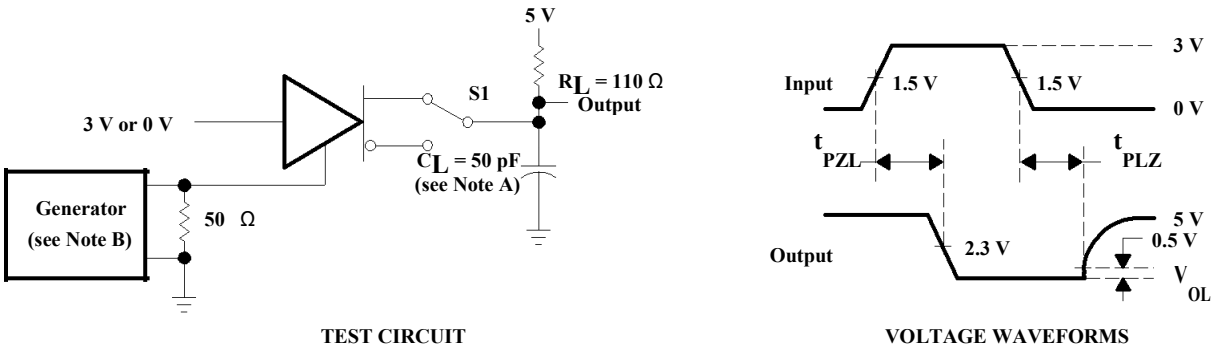
Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

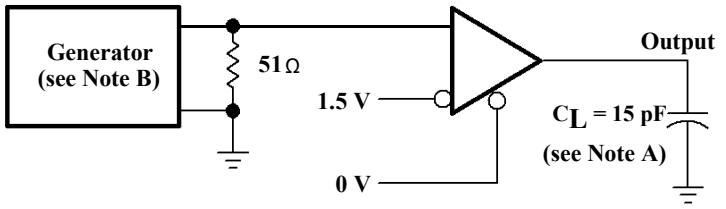
Figure 5. Receiver Test Circuit and Voltage Waveforms



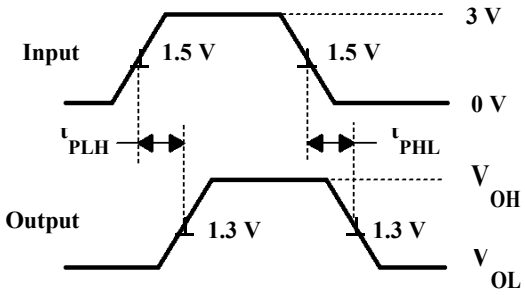
A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 6. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 7. Receiver Test Circuit and Voltage Waveforms

TYPOCAL CHARACTERISTICS

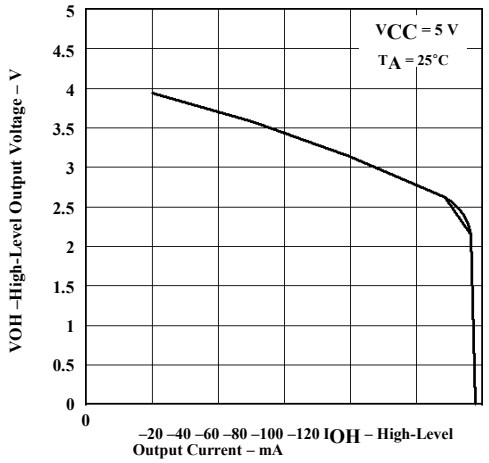


Figure 8. Driver High-Level Output Voltage vs High-Level Output Current

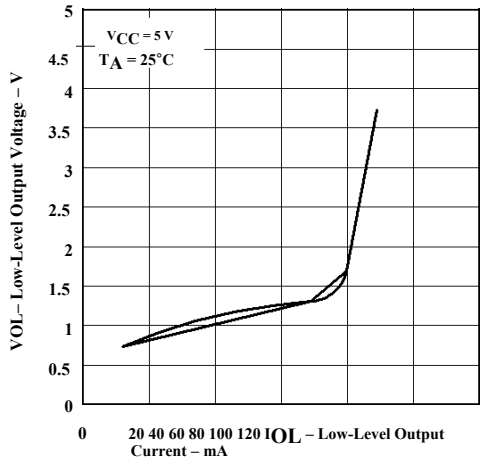


Figure 9. Driver Low-Level Output Voltage vs Low-Level Output Current

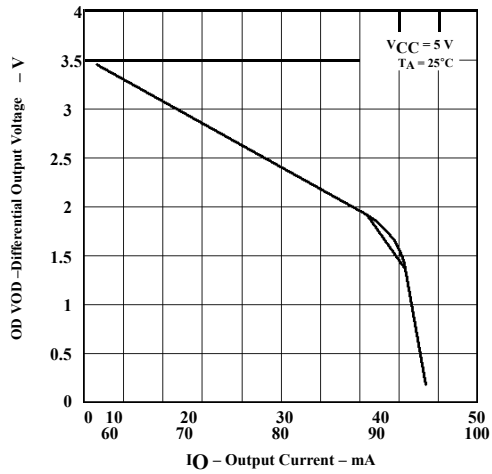


Figure 10. Driver Differential Output Voltage vs Output Current

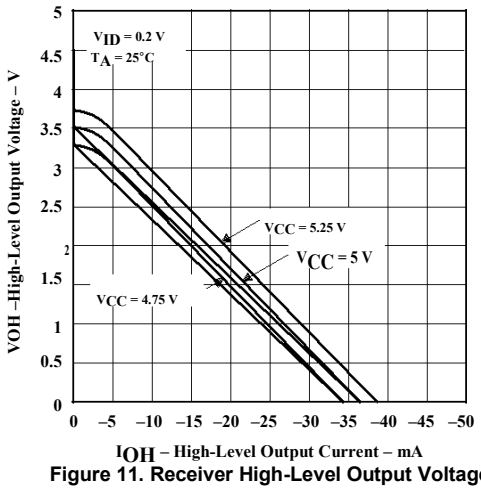


Figure 11. Receiver High-Level Output Voltage vs High-Level Output Current

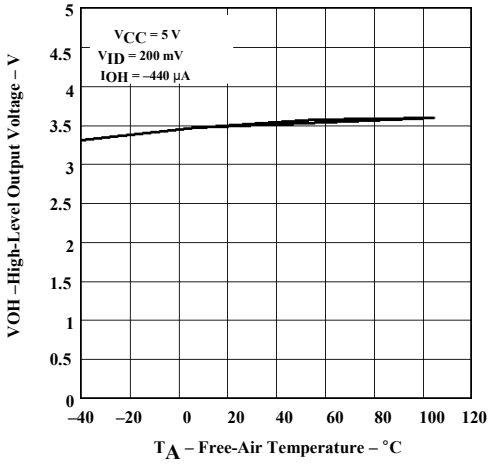


Figure 12. VOH-High-Level Output Voltage vs Free-Air Temperature

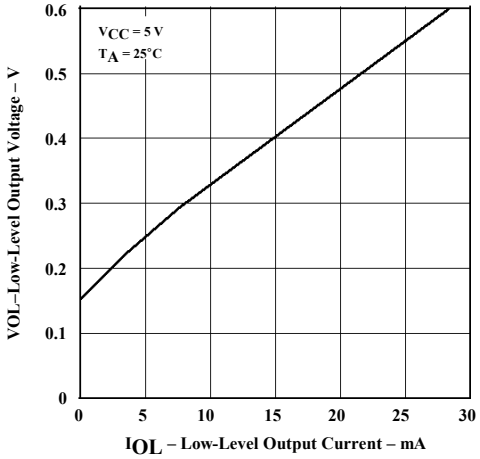


Figure 13. VOL-Low-Level Output Voltage vs Low -Level Output Current

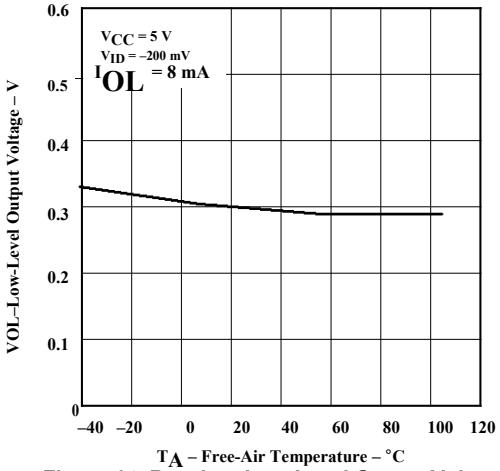


Figure 14. Receiver Low-Level Output Voltage vs Free-Air Temperature

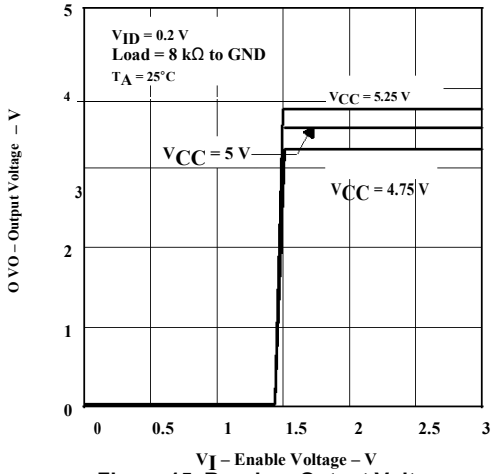


Figure 15. Receiver Output Voltage vs Enable Voltage

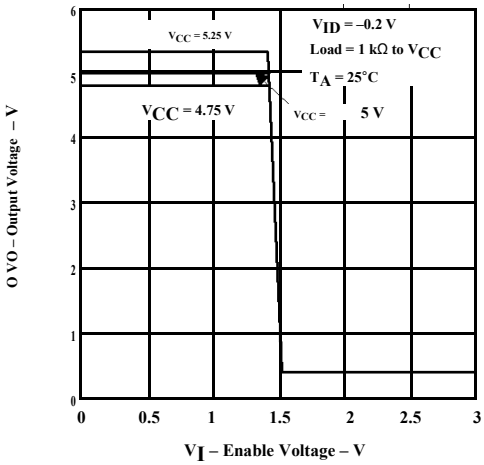
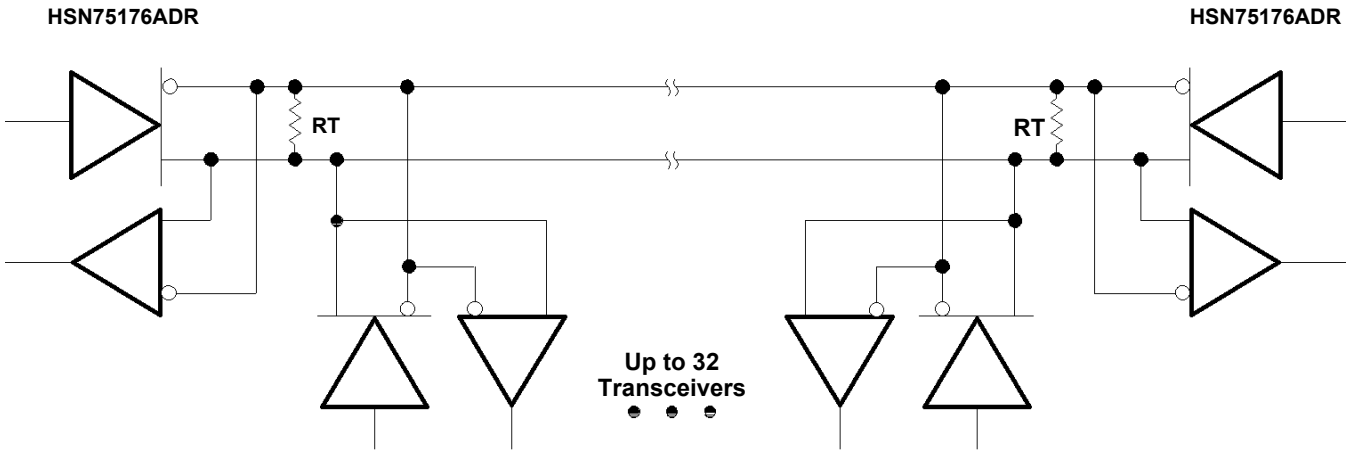


Figure 16. Receiver Output Voltage vs Enable Voltage

APPLICATION INFORMATION

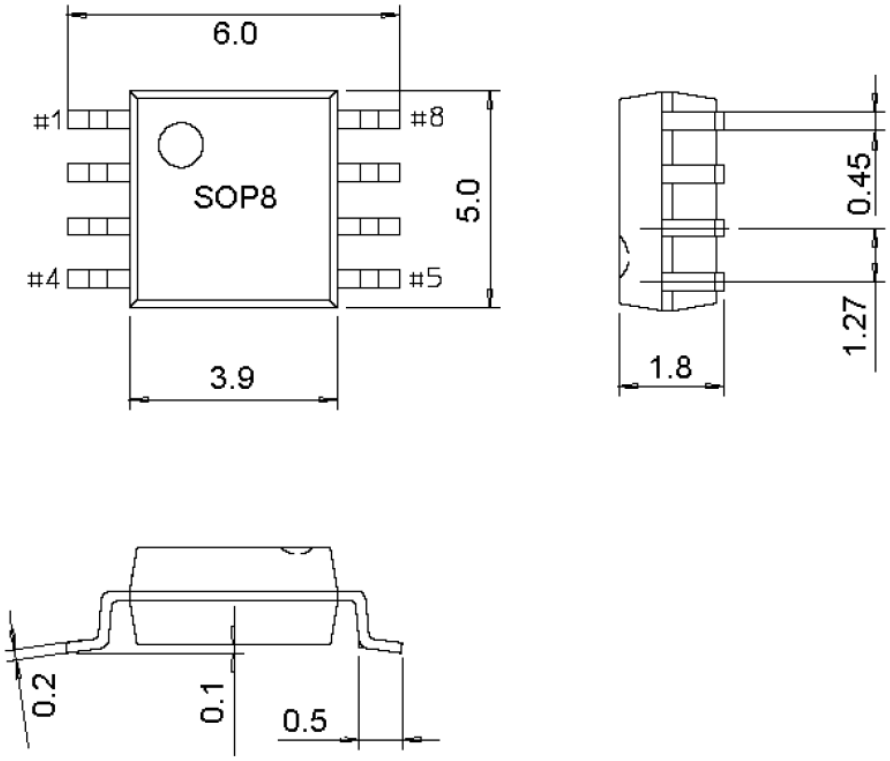


The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 17. Typical Application Circuit

PACKAGE OUTLINE DIMENSIONS

SOP-8



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