

Discription

The HSP4203-01FTG-Cprotects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. Excellent clamping capability, low leakage, low capacitance, and fast response time provide best in class protection on designs that are exposed to ESD. It gives designer the flexibility to protect one bi-directional line in applications where arrays are not practical.



SOD-323

Circuit Diagram



- ★ Ultra Low Capacitance 1 pF
- ★ Low Clamping Voltage
- ★ Low Body Height: 0.016" (0.4 mm)
- ★ Stand-off Voltage: 3.3 V
- ★ Low Leakage
- ★ Response Time is Typically < 1.0 ns
- ★ IEC61000-4-2 Level 4 ESD Protection
- ★ This is a Pb-Free Device

Orderingin formation

Product ID	Pack	Qty(PCS)
HSP4203-01FTG-C	SOD-323	3000

Absolute Ratings(Tamb = 25°C)

Symbol	Parameter	Value	Units
P _{PP}	Peak Pulse Power ($t_p = 8/20 \ \mu \ s$)	400	W
TL	Maximum lead temperature for soldering during 10s	260	°C
T _{stg}	Storage Temperature Range	-55 to +155	°C
T _{op}	Operating Temperature Range	-40 to +125	°C
Tj	Maximum junction temperature	150	°C
	IEC61000-4-2 (ESD) air discharge contact discharge	土10 土15	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Rating are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR-5 = 1.0*0.75*0.62 in.



Electrical Characteristics

	V _{RWM} (V)	I _R (μΑ) @ V _{RWM}	V _{BR} (V) @ I _T (Note 2)	ե	C (pF)	V _C (V) @ I _{PP} = 20 A (Note 3)	v _c
Device	Max	Мах	Min	mA	Тур	Max	Per IEC61000-4-2 (Note 4)
HSP4203-01FTG-C	3.3	1.0	5.4	1.0	1	20	Figures 1 and 2 See Below

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C. 3. Surge current waveform per Figure 5. 4. For test procedure see Figures 3 and 4.

Typical Characteristics

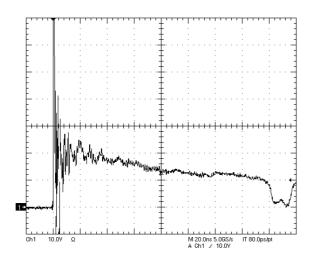
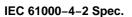


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2



Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

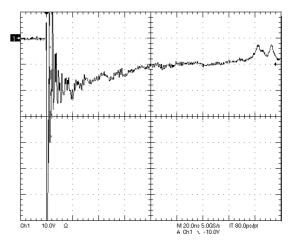
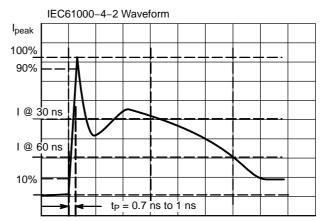
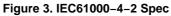


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2







Outline And Dimensions

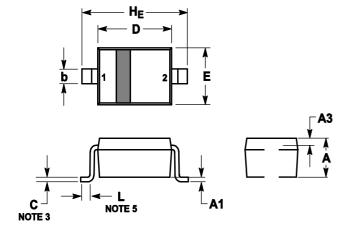
Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

2. CONTROLLING DIMENSION: MILLIMETERS.

3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

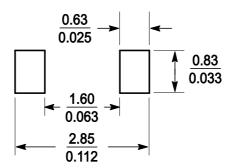
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD



FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS				INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
А	0.8	0.9	1	0.031	0.035	0.04	
A1	0	0.05	0.1	0	0.002	0.004	
A3	0.15REF			0	.006RE	F	
b	0.25	0.32	0.4	0.01	0.012	0.016	
С	0.089	0.12	0.177	0.003	0.005	0.007	
D	1.6	1.7	1.8	0.062	0.066	0.07	
Е	1.15	1.25	1.35	0.045	0.049	0.053	
L	0.08			0.003			
H _E	2.3	2.5	2.7	0.09	0.098	0.105	

Soledering Footprint





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