



Description

The IRF7105TRPBF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8

General Features

$V_{DS} = 30V$ $I_D = 6A$

$R_{DS(ON)} < 22m\Omega$ @ $V_{GS}=10V$

$V_{DS} = -30V$ $I_D = -5.5A$

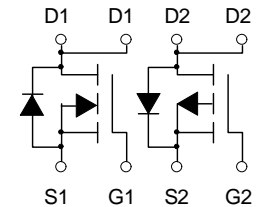
$R_{DS(ON)} < 45m\Omega$ @ $V_{GS}=-10V$

Application

Wireless charging

Boost driver

Brushless motor



N-Channel and P-Channel

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
IRF7105TRPBF	SOP-8	HXY MOSFET	3000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
VDS	Drain-Source Voltage	30	-30	V
VGS	Gate-Source Voltage	± 20	± 20	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	6	-5.5	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	5	-4.3	A
IDM	Pulsed Drain Current ²	30	-30	A
EAS	Single Pulse Avalanche Energy ³	5	26	mJ
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	2	2	W
TSTG	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62.5		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	40		$^\circ C/W$



N-Channel Electrical Characteristics (T_J =25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1.2	1.8	2.4	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =6A T _J =125°C		16 32	22 40	mΩ
		V _{GS} =4.5V, I _D =5A		22	30	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =6A		15		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.76	1	V
I _S	Maximum Body-Diode Continuous Current				2.5	A
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz	200	255	310	pF
C _{oss}	Output Capacitance		30	45	60	pF
C _{riss}	Reverse Transfer Capacitance		20	35	50	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.6	3.25	4.9	Ω
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =6A	4	5.2	6	nC
Q _{g(4.5V)}	Total Gate Charge		2	2.55	3	nC
Q _{gs}	Gate Source Charge			0.85		nC
Q _{gd}	Gate Drain Charge			1.3		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =2.5Ω, R _{GEN} =3Ω		4.5		ns
t _r	Turn-On Rise Time			2.5		ns
t _{D(off)}	Turn-Off DelayTime			14.5		ns
t _f	Turn-Off Fall Time			3.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =6A, di/dt=100A/μs		8.5	12	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =6A, di/dt=100A/μs		2.2	3	nC

- A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
- B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.
- C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.
- D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.



Typical Characteristics

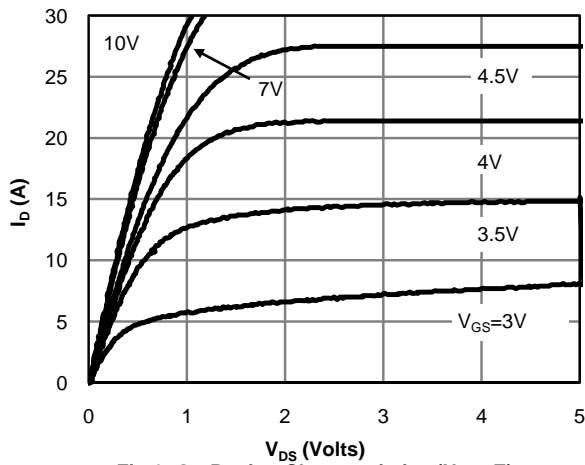


Figure 1: On-Region Characteristics (Note E)

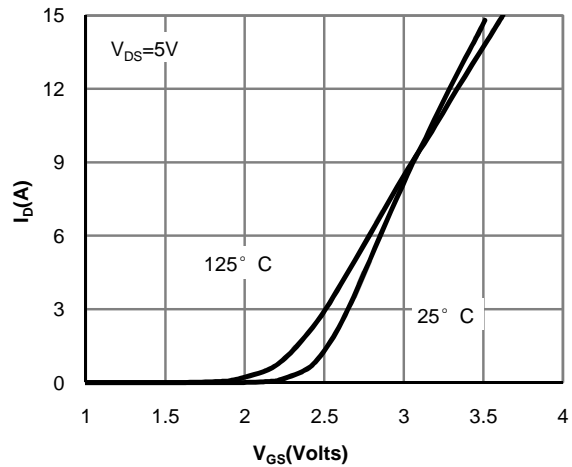


Figure 2: Transfer Characteristics (Note E)

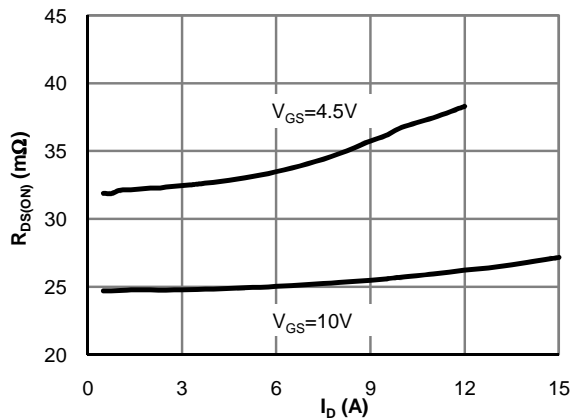


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

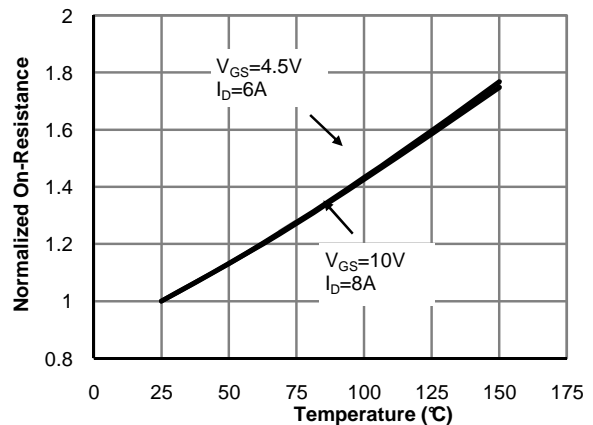


Figure 4: On-Resistance vs. Junction Temperature (Note E)

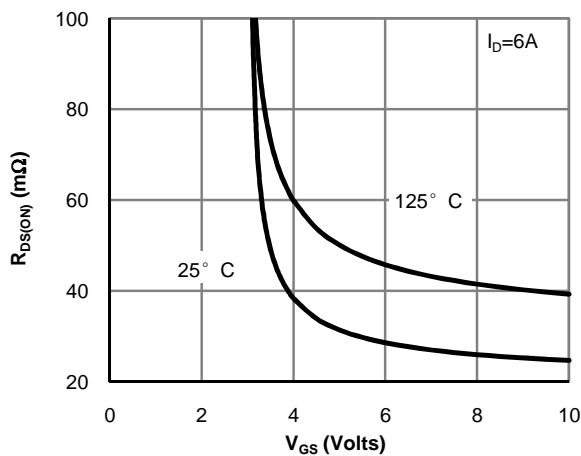


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

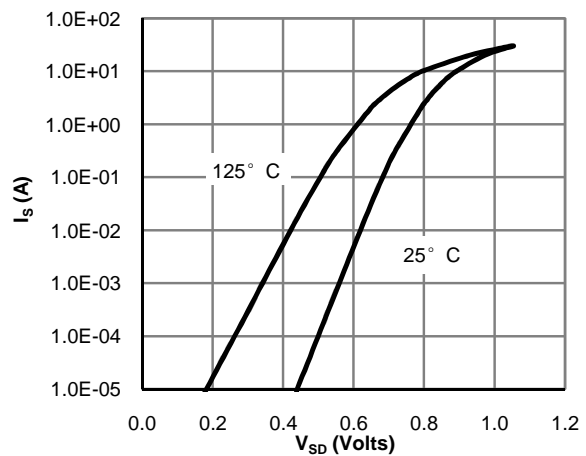


Figure 6: Body-Diode Characteristics (Note E)

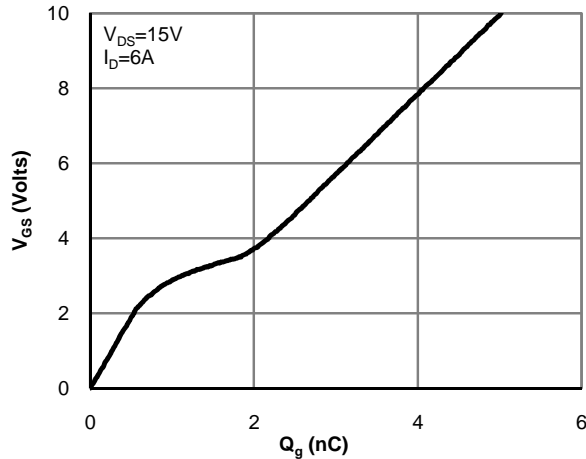


Figure 7: Gate-Charge Characteristics

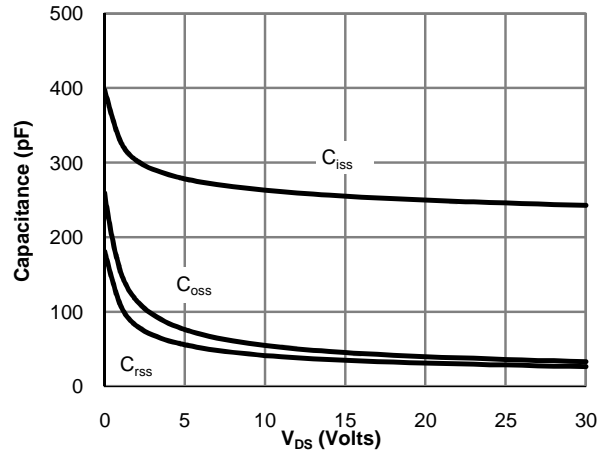


Figure 8: Capacitance Characteristics

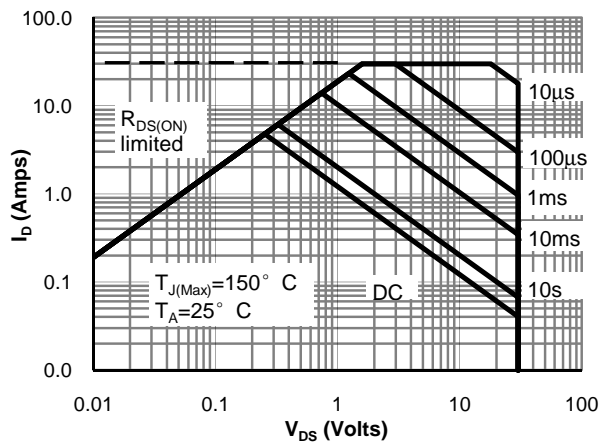


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

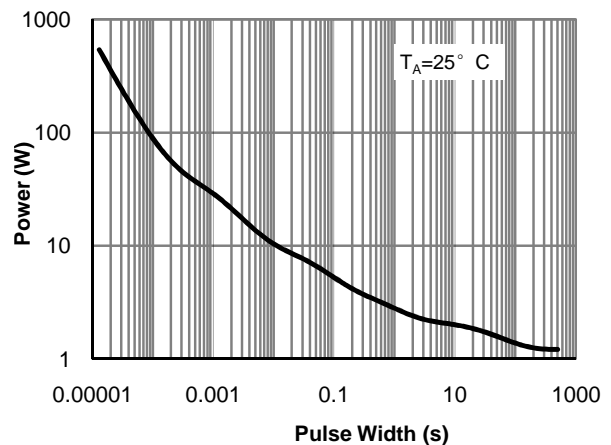


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

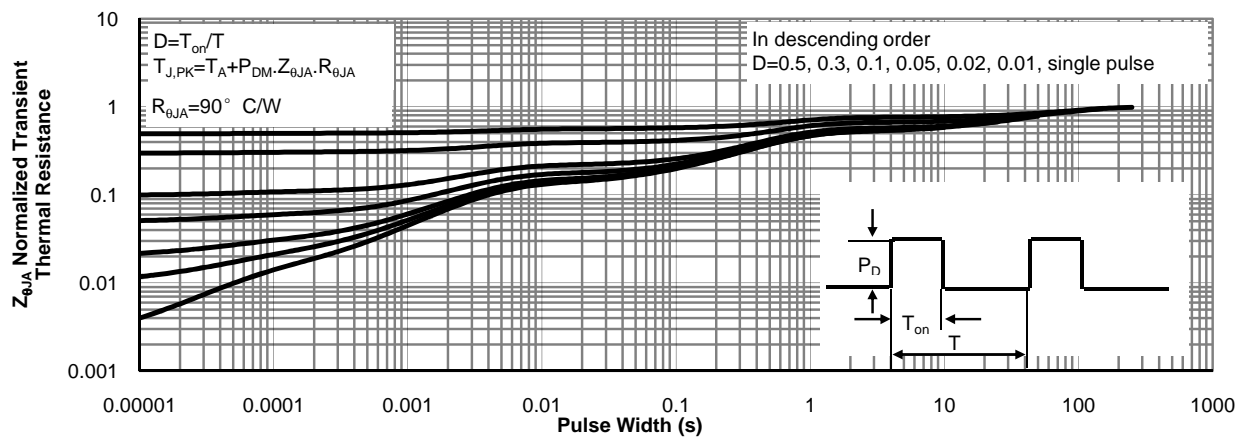
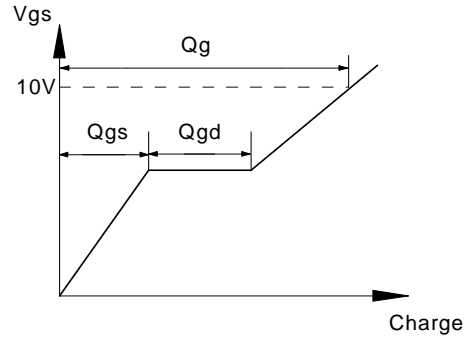
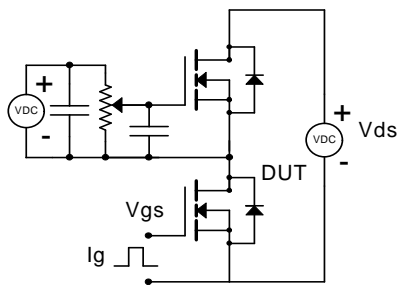


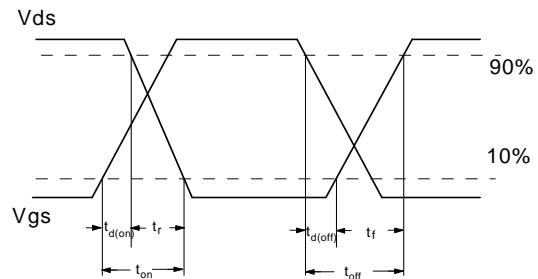
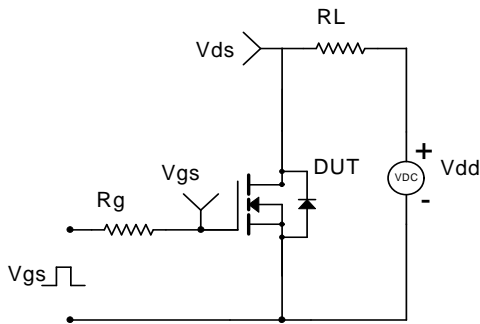
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



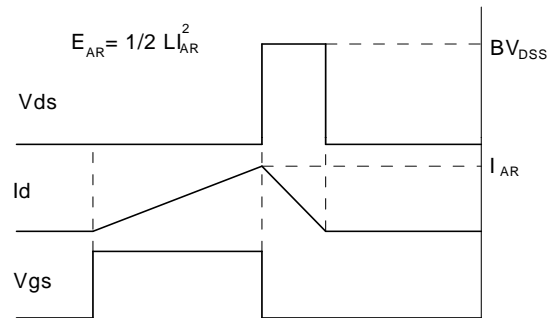
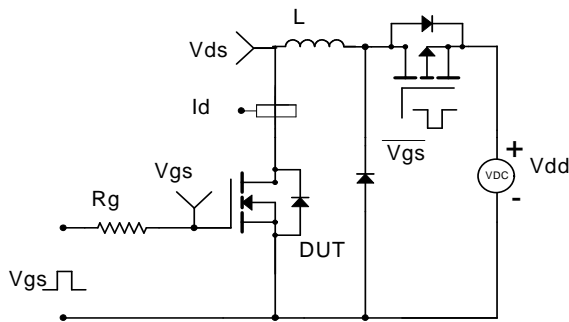
Gate Charge Test Circuit & Waveform



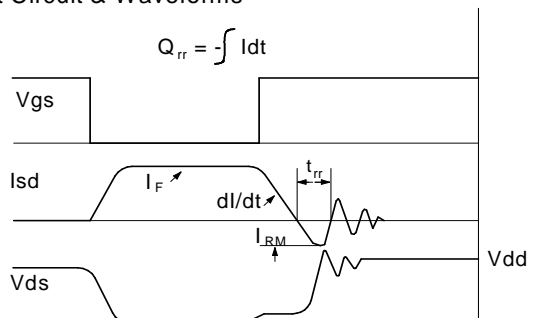
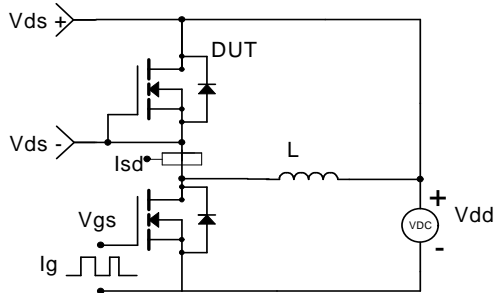
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms





P-Channel Electrical Characteristics (T_J =25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.3	-1.85	-2.4	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-6.5A T _J =125°C		36 32	45 40	mΩ
		V _{GS} =-4.5V, I _D =-5A		68	77	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-6.5A		18		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.8	-1	V
I _S	Maximum Body-Diode Continuous Current				-2.5	A
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		760		pF
C _{oss}	Output Capacitance			140		pF
C _{riss}	Reverse Transfer Capacitance			95		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.5	3.2	5	Ω
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =-15V, I _D =-6.5A		13.6	16	nC
Q _{g(4.5V)}	Total Gate Charge			6.7	8	nC
Q _{gs}	Gate Source Charge			2.5		nC
Q _{gd}	Gate Drain Charge			3.2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =-15V, R _L =2.3Ω, R _{GEN} =3Ω		8		ns
t _r	Turn-On Rise Time			6		ns
t _{D(off)}	Turn-Off DelayTime			17		ns
t _f	Turn-Off Fall Time			5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-6.5A, dI/dt=100A/μs		15		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-6.5A, dI/dt=100A/μs		9.7		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.



Typical Characteristics

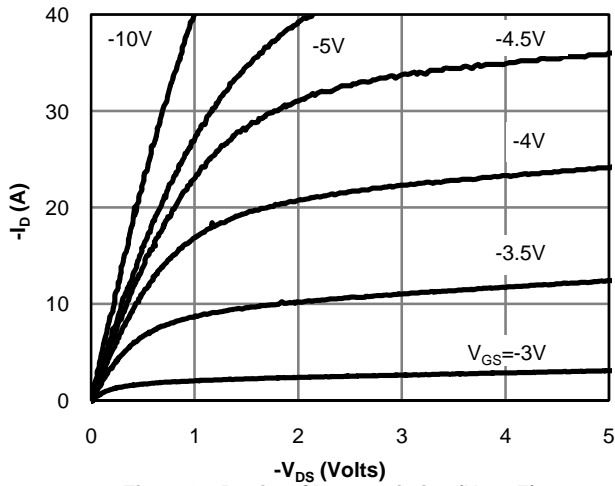


Fig 1: On-Region Characteristics (Note E)

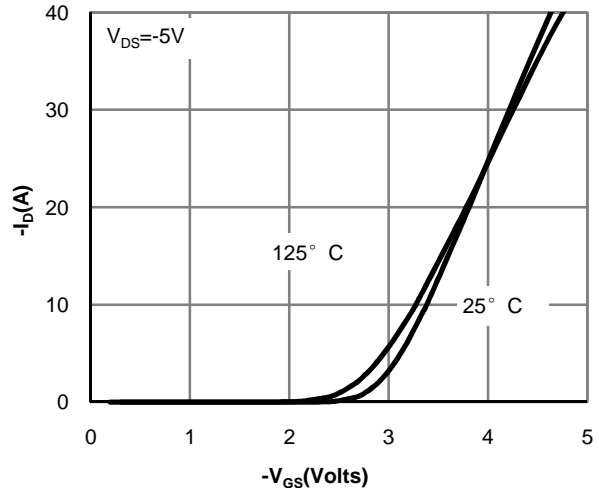


Figure 2: Transfer Characteristics (Note E)

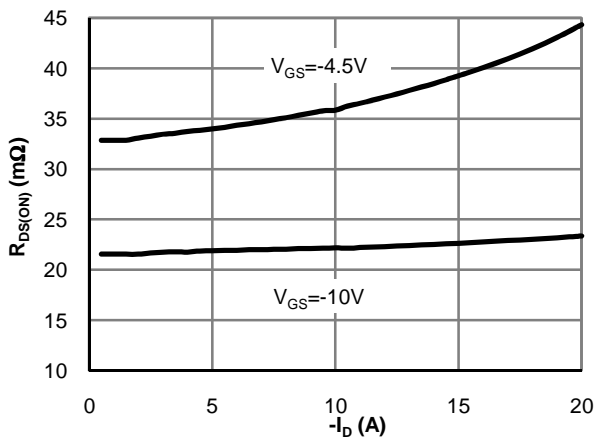


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

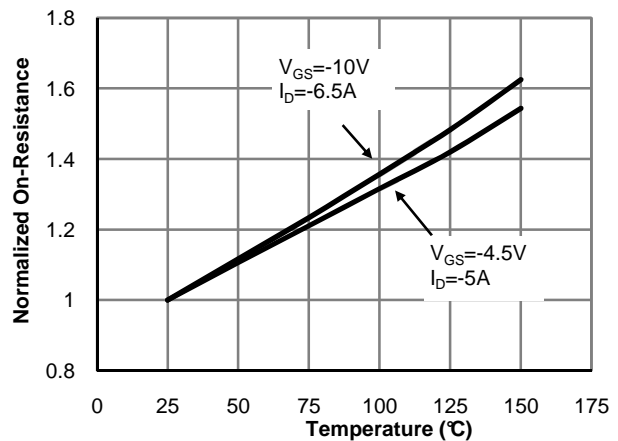


Figure 4: On-Resistance vs. Junction Temperature (Note E)

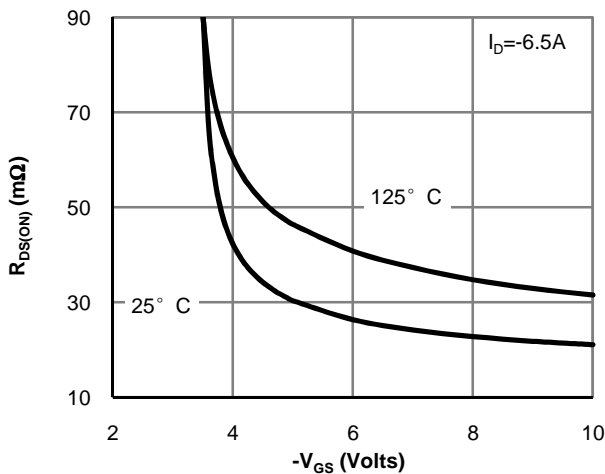


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

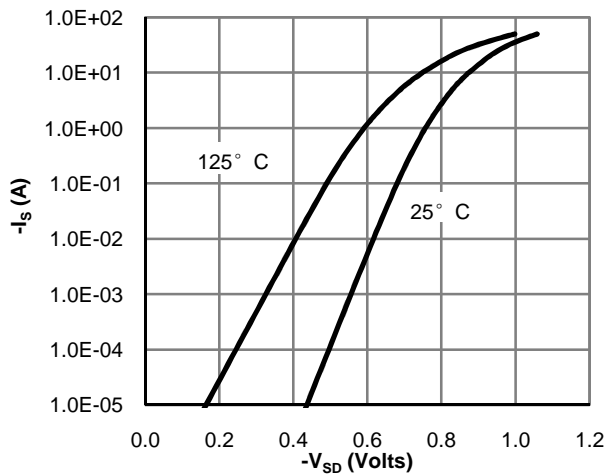


Figure 6: Body-Diode Characteristics (Note E)

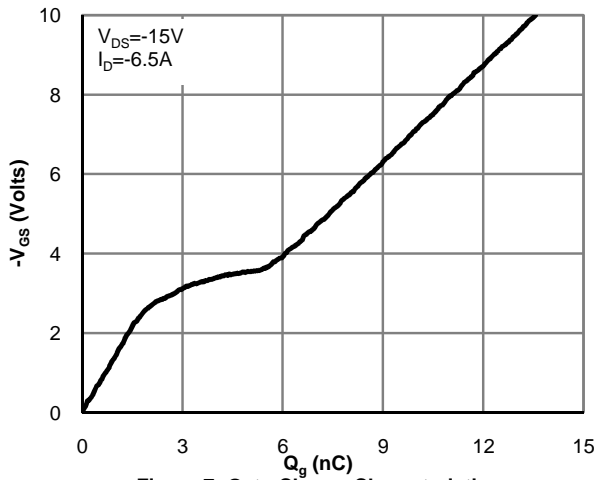


Figure 7: Gate-Charge Characteristics

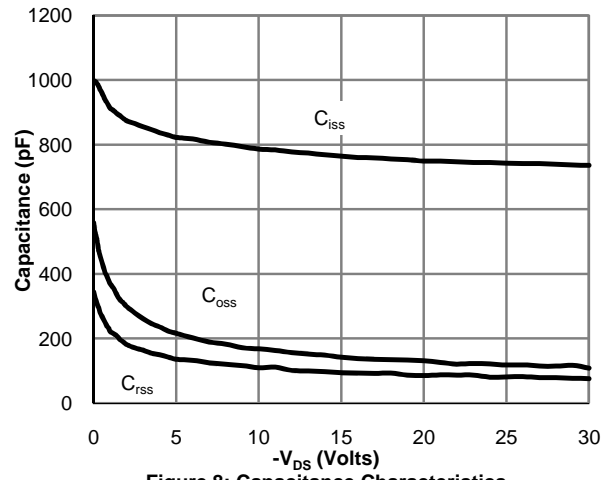
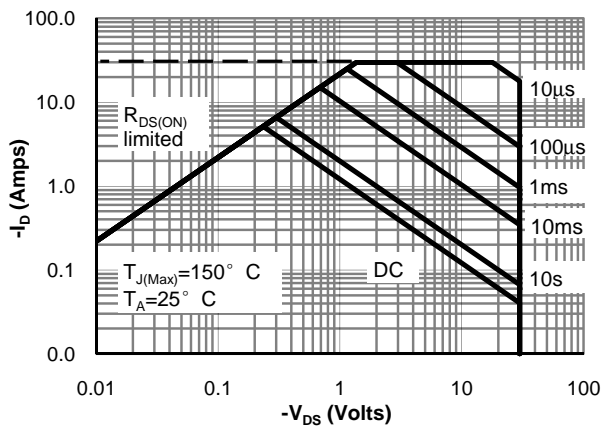
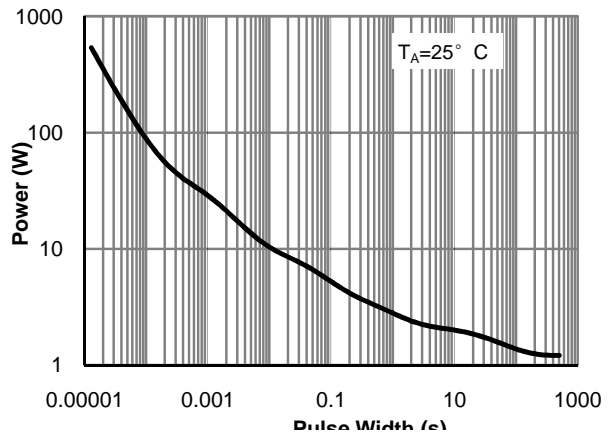


Figure 8: Capacitance Characteristics



Operating Area (Note F)



to-Ambient (Note F)

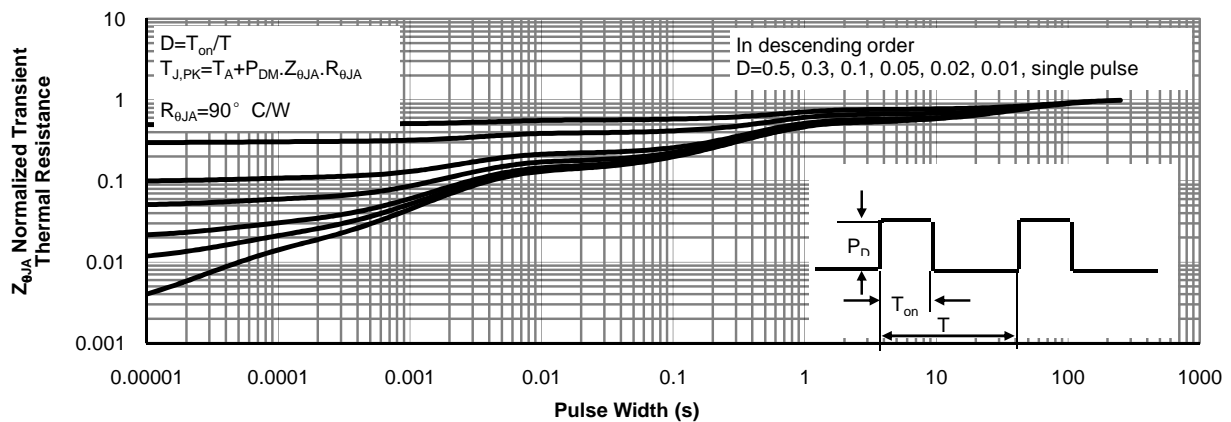
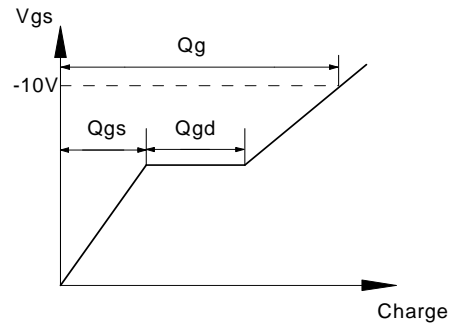
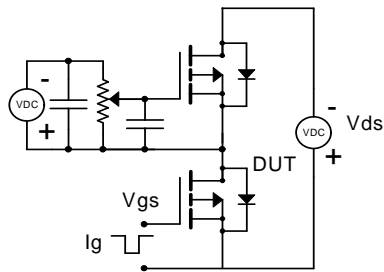


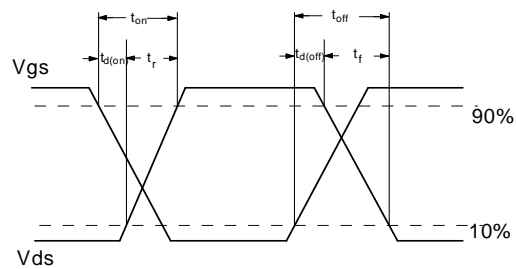
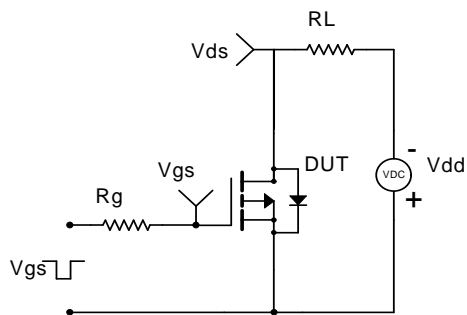
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



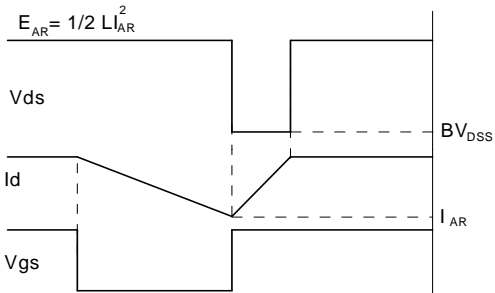
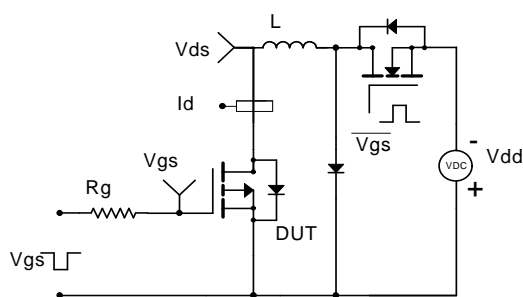
Gate Charge Test Circuit & Waveform



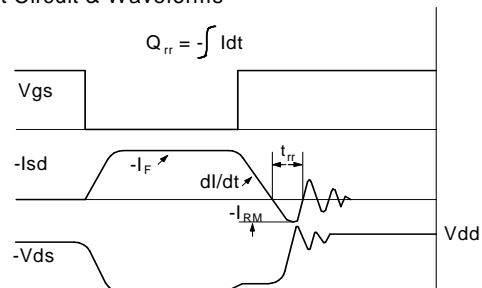
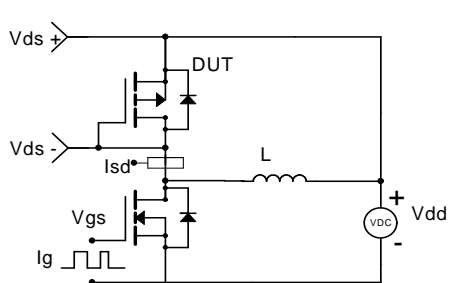
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

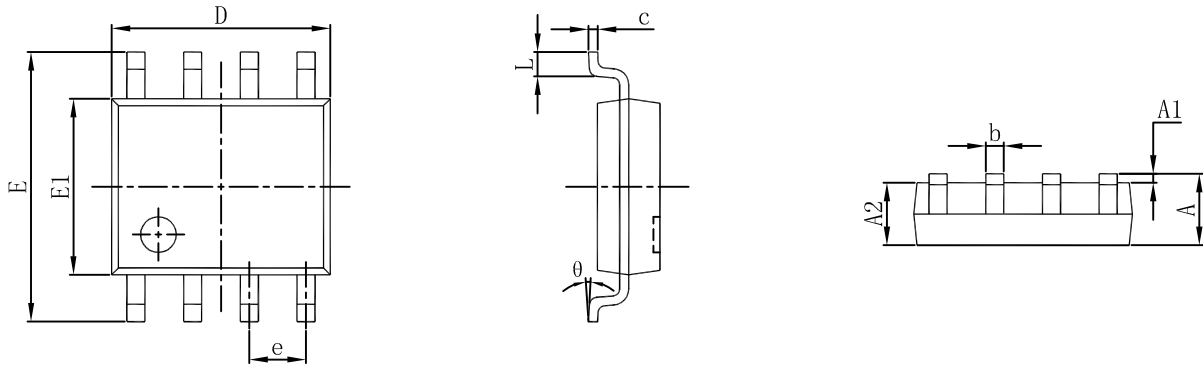


Diode Recovery Test Circuit & Waveforms

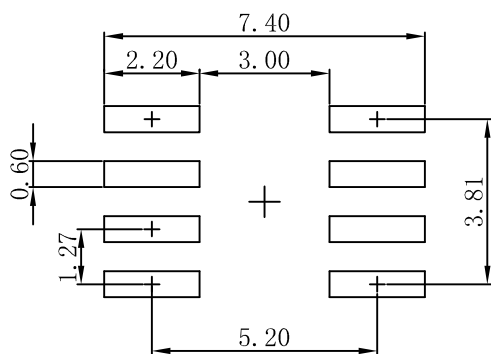




SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.



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[DMN2080UCB4-7](#) [DMN61D9UWQ-13](#) [US6M2GTR](#) [DMN31D5UDJ-7](#) [DMP22D4UFO-7B](#) [DMN1006UCA6-7](#) [DMN16M9UCA6-7](#)
[STF5N65M6](#) [IRF40H233XTMA1](#) [STU5N65M6](#) [DMN6022SSD-13](#) [DMN13M9UCA6-7](#) [DMTH10H4M6SPS-13](#) [DMN2990UFB-7B](#)
[IPB80P04P405ATMA2](#) [2N7002W-G](#) [MCAC30N06Y-TP](#) [MCQ7328-TP](#) [BXP7N65D](#) [BXP4N65F](#) [AOL1454G](#) [WMJ80N60C4](#) [BXP2N20L](#)
[BXP2N65D](#) [BXT1150N10J](#) [BXT1700P06M](#) [TSM60NB380CP ROG](#) [RQ7L055BGTCR](#) [DMNH15H110SK3-13](#) [SLF10N65ABV2](#)
[BSO203SP](#) [BSO211P](#) [IPA60R230P6](#) [IPA60R460CE](#)