

#### **Description**

The IRF7404PBF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features SOP-8

 $V_{DS} = -20V I_{D} = -20A$ 

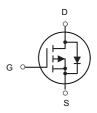
 $R_{DS(ON)}$  < 19m $\Omega$ @  $V_{GS}$ =10V

## **Application**

Battery protection

Load switch

Uninterruptible power supply



P-Channel MOSFET

## Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
IRF7404PBF	SOP-8	F7404 XXXX	3000

## Absolute Maximum Ratings (Tc=25°C unless otherwise noted )

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	-20	V
Vgs	Gate-Source Voltage	<u>+</u> 12	
ID@TA=25°C	Drain Current <sup>3</sup> , V <sub>GS</sub> @ 10V	-20	Α
ID@TA=70°C	Drain Current <sup>3</sup> , V <sub>GS</sub> @ 10V	-16	Α
Ідм	Pulsed Drain Current <sup>1</sup>	-68	Α
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation	18	W
Тѕтс	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C
Rthj-a	Maximum Thermal Resistance, Junction- ambient <sup>3</sup>	75	°C/W



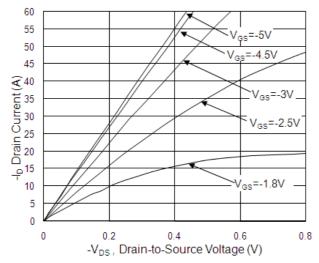
#### Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-20			V	
$\triangle BV_{DSS}/\triangle T_{J}$	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =-1mA		-0.012		V/°C	
		V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-10A		15	19		
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-2.5V , I <sub>D</sub> =-8A		19	23	mΩ	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V V 1 050-A	-0.4	-0.7	-1.0	V	
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	$V_{GS}=V_{DS}$ , $I_D=-250uA$		2.94		mV/°C	
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-15V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			1	uA	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±12 V , V <sub>DS</sub> =0V			±100	nA	
gfs	Forward Transconductance	V <sub>DS</sub> =-5V , I <sub>D</sub> =-10A		43		S	
Qg	Total Gate Charge (-4.5V)			35			
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =-10V , V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-10A		5.0		nC	
Q <sub>gd</sub>	Gate-Drain Charge			10			
T <sub>d(on)</sub>	Turn-On Delay Time			12.0			
Tr	Rise Time	V <sub>DD</sub> =-10V , V <sub>GS</sub> =-4.5V ,		40.0		20	
$T_{d(off)}$	Turn-Off Delay Time	R <sub>G</sub> =3.3Ω, I <sub>D</sub> =-10A		30		ns	
T <sub>f</sub>	Fall Time			10			
Ciss	Input Capacitance			2800			
Coss	Output Capacitance	V <sub>DS</sub> =-15V , V <sub>GS</sub> =0V , f=1MHz		690		pF	
C <sub>rss</sub>	Reverse Transfer Capacitance			590			
ls	Continuous Source Current <sup>1,4</sup>	Vo=Vo=0V Force Current			-20.0	Α	
I <sub>SM</sub>	Pulsed Source Current <sup>2,4</sup>	──V <sub>G</sub> =V <sub>D</sub> =0V , Force Current				Α	
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , T <sub>J</sub> =25°C			-1.2	٧	
t <sub>rr</sub>	Reverse Recovery Time	IF=-10A , dI/dt=100A/μs ,		27	-	nS	
Qrr	Reverse Recovery Charge	T <sub>J</sub> =25°C		17.8		nC	

#### Note:

- 1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%
- 3.The power dissipation is limited by 150°C junction temperature
- 4. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

## **Typical Characteristics**



**Fig.1 Typical Output Characteristics** 

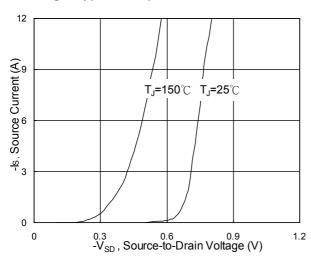


Fig.3 Forward Characteristics of Reverse

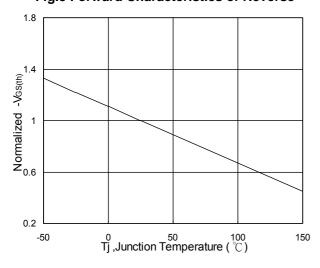


Fig.5 Normalized  $V_{\text{GS(th)}}$  vs.  $T_{\text{J}}$ 

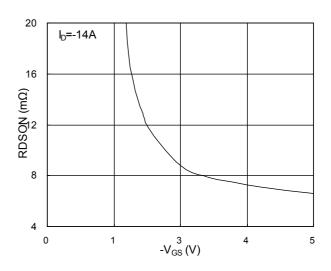


Fig.2 On-Resistance vs. G-S Voltage

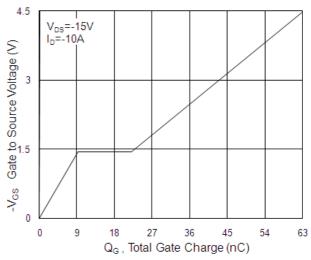


Fig.4 Gate-charge Characteristics

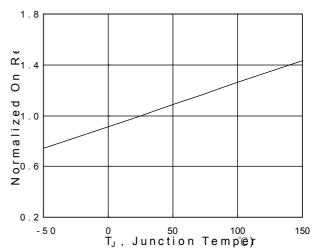
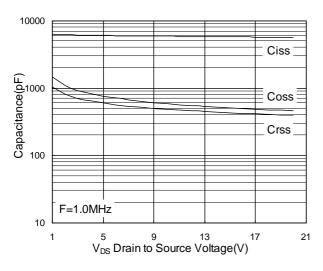


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>



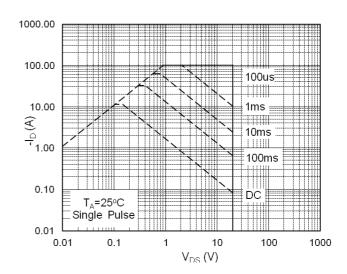


Fig.7 Capacitance

Fig.8 Safe Operating Area

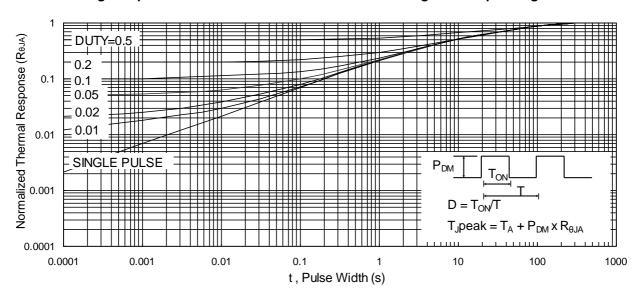
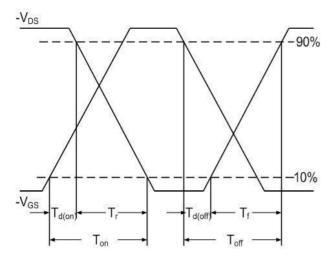


Fig.9 Normalized Maximum Transient Thermal Impedance



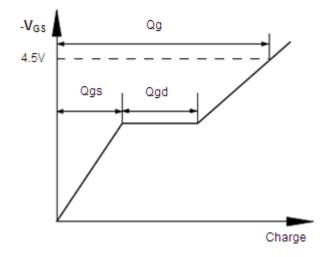
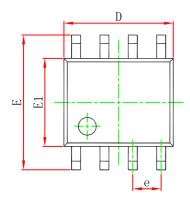
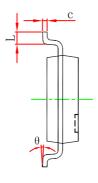


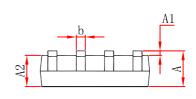
Fig.10 Switching Time Waveform

Fig.11 Gate Charge Waveform

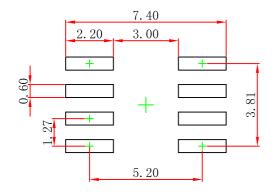
# **SOP-8 Package Outline Dimensions**







Symbol	Dimensions In Millimeters		Dimensions In Inches	
Symbol	Min	Max	Min	Max
A	1. 350	1.750	0.053	0.069
A1	0.100	0. 250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0. 197
e	1. 270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0. 244
E1	3.800	4.000	0.150	0. 157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



- Note: 1.Controlling dimension:in millimeters.
- 2.General tolerance:± 0.05mm.
  3.The pad layout is for reference purposes only.

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