

## **Description**

The IRLML5103PBF uses advanced trench technology to provide excellent  $R_{\text{DS(ON)}}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



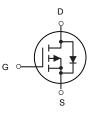
#### **General Features**

 $V_{DS}$  = -30V, $I_D$  = -4.1A  $R_{DS(ON)}$  <56m $\Omega$  @  $V_{GS}$ =10V

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### **Application**

High power and current handing capability
Lead free product is acquired
Surface mount package
PWM applications
Load switch
Power management



P-Channel MOSFET

### **Package Marking and Ordering Information**

Product ID	Pack	Brand	Qty(PCS)
IRLML5103PBF	SOT-23	HXY MOSFET	3000

## Absolute Maximum Ratings (T<sub>A</sub>=25 ℃ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V <sub>DS</sub>	Drain-Source Voltage	-30	V
V <sub>G</sub> s	Gate-Source Voltage	±20	V
<b>I</b> D	Drain Current-Continuous	-4.1	А
Ідм	Drain Current-Pulsed (Note 1)	-13	А
P <sub>D</sub>	Maximum Power Dissipation	1.32	W
Тл,Тѕтс	Operating Junction and Storage Temperature Range	-55 To 150	$^{\circ}$
Reja	Thermal Resistance, Junction-to-Ambient (Note 2)	125	°C/W



### Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-30			V
△BV <sub>DSS</sub> /△T <sub>J</sub>	BVDSS Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =-1mA		-0.02		V/°C
Б	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V , I <sub>D</sub> =-3A		48	56	
RDS(ON)		V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-1.5A		78	90	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	VV I- = 2500A	-1.2	-1.5	-2.5	V
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	$V_{GS}=V_{DS}$ , $I_D=-250uA$		4.32		mV/°C
	Drain-Source Leakage Current	V <sub>DS</sub> =-24V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			-1	- uA
I <sub>DSS</sub>		V <sub>DS</sub> =-24V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			-5	
Igss	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =-5V , I <sub>D</sub> =-3A		4.8		S
Rg	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		24	48	Ω
Qg	Total Gate Charge (-4.5V)			5.22	7.3	
Qgs	Gate-Source Charge	V <sub>DS</sub> =-20V , V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-3A		1.25	1.8	nC
Q <sub>gd</sub>	Gate-Drain Charge			2.3	3.2	
T <sub>d(on)</sub>	Turn-On Delay Time			18.4	37	
Tr	Rise Time	$V_{DD}$ =-15V , $V_{GS}$ =-10V , $R_{G}$ =3.3 $\Omega$		11.4	21	ns
T <sub>d(off)</sub>	Turn-Off Delay Time	I <sub>D</sub> =-1A		39.4	79	
T <sub>f</sub>	Fall Time			5.2	10.4	
Ciss	Input Capacitance			463	650	
Coss	Output Capacitance V <sub>DS</sub> =-15V , V <sub>GS</sub> =0V , f=1MHz			82	115	pF
Crss	Reverse Transfer Capacitance			68	95	
Is	Continuous Source Current <sup>1,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			-3.2	Α
I <sub>SM</sub>	Pulsed Source Current <sup>2,4</sup>	vg-vb-ov , roice Curiefit	-		-13	Α
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , T <sub>J</sub> =25°C			-1	V

#### Note:

<sup>1.</sup> The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.

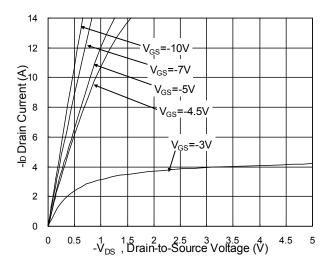
<sup>2.</sup>The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%

<sup>3.</sup>The power dissipation is limited by 150°C junction temperature

<sup>4.</sup> The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



### **Typical Characteristics**



**Fig.1 Typical Output Characteristics** 

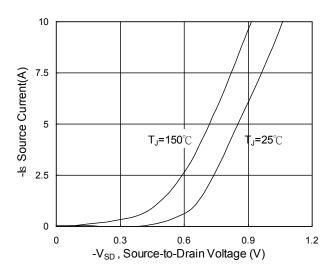


Fig.3 Source Drain Forward Characteristics

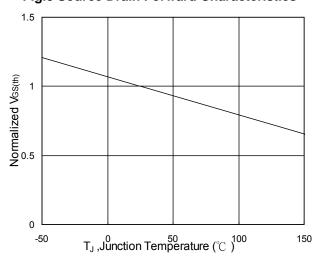


Fig.5 Normalized V<sub>GS(th)</sub> vs. T<sub>J</sub>

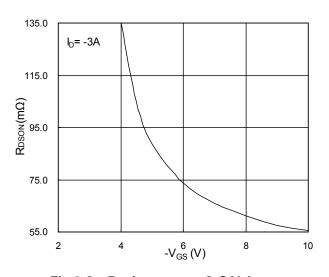


Fig.2 On-Resistance vs. G-S Voltage

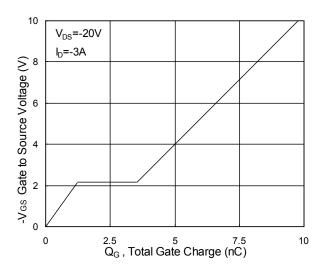


Fig.4 Gate-Charge Characteristics

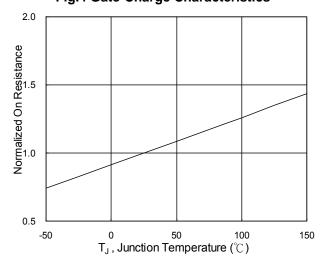
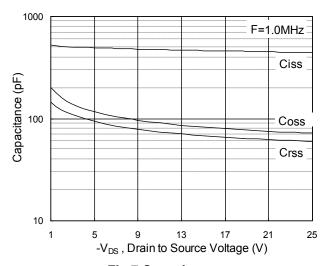


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>





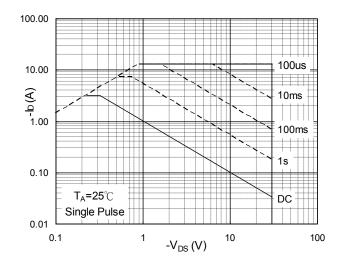


Fig.7 Capacitance

Fig.8 Safe Operating Area

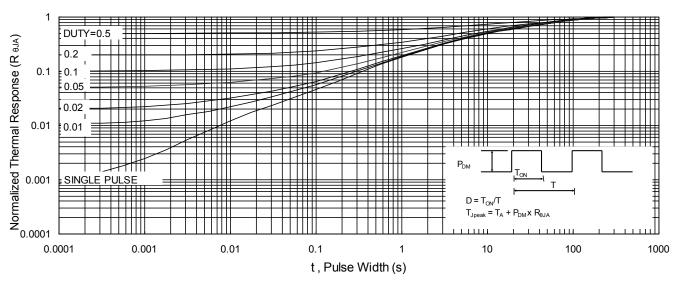
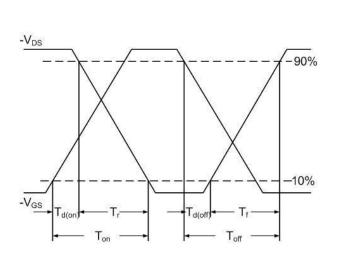


Fig.9 Normalized Maximum Transient Thermal Impedance



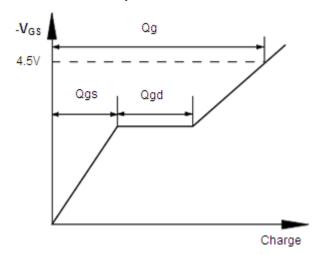
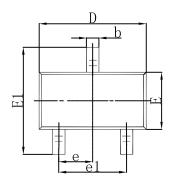


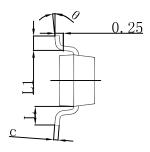
Fig.10 Switching Time Waveform

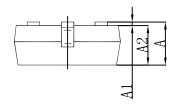
Fig.11 Gate Charge Waveform



## **SOT-23 Package Outline Dimensions**

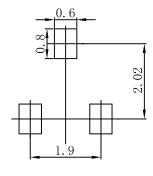






Cumbal	Dimensions In Millimeters		Dimensions In Inches		
Symbol	Min	Max	Min	Max	
Α	0.900	1.150	0.035	0.045	
A1	0.000	0.100	0.000	0.004	
A2	0.900	1.050	0.035	0.041	
b	0.300	0.500	0.012	0.020	
С	0.080	0.150	0.003	0.006	
D	2.800	3.000	0.110	0.118	
E	1.200	1.400	0.047	0.055	
E1	2.250	2.550	0.089	0.100	
е	0.950 TYP		0.037 TYP		
e1	1.800	2.000	0.071	0.079	
L	0.550 REF		0.022 REF		
L1	0.300	0.500	0.012	0.020	
θ	0°	8°	0°	8°	

## **SOT-23 Suggested Pad Layout**



#### Note:

- 1.Controlling dimension:in millimeters.
- 2.General tolerance:± 0.05mm.
  3.The pad layout is for reference purposes only.



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